TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74ACT138P, TC74ACT138F, TC74ACT138FN, TC74ACT138FT

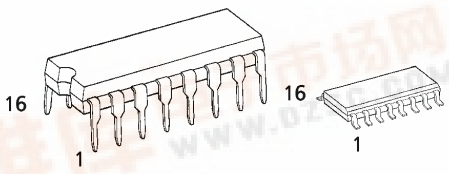
3 – TO – 8 LINE DECODER

The TC74ACT138 is an advanced high speed CMOS 3 - to - 8 LINE DECODER fabricated with silicon gate and double - layer metal wiring C^2MOS technology.
It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.
This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.
When the device is enabled, 3 Binary Select inputs (A, B and C) determine which one of the outputs ($\overline{Y}0$ - $\overline{Y}7$) will go low.
When enable input G1 is held low or either $\overline{G}2A$ or $\overline{G}2B$ is held high, decoding function is inhibited and all outputs go high.
G1, $\overline{G}2A$, and $\overline{G}2B$ inputs are provided to ease cascade connection and for use as an address decoder for memory systems.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

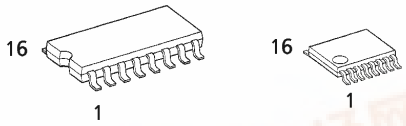
FEATURES :

- High Speed ····· t_{pd} = 6.0ns(typ.) at V_{CC} = 5V
- Low Power Dissipation ····· I_{CC} = 8μA(Max.) at Ta = 25°C
- Compatible with TTL outputs ··· V_{IL} = 0.8V (Max.)
  V_{IH} = 2.0V (Min.)
- Symmetrical Output Impedance··· $|I_{OH}|$ = I_{OL} = 24mA(Min.)
  Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ····· $t_{pLH} \simeq t_{pHL}$
- Pin and Function Compatible with 74F138

(Note) The JEDEC SOP (FN) is not available in Japan.

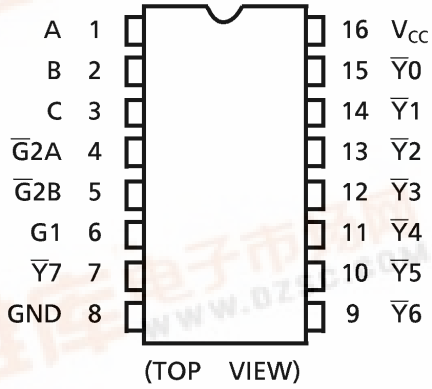


P (DIP16-P-300-2.54A) Weight : 1.00g (Typ.)
FN (SOL16-P-150-1.27) Weight : 0.13g (Typ.)

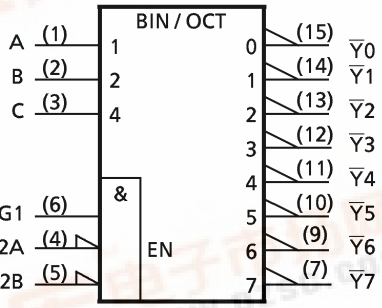


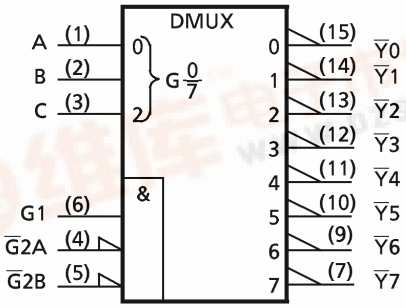
F (SOP16-P-300-1.27) Weight : 0.18g (Typ.)
FT (TSSOP16-P-0044-0.65) Weight : 0.06g (Typ.)

PIN ASSIGNMENT



IEC LOGIC SYMBOL





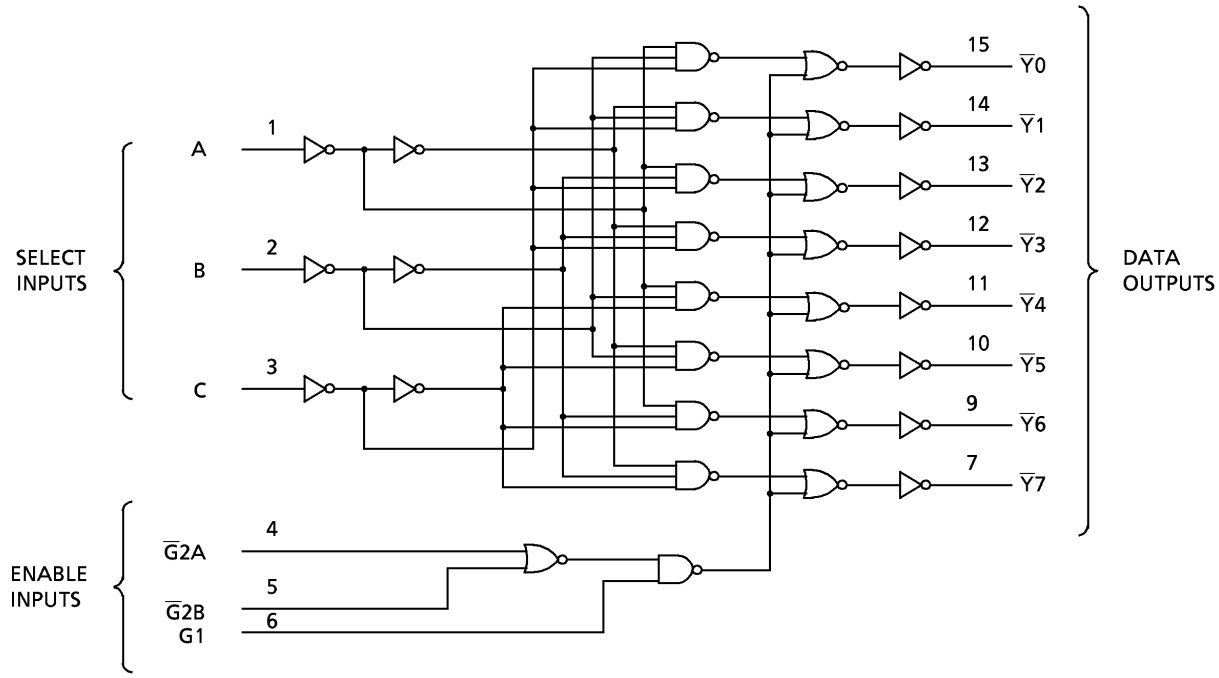
961001EBA2

TRUTH TABLE

INPUTS						OUTPUTS								SELECTED OUTPUT
ENABLE			SELECT			$\overline{Y}0$	$\overline{Y}1$	$\overline{Y}2$	$\overline{Y}3$	$\overline{Y}4$	$\overline{Y}5$	$\overline{Y}6$	$\overline{Y}7$	
G1	$\overline{G}2A$	$\overline{G}2B$	C	B	A									
L	X	X	X	X	X	H	H	H	H	H	H	H	H	NONE
X	H	X	X	X	X	H	H	H	H	H	H	H	H	NONE
X	X	H	X	X	X	H	H	H	H	H	H	H	H	NONE
H	L	L	L	L	L	L	H	H	H	H	H	H	H	$\overline{Y}0$
H	L	L	L	L	H	H	L	H	H	H	H	H	H	$\overline{Y}1$
H	L	L	L	H	L	H	H	L	H	H	H	H	H	$\overline{Y}2$
H	L	L	L	H	H	H	H	H	L	H	H	H	H	$\overline{Y}3$
H	L	L	H	L	L	H	H	H	H	L	H	H	H	$\overline{Y}4$
H	L	L	H	L	H	H	H	H	H	H	L	H	H	$\overline{Y}5$
H	L	L	H	H	L	H	H	H	H	H	H	L	H	$\overline{Y}6$
H	L	L	H	H	H	H	H	H	H	H	H	H	L	$\overline{Y}7$

X : Don't Care

LOGIC DIAGRAM



961001EBA2'

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±200	mA
Power Dissipation	P_D	500 (DIP)* / 180 (SOP/TSSOP)	mW
Storage Temperature	T_{stg}	−65~150	°C

*500mW in the range of Ta = −40°C~65°C. From Ta = 65°C to 85°C a derating factor of −10mW/°C should be applied up to 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5~5.5	V
Input Voltage	V_{IN}	0~V_{CC}	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	dt / dV	0~10	ns / V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C MIN.	Ta = 25°C TYP.	Ta = 25°C MAX.	Ta = −40~85°C MIN.	Ta = −40~85°C MAX.	UNIT
High - Level Input Voltage	V_{IH}			4.5 ~ 5.5	2.0	−	−	2.0	−	V
Low - Level Input Voltage	V_{IL}			4.5 ~ 5.5	−	−	0.8	−	0.8	V
High - Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50μA I_{OH} = −24mA I_{OH} = −75mA*	4.5 4.5 5.5	4.4 3.94 −	4.5 − −	− − −	4.4 3.80 3.85	− − −	V
Low - Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50μA I_{OL} = 24mA I_{OL} = 75mA*	4.5 4.5 5.5	− − −	0.0 − −	0.1 0.36 −	− − −	0.1 0.44 1.65	V
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	−	−	8.0	−	80.0	μA
	I_C	PER INPUT : V_{IN} = 3.4V OTHER INPUT : V_{CC} or GND		5.5	−	−	1.35	−	1.5	mA

* : This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

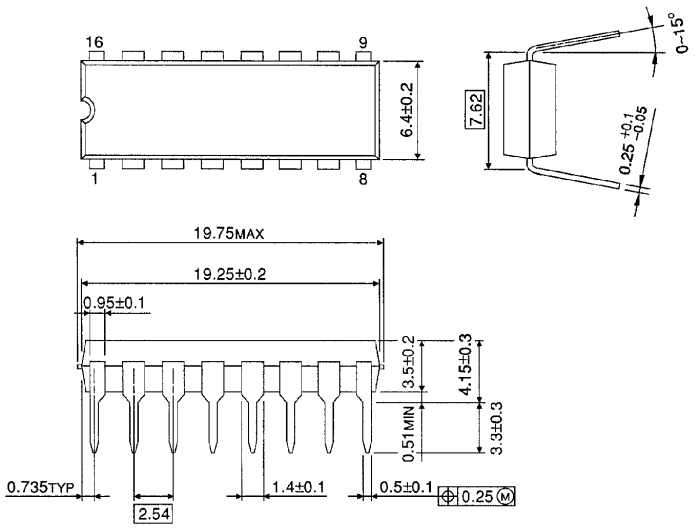
AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, R_L = 500Ω, Input $t_r = t_f$ = 3ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C			Ta = −40~85°C		UNIT
			V_{CC} (V)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (A, B, C−$\overline{Y}$)	t_{pLH} t_{pHL}		5.0 ± 0.5	−	6.7	10.1	1.0	11.5	ns
Propagation Delay Time (G1−$\overline{Y}$)	t_{pLH} t_{pHL}		5.0 ± 0.5	−	6.8	10.5	1.0	12.0	
Propagation Delay Time ($\overline{G}$2−$\overline{Y}$)	t_{pLH} t_{pHL}		5.0 ± 0.5	−	6.9	11.0	1.0	12.5	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD} (1)			−	55	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

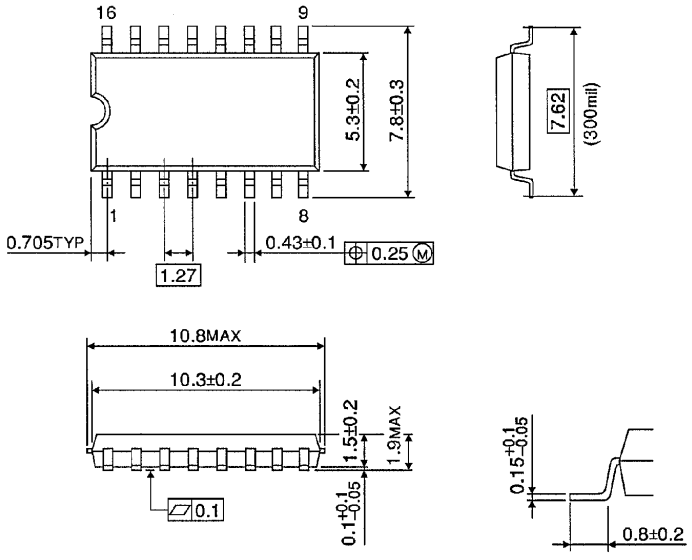
$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

DIP 16PIN OUTLINE DRAWING (DIP16-P-300-2.54A) Unit in mm



Weight : 1.00g (Typ.)

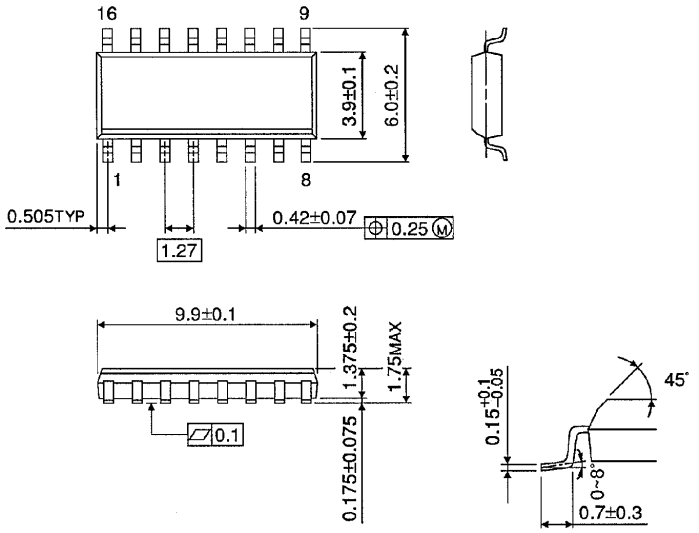
SOP 16PIN (200mil BODY) OUTLINE DRAWING (SOP16-P-300-1.27) Unit in mm



Weight : 0.18g (Typ.)

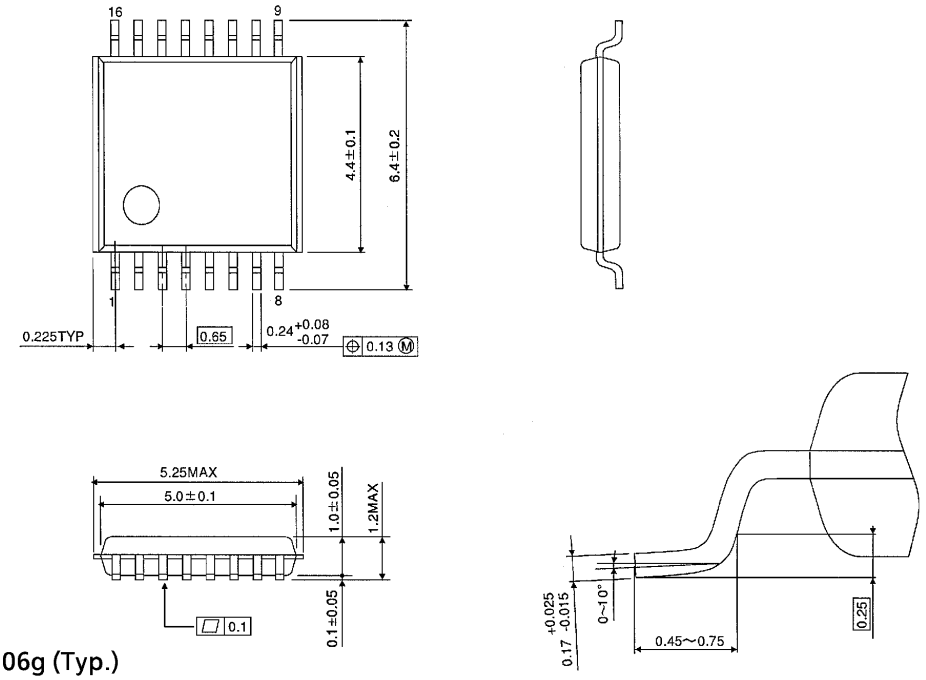
SOP 16PIN (150mil BODY) OUTLINE DRAWING (SOL16-P-150 -1.27) Unit in mm

(Note) This package is not available in Japan.



Weight : 0.13g (Typ.)

TSSOP 16PIN OUTLINE DRAWING (TSSOP16-P-0044-0.65) Unit in mm



Weight : 0.06g (Typ.)