TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74ACT280P, TC74ACT280F, TC74ACT280FN

9 – BIT PARITY GENERATOR / CHECKER

(Note) The JEDEC SOP (FN) is not available in Japan.

The TC74ACT280 is an advanced high speed CMOS 9 - BIT PARITY GENERATOR fabricated with silicon gate and double - layer metal wiring C²MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.

The TC74ACT280 is composed of nine data inputs (A thru I) and odd / even parity outputs (Σ ODD and Σ EVEN).

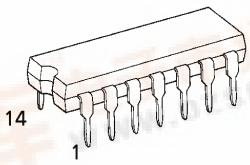
The odd parity output is high when an odd number of data inputs are high. The even parity output is high when an even number of data inputs are high.

The word - length capability is easily expanded by cascading.

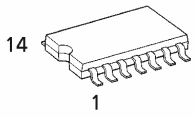
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES :

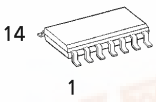
- High Speed ····· t_{pd} = 9.2ns(typ.) at V_{CC} = 5V
- Low Power Dissipation ····· I_{CC} = 8μA(Max.) at Ta = 25°C
- Compatible with TTL outputs ····· V_{IL} = 0.8V (Max.)
  V_{IH} = 2.0V (Min.)
- Symmetrical Output Impedance ··· | I_{OH} | = I_{OL} = 24mA(Min.)
  Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ····· $t_{pLH} \simeq t_{pHL}$
- Pin and Function Compatible with 74F280



P (DIP14-P-300-2.54)
Weight : 0.96g (Typ.)

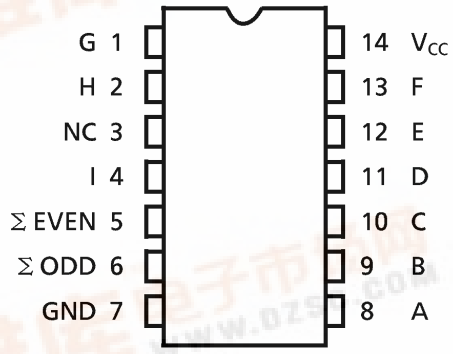


F (SOP14-P-300-1.27)
Weight : 0.18g (Typ.)



FN (SOL14-P-150-1.27)
Weight : 0.12g (Typ.)

PIN ASSIGNMENT

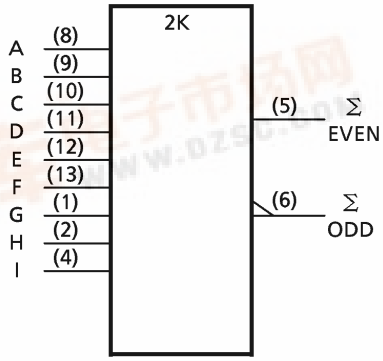


(TOP VIEW)
NC:No Connection

TRUTH TABLE

Number of inputs A through I that are High	Outputs	
	Σ EVEN	Σ ODD
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

IEC LOGIC SYMBOL



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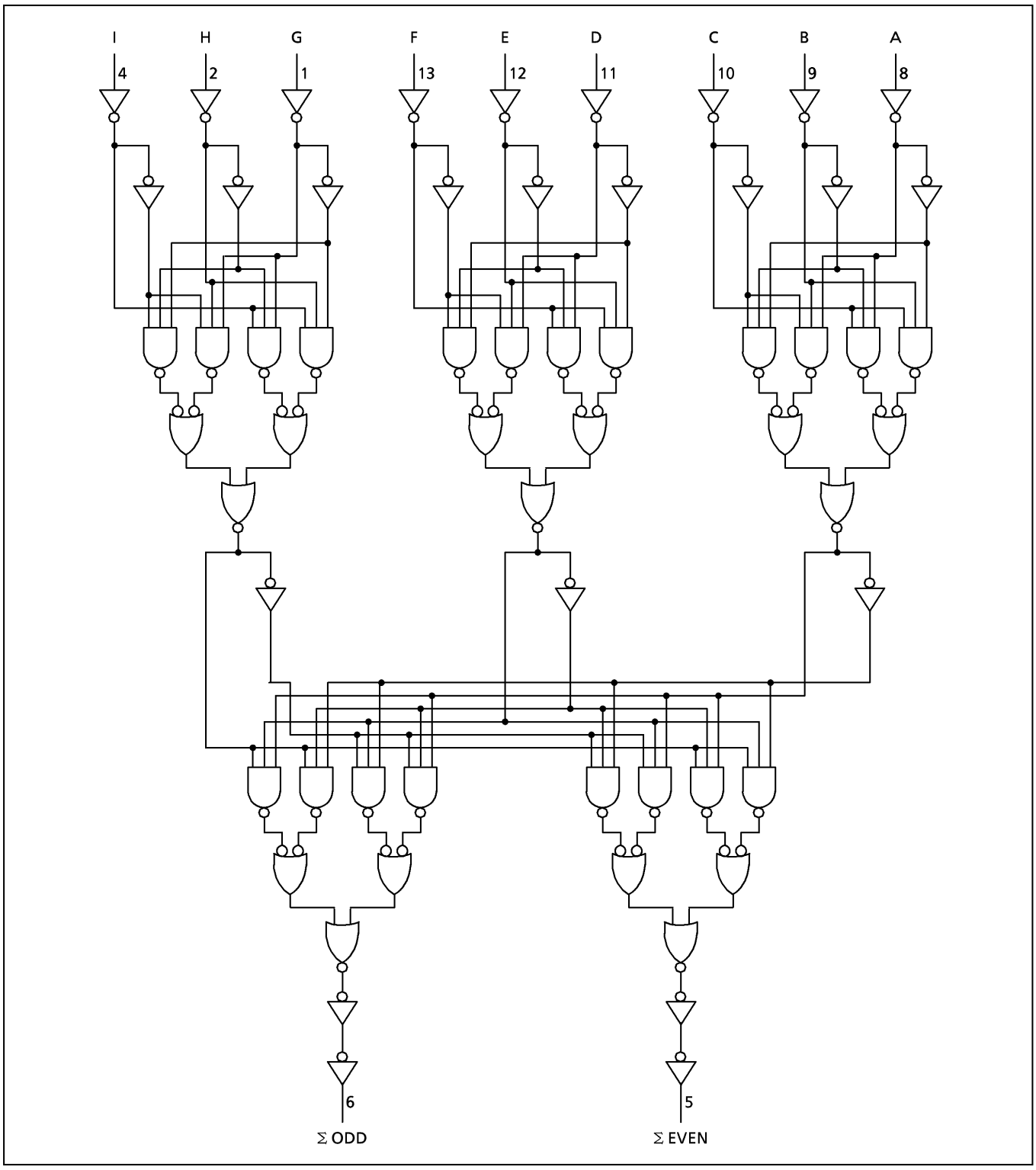
SYSTEM DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±100	mA
Power Dissipation	P_D	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	T_{stg}	−65~150	°C

*500mW in the range of Ta = −40°C~65°C. From Ta = 65°C to 85°C a derating factor of −10mW/°C should be applied up to 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5~5.5	V
Input Voltage	V_{IN}	0~V_{CC}	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	dt / dV	0~10	ns / V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C MIN.	Ta = 25°C TYP.	Ta = 25°C MAX.	Ta = −40~85°C MIN.	Ta = −40~85°C MAX.	UNIT
High - Level Input Voltage	V_{IH}			4.5 ~ 5.5	2.0	−	−	2.0	−	V
Low - Level Input Voltage	V_{IL}			4.5 ~ 5.5	−	−	0.8	−	0.8	V
High - Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50μA I_{OH} = −24mA I_{OH} = −75mA*	4.5 4.5 5.5	4.4 3.94 −	4.5 − −	− − −	4.4 3.80 3.85	− − −	V
Low - Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50μA I_{OL} = 24mA I_{OL} = 75mA*	4.5 4.5 5.5	− − −	0.0 − −	0.1 0.36 −	− − −	0.1 0.44 1.65	V
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	−	−	8.0	−	80.0	μA
	I_C	PER INPUT : V_{IN} = 3.4V OTHER INPUT : V_{CC} or GND		5.5	−	−	1.35	−	1.5	mA

* : This spec is indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

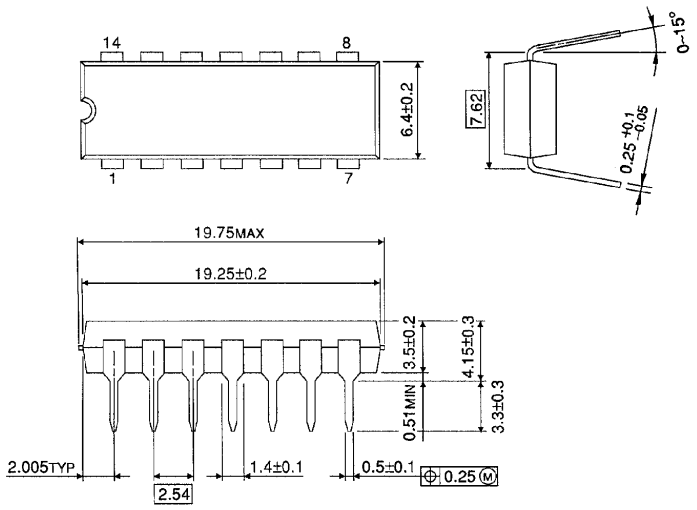
AC ELECTRICAL CHARACTERISTICS ($C_L = 50_pF$, $R_L = 500\Omega$, Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C			Ta = −40~85°C		UNIT
		V_{CC} (V)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time	t_{pLH} t_{pHL}	5.0 ± 0.5	−	9.9	14.5	1.0	16.5	ns
Input Capacitance	C_{IN}		−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD} (1)		−	78	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

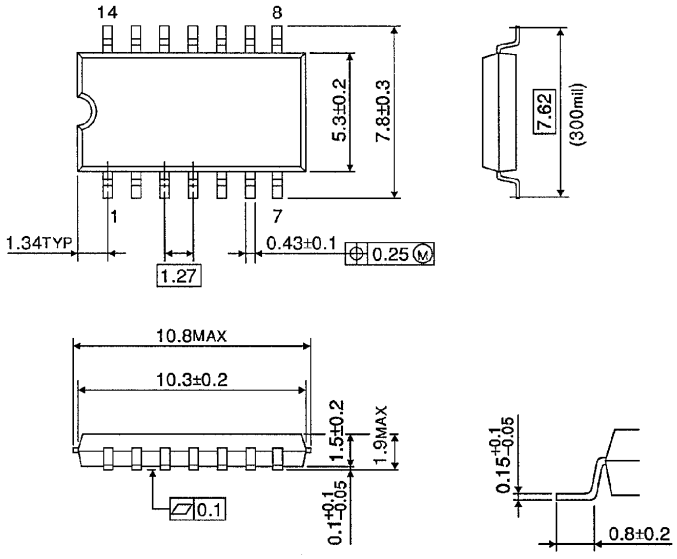
$$I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

DIP 14PIN OUTLINE DRAWING (DIP14-P-300-2.54) Unit in mm



Weight : 0.96g (Typ.)

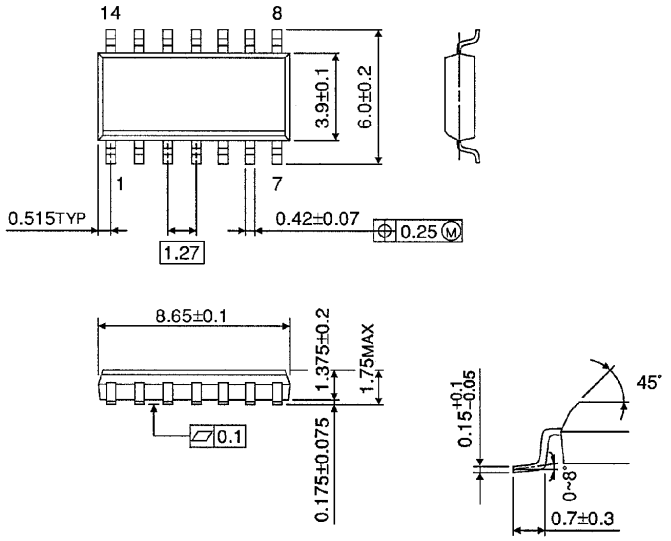
SOP 14PIN (200mil BODY) OUTLINE DRAWING (SOP14-P-300-1.27) Unit in mm



Weight : 0.18g (Typ.)

SOP 14PIN (150mil BODY) OUTLINE DRAWING (SOL14-P-150 -1.27) Unit in mm

(Note) This package is not available in Japan.



Weight : 0.12g (Typ.)