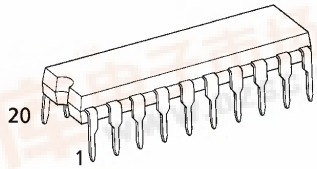
TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74ACT299P, TC74ACT299F, TC74ACT299FW

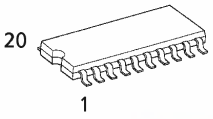
8 – BIT PIPO SHIFT REGISTER WITH ASYNCHRONOUS CLEAR

(Note) The JEDEC SOP (FW) is not available in Japan.

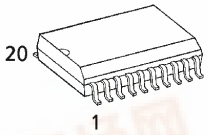
The TC74ACT299 is an advanced high speed CMOS 8-BIT PIPO SHIFT REGISTER fabricated with silicon gate and double-layer metal wiring C^2MOS technology.
It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.
This device may be used as a level converter for interfacing TLL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.
It has a four modes (HOLD, SHIFT LEFT, SHIFT RIGHT and LOAD DATA) controlled by the two selection inputs (S0, S1).
When one or both enable ($\overline{G1}$, $\overline{G2}$) are high, the eight I/O outputs are forced to the high-impedance state; however, sequential operation or clearing of the register is not affected.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.



P (DIP20-P-300-2.54A)
Weight : 1.30g (Typ.)



F (SOP20-P-300-1.27)
Weight : 0.22g (Typ.)

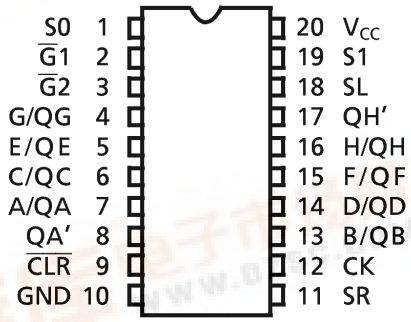


FW (SOL20-P-300-1.27)
Weight : 0.46g (Typ.)

FEATURES :

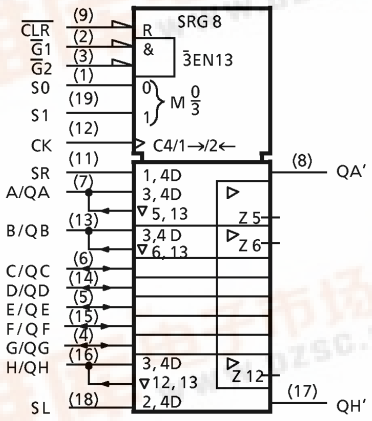
- High Speed ····· f_{MAX} = 130MHz (typ.) at V_{CC} = 5V
- Low Power Dissipation ····· I_{CC} = 8μA(Max.) at Ta = 25°C
- Compaible with TTL outputs ···· V_{IL} = 0.8V(Max.) V_{IH} = 2.0V(Min.)
- Symmetrical Output Impedance··· $|I_{OH}| = I_{OL}$ = 24mA (Min.) Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ····· $t_{pLH} \simeq t_{pHL}$
- Pin and Function Compatible with 74F299

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



APPLICATION NOTES

1) Do not apply a signal to any bus terminal when it is in the output mode. Damage may result.
2) All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or pull down resistors.

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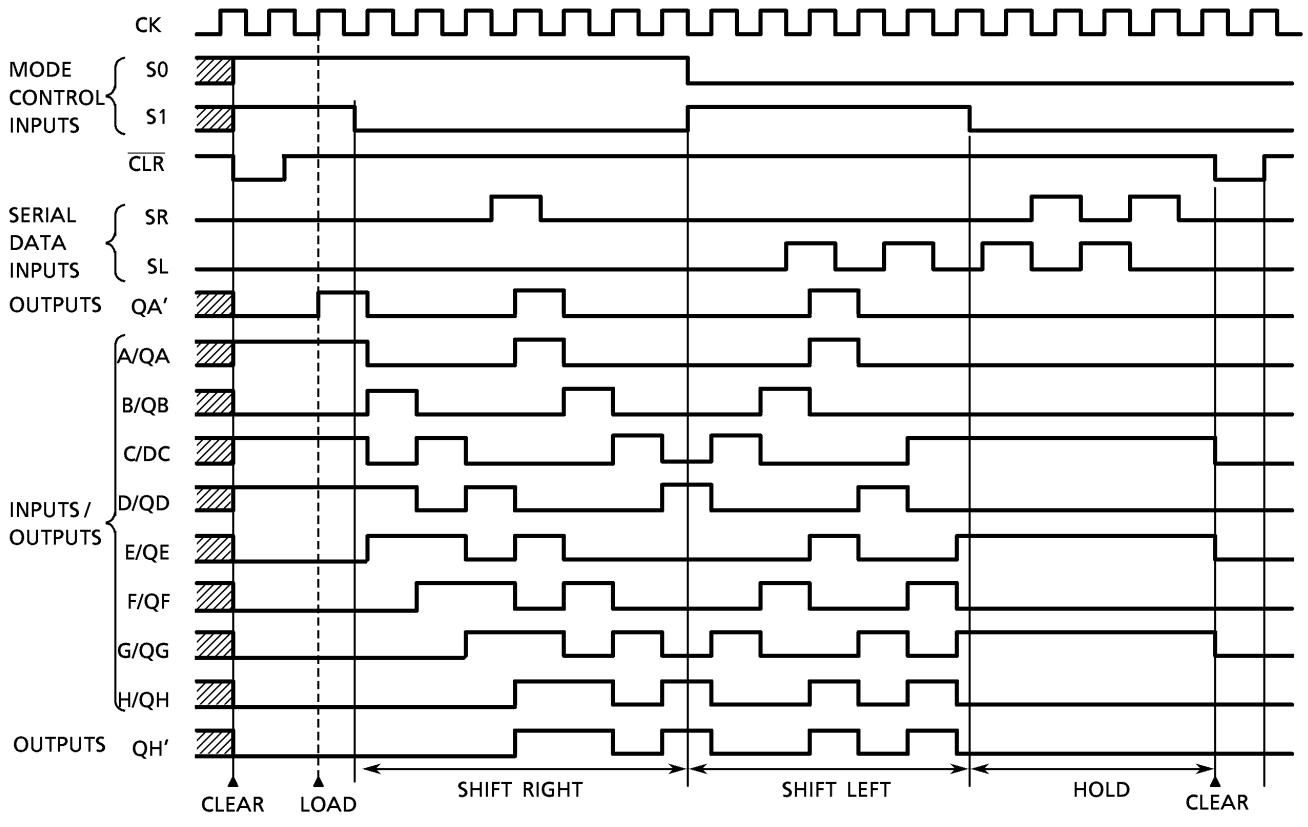
TRUTH TABLE

MODE	INPUTS								INPUTS/ OUTPUTS		OUTPUTS	
	$\overline{CLR}$	FUNCTION SELECT		OUTPUT CONTROL		CK	SERIAL		A/QA	H/QH	QA'	QH'
		S1	S0	$\overline{G}1$*	$\overline{G}2$*		SL	SR				
Z	L	H	H	X	X	X	X	X	Z	Z	L	L
CLEAR	L	L	X	L	L	X	X	X	L	L	L	L
	L	X	L	L	L	X	X	X	L	L	L	L
HOLD	H	L	L	L	L	X	X	X	QA0	QH0	QA0	QH0
SHIFT RIGHT	H	L	H	L	L	↑	X	H	H	QGn	H	QGn
	H	L	H	L	L	↑	X	L	L	QGn	L	QGn
SHIFT LEFT	H	H	L	L	L	↑	H	X	QBn	H	QBn	H
	H	H	L	L	L	↑	L	X	QBn	L	QBn	L
LOAD	H	H	H	X	X	↑	X	X	a	h	a	h

* When one or both output controls are high, the eight input/output terminals are in the high-impedance state; however sequential or clearing of the register is not affected.

Z : High Impedance
Qn0 : The level of Qn before the indicated steady – state input conditions were established.
Qnn : The level of Qn before the most recent active transition indicated by ↓ or ↑.
a, h : The level of the steady – state inputs A, H, respectively.
X : Don't Care.

TIMING CHART



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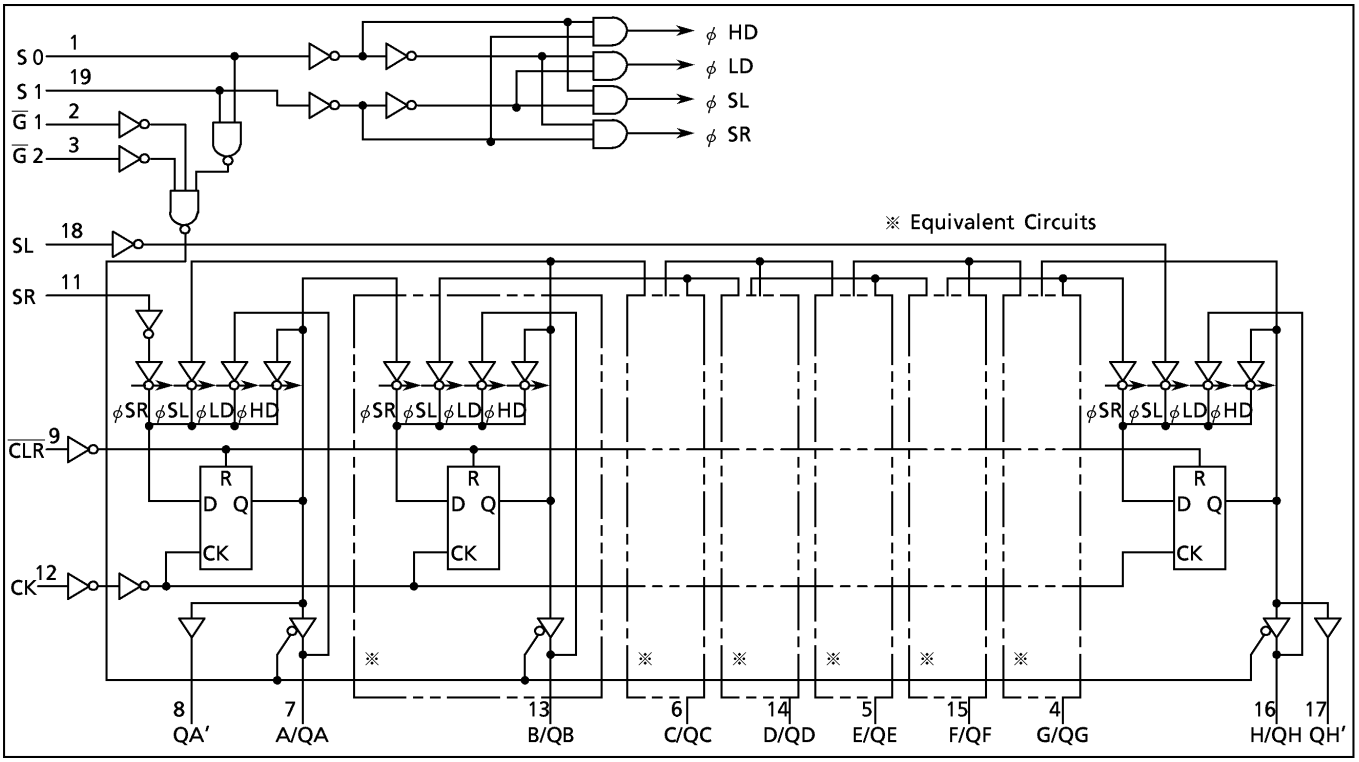
SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±250	mA
Power Dissipation	P_D	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	T_{stg}	−65~150	°C

*500mW in the range of Ta = −40°C~65°C. From Ta = 65°C to 85°C a derating factor of −10mW/°C should be applied up to 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5~5.5	V
Input Voltage	V_{IN}	0~V_{CC}	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	dt / dV	0~10	ns / V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C MIN.	Ta = 25°C TYP.	Ta = 25°C MAX.	Ta = −40~85°C MIN.	Ta = −40~85°C MAX.	UNIT
High - Level Input Voltage	V_{IH}			4.5 ~ 5.5	2.0	—	—	2.0	—	V
Low - Level Input Voltage	V_{IL}			4.5 ~ 5.5	—	—	0.8	—	0.8	V
High - Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50μA	4.5	4.4	4.5	—	4.4	—	V
			I_{OH} = −24mA	4.5	3.94	—	—	3.80	—	
			I_{OH} = −75mA*	5.5	—	—	—	3.85	—	
Low - Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50μA	4.5	—	0.0	0.1	—	0.1	V
			I_{OL} = 24mA	4.5	—	—	0.36	—	0.44	
			I_{OL} = 75mA*	5.5	—	—	—	—	1.65	
3 - State Output Off - State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		5.5	—	—	±0.5	—	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		5.5	—	—	±0.1	—	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	—	8.0	—	80.0	
	I_C	PER INPUT: V_{IN} = 3.4V OTHER INPUT: V_{CC} or GND		5.5	—	—	1.35	—	1.5	mA

* : This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

TIMING REQUIREMENTS (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	Ta = 25°C LIMIT	Ta = −40~85°C LIMIT	UNIT
Minimum Pulse Width (CK)	$t_{W(L)}$ $t_{W(H)}$		5.0 ± 0.5	5.0	5.0	ns
Minimum Pulse Width ($\overline{CLR}$)	$t_{W(L)}$		5.0 ± 0.5	5.0	5.0	
Minimum Set - up Time (SL, SR, A~H)	t_s		5.0 ± 0.5	3.5	3.5	
Minimum Set - up Time (S0, S1)	t_s		5.0 ± 0.5	6.0	6.5	
Minimum Hold Time (SL, SR, A~H)	t_h		5.0 ± 0.5	2.0	2.0	
Minimum Hold Time (S0, S1)	t_h		5.0 ± 0.5	0.0	0.0	
Minimum Removal Time ($\overline{CLR}$)	t_{rem}		5.0 ± 0.5	2.0	2.0	

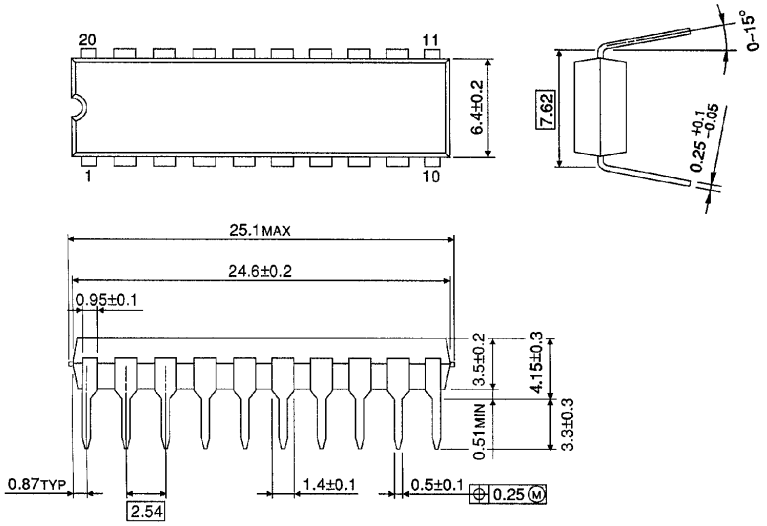
AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, R_L = 500Ω, $t_r = t_f$ = 3ns)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C			Ta = −40~85°C		UNIT
		V_{CC} (V)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (CK−QA′ , QH′)	t_{pLH} t_{pHL}	5.0 ± 0.5	−	7.2	10.5	1.0	12.0	ns
Propagation Delay Time ($\overline{CLR}$−QA′ , QH′)	t_{pHL}	5.0 ± 0.5	−	6.0	10.0	1.0	11.5	
Propagation Delay Time (CK−QA~QH)	t_{pLH} t_{pHL}	5.0 ± 0.5	−	7.4	11.4	1.0	13.0	
Propagation Delay Time ($\overline{CLR}$−QA~QH)	t_{pHL}	5.0 ± 0.5	−	6.3	10.5	1.0	12.0	
Output Enable Time	t_{pZL} t_{pZH}	5.0 ± 0.5	−	7.4	11.4	1.0	13.0	
Output Disable Time	t_{pLZ} t_{pHZ}	5.0 ± 0.5	−	7.2	9.6	1.0	11.0	
Maximum Clock Frequency	f_{MAX}	5.0 ± 0.5	80	120	−	80	−	MHz
Input Capacitance	C_{IN}		−	5	10	−	10	pF
Bus Input Capacitance	$C_{I/O}$		−	13	−	−	−	
Power Dissipation Capacitance	C_{PD} (1)		−	160	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

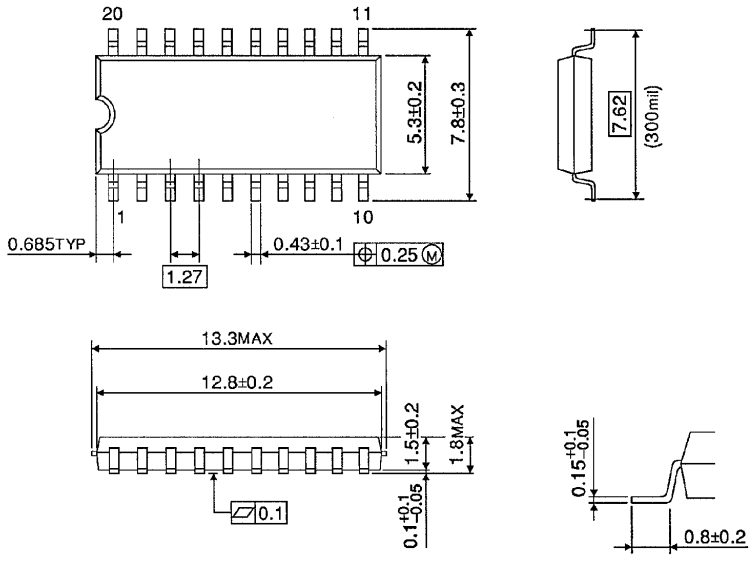
$$I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

DIP 20PIN OUTLINE DRAWING (DIP20-P-300-2.54A) Unit in mm



Weight : 1.30g (Typ.)

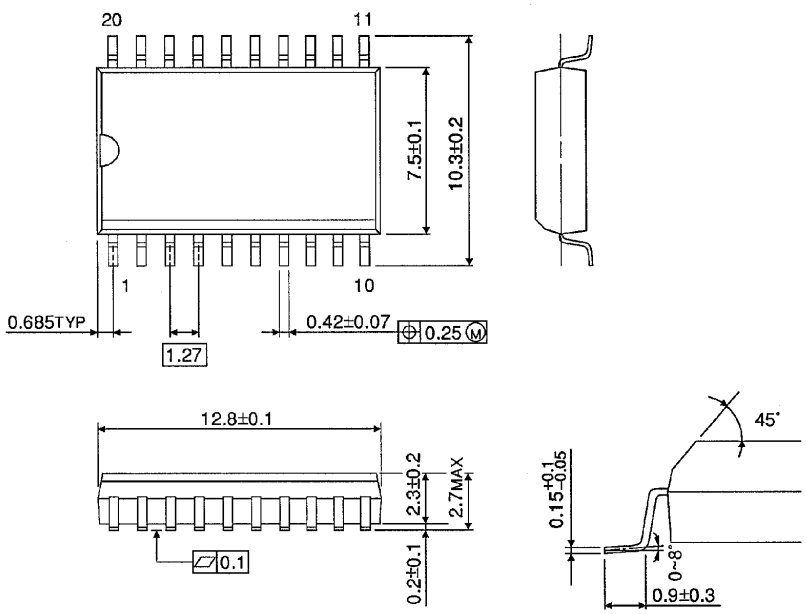
SOP 20PIN (200mil BODY) OUTLINE DRAWING (SOP20-P-300-1.27) Unit in mm



Weight : 0.22g (Typ.)

SOP 20PIN (300mil BODY) OUTLINE DRAWING (SOL20-P-300-1.27) Unit in mm

(Note) This package is not available in Japan.



Weight : 0.46g (Typ.)