

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74HC132AP, TC74HC132AF, TC74HC132AFN

QUAD 2-INPUT SCHMITT NAND GATE

The TC74HC132A is a high speed CMOS 2-INPUT NAND SCHMITT TRIGGER GATE fabricated with silicon gate C²MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

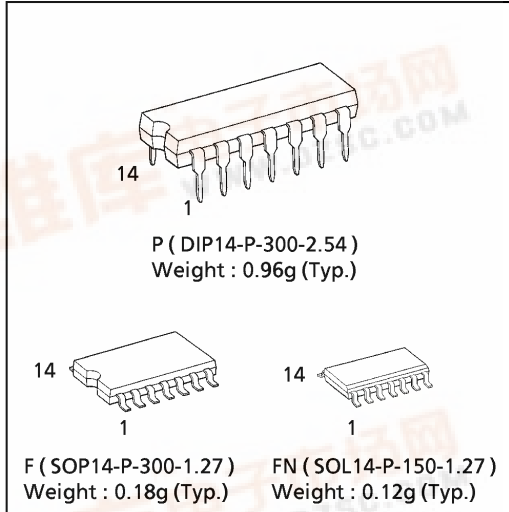
Pin configuration and function are the same as the TC74HC00A but the inputs have 25% V_{CC} hysteresis and with its schmitt trigger inputs, the TC74HC132A can be used as a line receiver for slow input signals.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

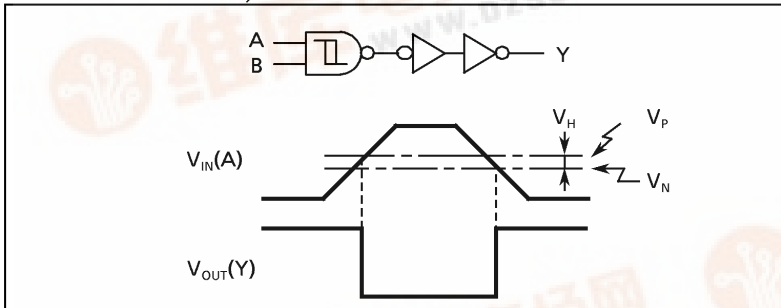
FEATURES:

- High Speed..... t_{pd} = 11ns(typ.) at V_{CC} = 5V
- Low Power Dissipation..... I_{CC} = 1μA(Max.) at Ta = 25°C
- High Noise Immunity..... V_H = 1.1V at V_{CC} = 5V
- Output Drive Capability..... 10 LSTTL Loads
- Symmetrical Output Impedance... |I_{OH}| = I_{OL} = 4mA(Min.)
- Balanced Propagation Delays..... t_{pLH} ≈ t_{pHL}
- Wide Operating Voltage Range... V_{CC} (opr.) = 2V~6V
- Pin and Function Compatible with 74LS132

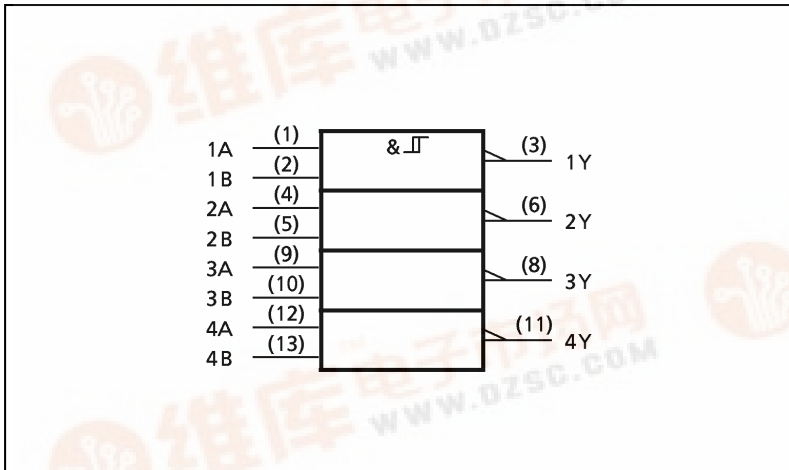
(Note) The JEDEC SOP (FN) is not available in Japan.



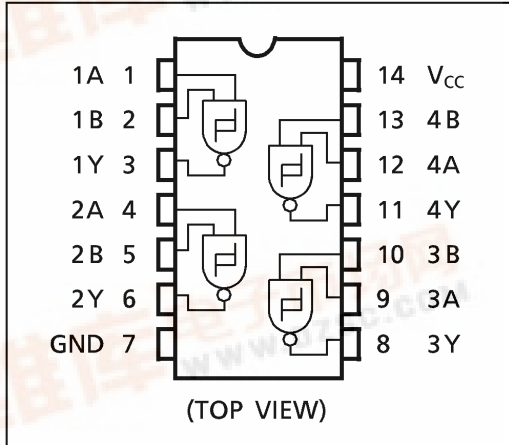
SYSTEM DIAGRAM, WAVEFORM



IEC LOGIC SYMBOL



PIN ASSIGNMENT



TRUTH TABLE

A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

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● TOSHIBA is continually working to improve the quality and the reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to observe standards of safety, and to avoid situations in which a malfunction or failure of a TOSHIBA product could cause loss of human life, bodily injury or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent products specifications. Also, please keep in mind the precautions and conditions set forth in the TOSHIBA Semiconductor Reliability Handbook.



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5~7	V
DC Input Voltage	V_{IN}	-0.5~ $V_{CC} + 0.5$	V
DC Output Voltage	V_{OUT}	-0.5~ $V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC} / Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	T_{stg}	-65~150	°C

*500mW in the range of $T_a = -40^{\circ}C \sim 65^{\circ}C$. From $T_a = 65^{\circ}C$ to $85^{\circ}C$ a derating factor of $-10mW/^{\circ}C$ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2~6	V
Input Voltage	V_{IN}	0~ V_{CC}	V
Output Voltage	V_{OUT}	0~ V_{CC}	V
Operating Temperature	T_{opr}	-40~85	°C

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	$T_a = 25^{\circ}C$			$T_a = -40 \sim 85^{\circ}C$		UNIT	
				MIN.	TYP.	MAX.	MIN.	MAX.		
Positive Threshold Voltage	V_P		2.0	1.0	1.25	1.50	1.0	1.50	V	
			4.5	2.3	2.70	3.15	2.3	3.15		
			6.0	3.0	3.50	4.20	3.0	4.20		
Negative Threshold Voltage	V_N		2.0	0.30	0.65	0.9	0.30	0.9	V	
			4.5	1.13	1.60	2.0	1.13	2.0		
			6.0	1.50	2.30	2.6	1.50	2.6		
Hysteresis Output Voltage	V_H		2.0	0.3	0.6	1.0	0.3	1.0	V	
			4.5	0.6	1.1	1.4	0.6	1.4		
			6.0	0.8	1.2	1.7	0.8	1.7		
High - Level Output Voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -20\mu A$	2.0	1.9	2.0	—	1.9	—	V
				4.5	4.4	4.5	—	4.4	—	
				6.0	5.9	6.0	—	5.9	—	
Low - Level Output Voltage	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 20\mu A$	2.0	—	0.0	0.1	—	0.1	V
				4.5	—	0.0	0.1	—	0.1	
				6.0	—	0.0	0.1	—	0.1	
Low - Level Output Voltage	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 4\text{ mA}$ $I_{OL} = 5.2\text{ mA}$	4.5	—	0.17	0.26	—	0.33	V
				6.0	—	0.18	0.26	—	0.33	
				6.0	—	0.18	0.26	—	0.33	
Input Leakage Current	I_{IN}	$V_{IN} = V_{CC}$ or GND	6.0	—	—	±0.1	—	±1.0	μA	
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC}$ or GND	6.0	—	—	1.0	—	10.0		

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AC ELECTRICAL CHARACTERISTICS ($C_L = 15\text{pF}$, $V_{CC} = 5\text{V}$, $T_a = 25^\circ\text{C}$, Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH}		—	4	8	ns
	t_{THL}					
Propagation Delay Time	t_{pLH}		—	11	18	ns
	t_{pHL}					

AC ELECTRICAL CHARACTERISTICS ($C_L = 50\text{pF}$, Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	$T_a = 25^\circ\text{C}$			$T_a = -40\sim 85^\circ\text{C}$		UNIT	
			$V_{CC}(\text{V})$	MIN.	TYP.	MAX.	MIN.		MAX.
Output Transition Time	t_{TLH}		2.0	—	30	75	—	95	ns
	t_{THL}		4.5	—	8	15	—	19	
			6.0	—	7	13	—	16	
Propagation Delay Time	t_{pLH}		2.0	—	42	110	—	140	ns
	t_{pHL}		4.5	—	14	22	—	28	
			6.0	—	12	19	—	24	
Input Capacitance	C_{IN}			—	5	10	—	10	pF
Power Dissipation Capacitance	$C_{PD} (1)$			—	29	—	—	—	

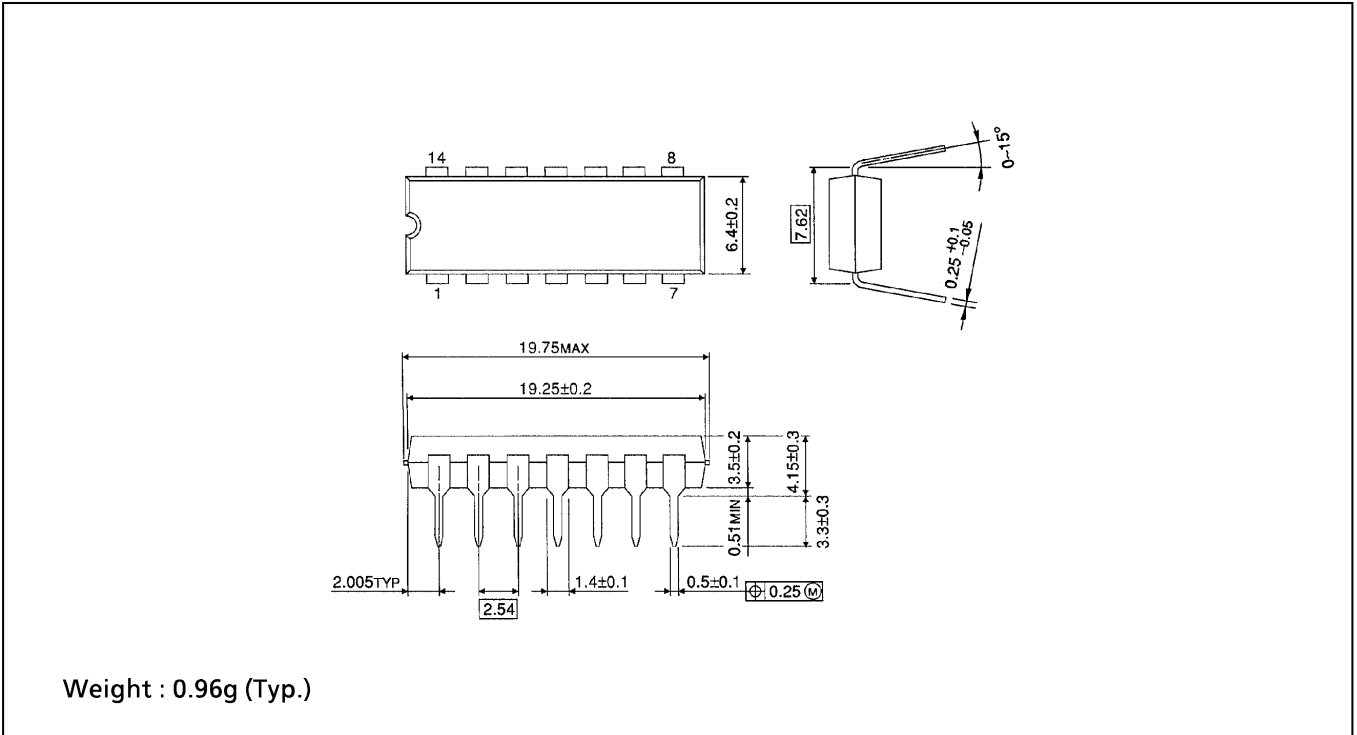
Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per Gate)}$$

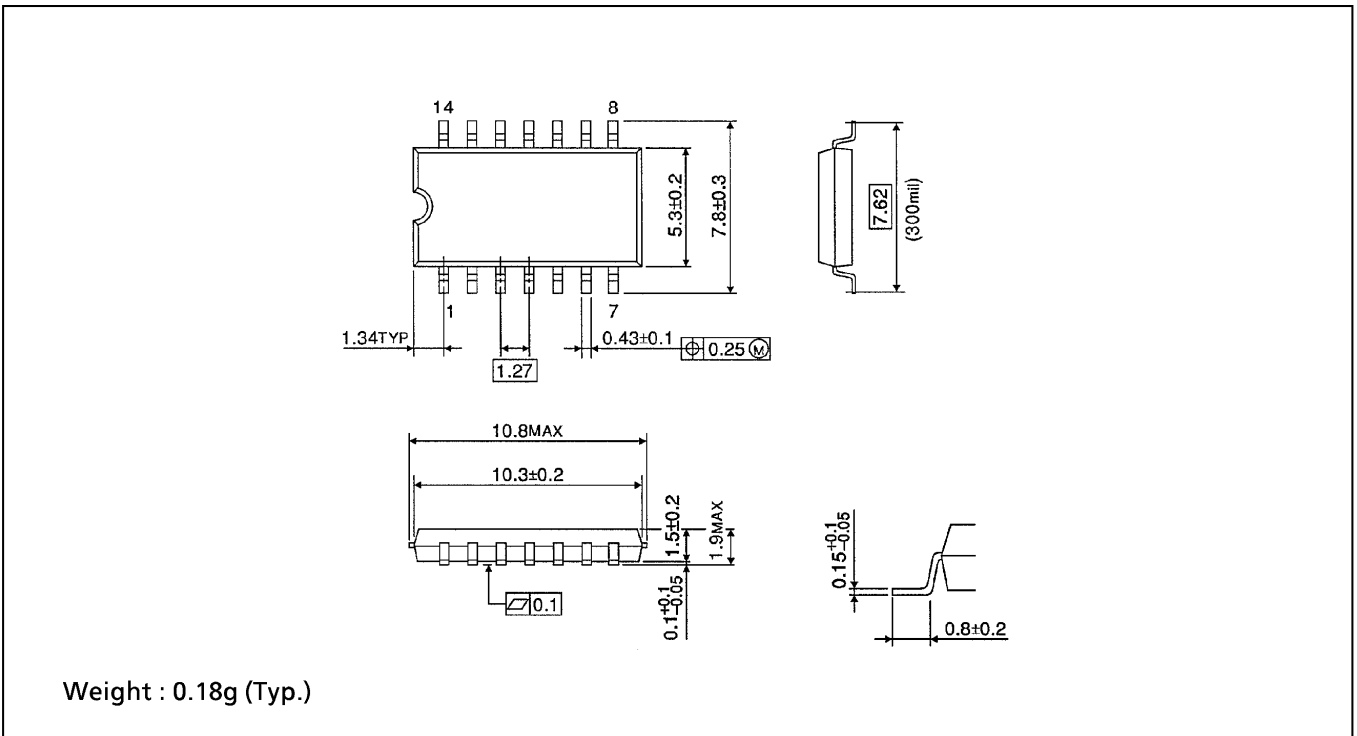
DIP 14PIN OUTLINE DRAWING (DIP14-P-300-2.54)

Unit in mm



SOP 14PIN (200mil BODY) OUTLINE DRAWING (SOP14-P-300-1.27)

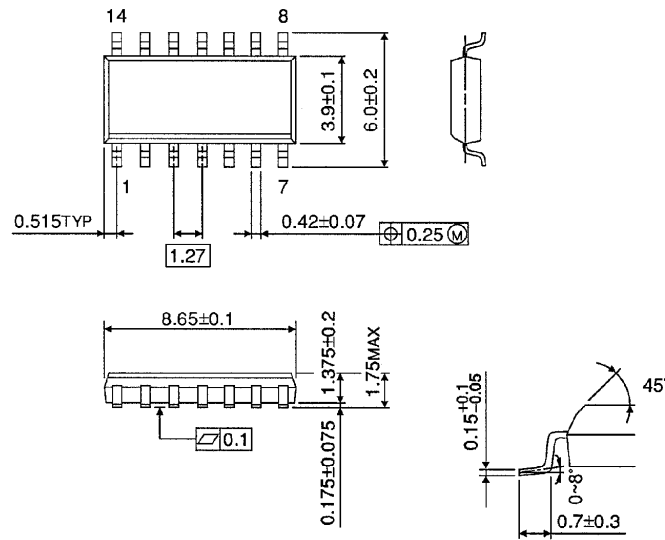
Unit in mm



SOP 14PIN (150mil BODY) OUTLINE DRAWING (SOL14-P-150 -1.27)

Unit in mm

(Note) This package is not available in Japan.



Weight : 0.12g (Typ.)