

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74HC175AP, TC74HC175AF, TC74HC175AFN

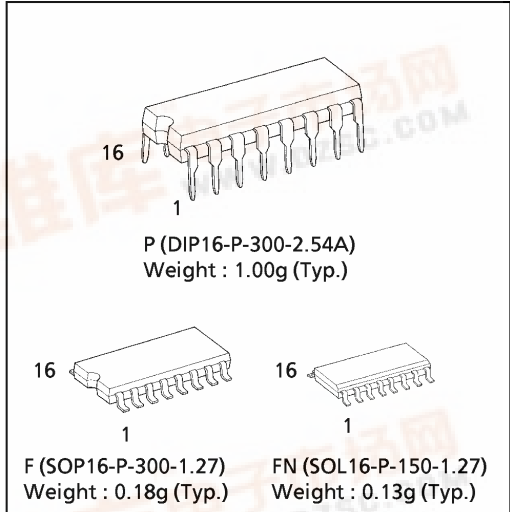
QUAD D-TYPE FLIP FLOP WITH CLEAR

(Note) The JEDEC SOP (FN) is not available in Japan.

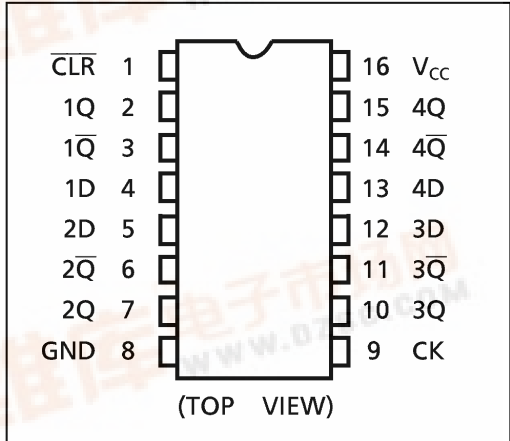
The TC74HC175A is a high speed CMOS D-TYPE FLIP FLOP fabricated with silicon gate C²MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. Information signals applied to D inputs are transferred to the Q and \bar{Q} outputs on the positive going edge of the clock pulse. When the $\overline{\text{CLR}}$ input is held low, the Q outputs are at the low logic level and the \bar{Q} outputs are at the high logic level independent of the other inputs. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES :

- High Speed..... $f_{\text{MAX}} = 63\text{MHz}(\text{typ.})$
at $V_{\text{CC}} = 5\text{V}$
- Low Power Dissipation..... $I_{\text{CC}} = 4\mu\text{A}(\text{Max.})$ at $T_a = 25^\circ\text{C}$
- High Noise Immunity..... $V_{\text{NIH}} = V_{\text{NIL}} = 28\% V_{\text{CC}} (\text{Min.})$
- Symmetrical Output Impedance... $|I_{\text{OH}}| = I_{\text{OL}} = 4\text{mA}(\text{Min.})$
- Balanced Propagation Delays... $t_{\text{PLH}} \approx t_{\text{PHL}}$
- Wide Operating Voltage Range... $V_{\text{CC}} (\text{opr.}) = 2\text{V} \sim 6\text{V}$
- Pin and Function Compatible with 74LS175



PIN ASSIGNMENT

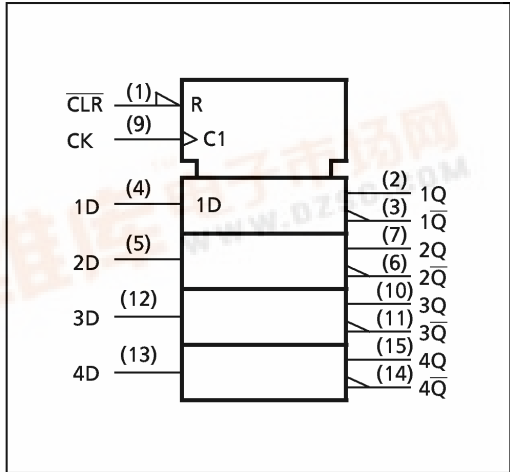


TRUTH TABLE

INPUTS			OUTPUTS		FUNCTION
$\overline{\text{CLR}}$	D	CK	Q	\bar{Q}	
L	X	X	L	H	Clear
H	L		L	H	—
H	H		H	L	—
H	X		Q_n	\bar{Q}_n	No change

X : Don't Care

IEC LOGIC SYMBOL

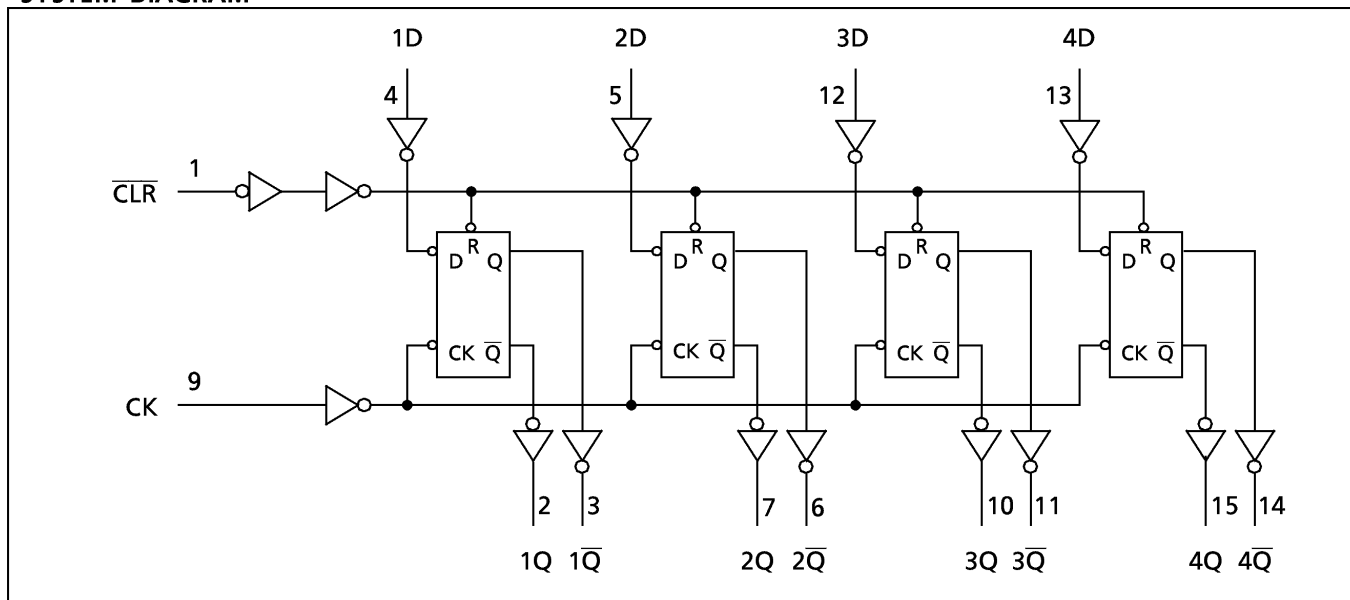


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SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5~7	V
DC Input Voltage	V_{IN}	-0.5~ $V_{CC} + 0.5$	V
DC Output Voltage	V_{OUT}	-0.5~ $V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC} /Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	T_{stg}	-65~150	°C

*500mW in the range of $T_a = -40^{\circ}C \sim 65^{\circ}C$. From $T_a = 65^{\circ}C$ to $85^{\circ}C$ a derating factor of $-10mW/^{\circ}C$ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2~6	V
Input Voltage	V_{IN}	0~ V_{CC}	V
Output Voltage	V_{OUT}	0~ V_{CC}	V
Operating Temperature	T_{opr}	-40~85	°C
Input Rise and Fall Time	t_r, t_f	0~1000 ($V_{CC} = 2.0V$) 0~500 ($V_{CC} = 4.5V$) 0~400 ($V_{CC} = 6.0V$)	ns

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DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V _{CC} (V)	Ta = 25°C			Ta = -40~85°C		UNIT	
				MIN.	TYP.	MAX.	MIN.	MAX.		
High - Level Input Voltage	V _{IH}		2.0	1.50	—	—	1.50	—	V	
			4.5	3.15	—	—	3.15	—		
			6.0	4.20	—	—	4.20	—		
Low - Level Input Voltage	V _{IL}		2.0	—	—	0.50	—	0.50	V	
			4.5	—	—	1.35	—	1.35		
			6.0	—	—	1.80	—	1.80		
High - Level Output Voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -20 μA	2.0	1.9	2.0	—	1.9	—	V
				4.5	4.4	4.5	—	4.4	—	
			I _{OH} = -4 mA I _{OH} = -5.2 mA	4.5	4.18	4.31	—	4.13	—	
				6.0	5.68	5.80	—	5.63	—	
Low - Level Output Voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 20 μA	2.0	—	0.0	0.1	—	0.1	V
				4.5	—	0.0	0.1	—	0.1	
			I _{OL} = 4 mA I _{OL} = 5.2 mA	4.5	—	0.17	0.26	—	0.33	
				6.0	—	0.18	0.26	—	0.33	
Input Leakage Current	I _{IN}	V _{IN} = V _{CC} or GND	6.0	—	—	±0.1	—	±1.0	μA	
Quiescent Supply Current	I _{CC}	V _{IN} = V _{CC} or GND	6.0	—	—	4.0	—	40.0		

TIMING REQUIREMENTS (Input t_r = t_f = 6ns)

PARAMETER	SYMBOL	TEST CONDITION	V _{CC} (V)	Ta = 25°C		Ta = -40~85°C		UNIT
				TYP.	LIMIT	LIMIT		
Minimum Pulse Width (CK)	t _{w(L)} t _{w(H)}		2.0	—	75	95	ns	
			4.5	—	15	19		
			6.0	—	13	16		
Minimum Pulse Width (CLR)	t _{w(L)}		2.0	—	75	95	ns	
			4.5	—	15	19		
			6.0	—	13	16		
Minimum Set-up Time	t _s		2.0	—	75	95	ns	
			4.5	—	15	19		
			6.0	—	13	16		
Minimum Hold Time	t _h		2.0	—	0	0	ns	
			4.5	—	0	0		
			6.0	—	0	0		
Minimum Removal Time	t _{rem}		2.0	—	75	95	ns	
			4.5	—	15	19		
			6.0	—	13	16		
Clock Frequency	f		2.0	—	6	5	MHz	
			4.5	—	31	25		
			6.0	—	36	29		

AC ELECTRICAL CHARACTERISTICS ($C_L = 15\text{pF}$, $V_{CC} = 5\text{V}$, $T_a = 25^\circ\text{C}$, Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		—	4	8	ns
Propagation Delay Time ($\overline{\text{CK}} - \text{Q}$, $\overline{\text{Q}}$)	t_{pLH} t_{pHL}		—	16	24	
Propagation Delay Time ($\overline{\text{CLR}} - \text{Q}$, $\overline{\text{Q}}$)	t_{pLH} t_{pHL}		—	13	21	
Maximum Clock Frequency	f_{MAX}		36	63	—	MHz

AC ELECTRICAL CHARACTERISTICS ($C_L = 50\text{pF}$, Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	$T_a = 25^\circ\text{C}$			$T_a = -40 \sim 85^\circ\text{C}$		UNIT
			V_{CC} (V)	MIN.	TYP.	MAX.	MIN.	
Output Transition Time	t_{TLH} t_{THL}		2.0	—	30	75	—	95
			4.5	—	8	15	—	19
			6.0	—	7	13	—	16
Propagation Delay Time ($\overline{\text{CK}} - \text{Q}$, $\overline{\text{Q}}$)	t_{pLH} t_{pHL}		2.0	—	70	140	—	175
			4.5	—	19	28	—	35
			6.0	—	16	24	—	30
Propagation Delay Time ($\overline{\text{CLR}} - \text{Q}$, $\overline{\text{Q}}$)	t_{pLH} t_{pHL}		2.0	—	50	125	—	160
			4.5	—	16	25	—	32
			6.0	—	12	22	—	27
Maximum Clock Frequency	f_{MAX}		2.0	6	14	—	5	—
			4.5	31	53	—	25	—
			6.0	36	63	—	29	—
Input Capacitance	C_{IN}		—	5	10	—	10	pF
Power Dissipation Capacitance	C_{PD} (1)		—	53	—	—	—	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

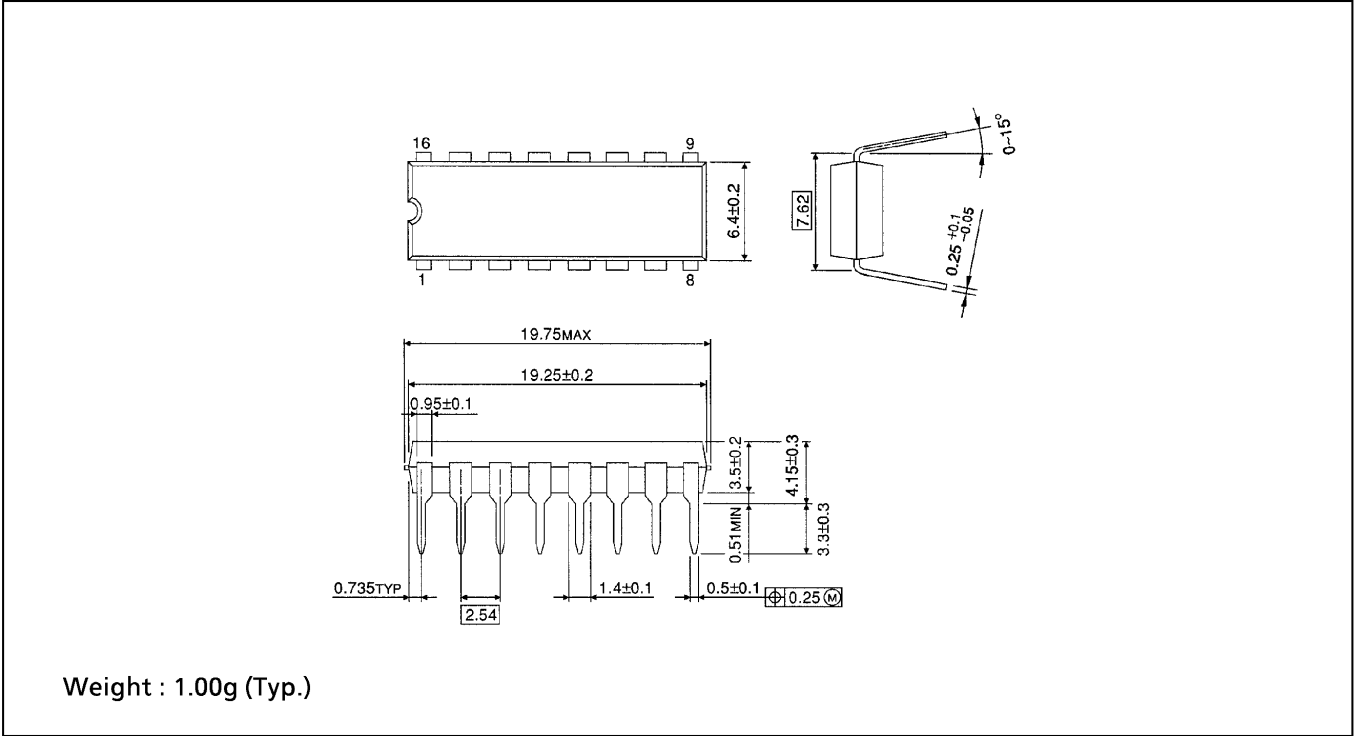
$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per F / F)}$$

And the total C_{PD} when n pcs. of Flip Flop operate can be gained by the following equation :

$$CPD(\text{total}) = 32 + 21 \cdot n$$

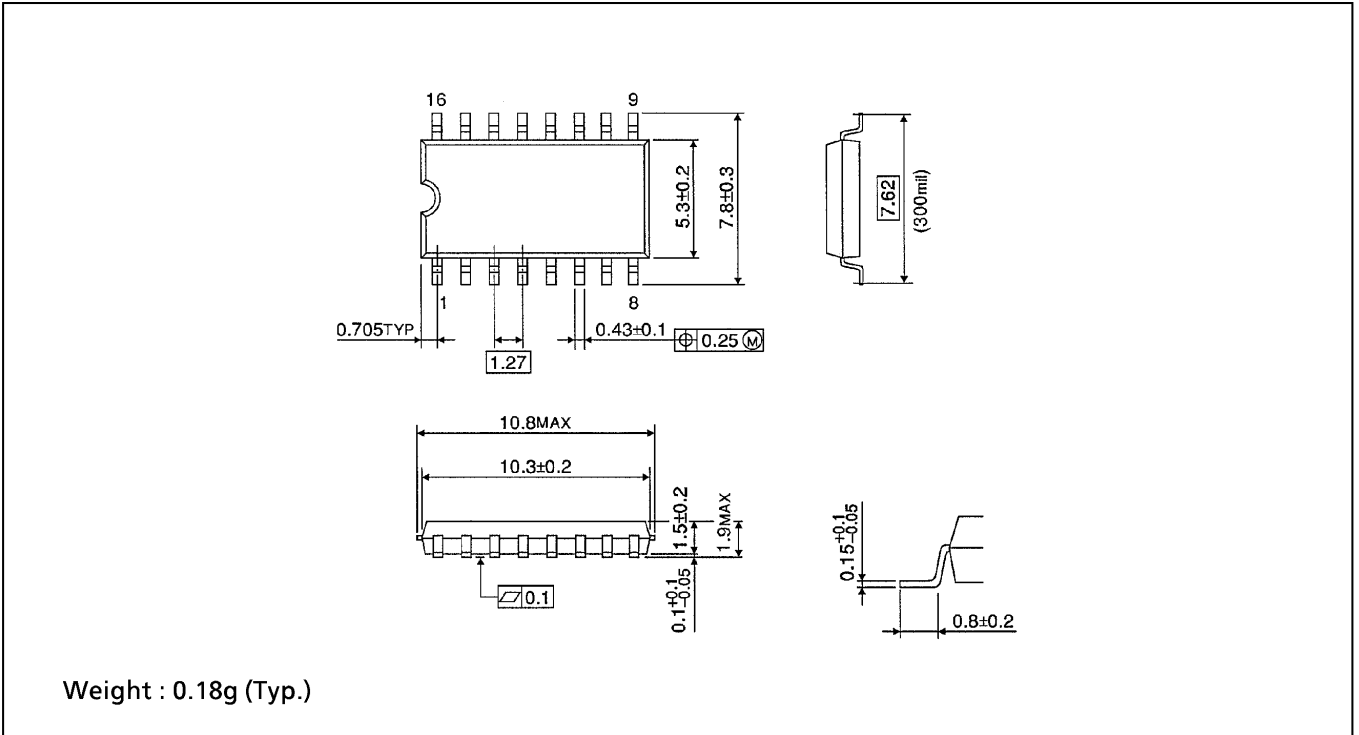
DIP 16PIN OUTLINE DRAWING (DIP16-P-300-2.54A)

Unit in mm



SOP 16PIN (200mil BODY) OUTLINE DRAWING (SOP16-P-300-1.27)

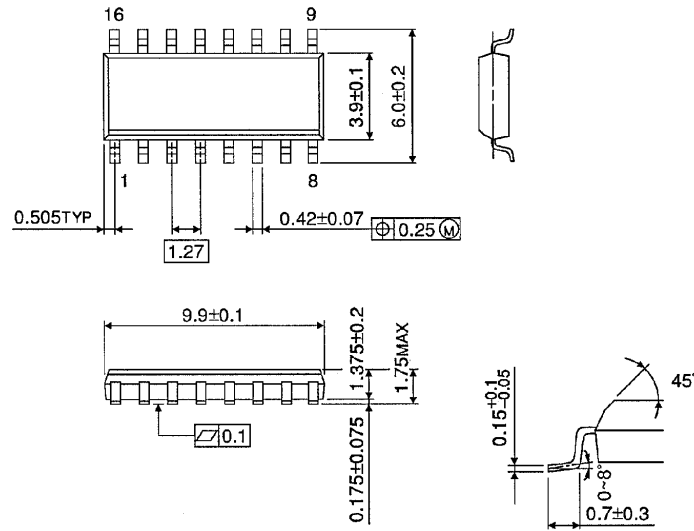
Unit in mm



SOP 16PIN (150mil BODY) OUTLINE DRAWING (SOL16-P-150 -1.27)

Unit in mm

(Note) This package is not available in Japan.



Weight : 0.13g (Typ.)