

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

**TC74HC365AP, TC74HC365AF**  
**TC74HC366AP, TC74HC366AF**

HEX BUS BUFFER  
 TC74HC365AP/AF NON - INVERTED (3-STATE)  
 TC74HC366AP/AF INVERTED (3-STATE)

The TC74HC365A and TC74HC366A are high speed CMOS 3 - STATE BUFFERs fabricated with silicon gate C<sup>2</sup>MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. The TC74HC366A is an inverting type, while the TC74HC365A is non - inverting.

All six buffers are controlled by the combination of two enable inputs ( $\bar{G}1$  and  $\bar{G}2$ ); the outputs of these buffers are enabled only when both  $\bar{G}1$  and  $\bar{G}2$  inputs held low, and at the other combinations, these outputs are disabled to the high impedance state.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

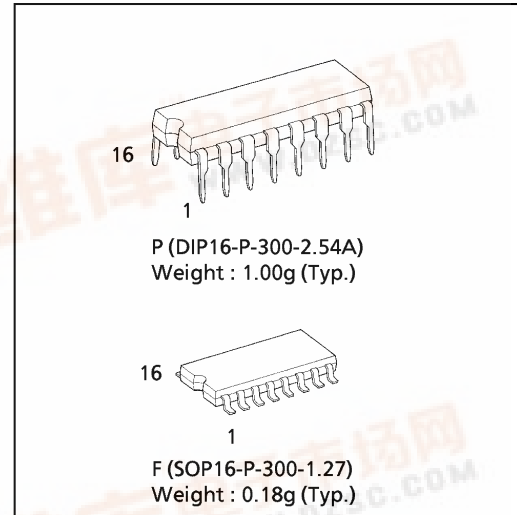
**FEATURES :**

- High Speed..... $t_{pd} = 9ns$ (typ.) at  $V_{CC} = 5V$
- Low Power Dissipation..... $I_{CC} = 4\mu A$ (Max.)at  $T_a = 25^\circ C$
- High Noise Immunity..... $V_{NIH} = V_{NIL} = 28\% V_{CC}$  (Min.)
- Output Drive Capability..... 15 LSTTL Loads
- Symmetrical Output Impedance... $|I_{OH}| = |I_{OL}| = 6mA$ (Min.)
- Balanced Propagation Delays..... $t_{pLH} \approx t_{pHL}$
- Wide Operating Voltage Range... $V_{CC}$  (opr.) = 2V~6V
- Open Drain Structure
- Pin and Function Compatible with 74LS365/366

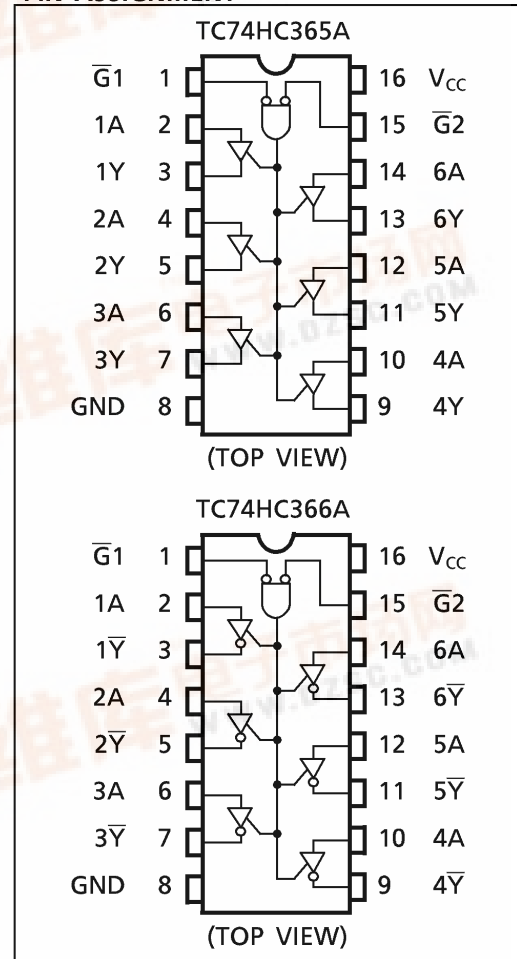
**TRUTH TABLE**

INPUTS			OUTPUTS	
$\bar{G}1$	$\bar{G}2$	An	Yn(365A)	$\bar{Y}n(366A)$
L	L	L	L	H
L	L	H	H	L
H	X	X	Z	Z
X	H	X	Z	Z

X : Don't Care, Z : High Impedance



**PIN ASSIGNMENT**

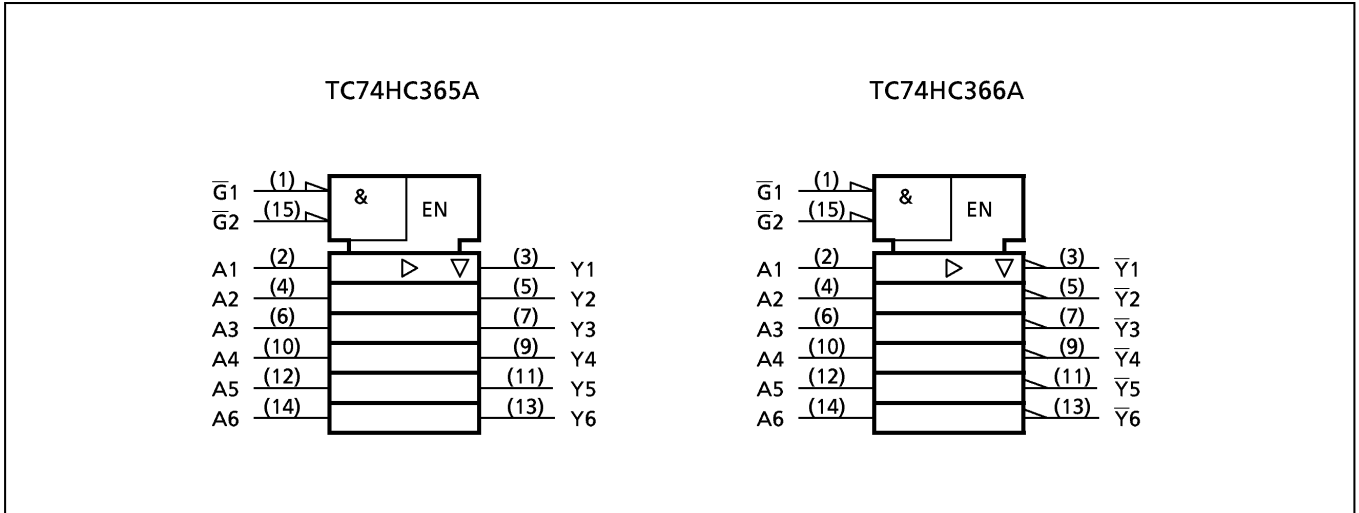


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**IEC LOGIC SYMBOL**



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**ABSOLUTE MAXIMUM RATINGS**

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	$V_{CC}$	-0.5~7	V
DC Input Voltage	$V_{IN}$	-0.5~ $V_{CC}+0.5$	V
DC Output Voltage	$V_{OUT}$	-0.5~ $V_{CC}+0.5$	V
Input Diode Current	$I_{IK}$	±20	mA
Output Diode Current	$I_{OK}$	±20	mA
DC Output Current	$I_{OUT}$	±35	mA
DC $V_{CC}$ /Ground Current	$I_{CC}$	±75	mA
Power Dissipation	$P_D$	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	$T_{stg}$	-65~150	°C

\*500mW in the range of  $T_a = -40^{\circ}\text{C} \sim 65^{\circ}\text{C}$ . From  $T_a = 65^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  a derating factor of  $-10\text{mW}/^{\circ}\text{C}$  shall be applied until 300mW.

**RECOMMENDED OPERATING CONDITIONS**

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	$V_{CC}$	2~6	V
Input Voltage	$V_{IN}$	0~ $V_{CC}$	V
Output Voltage	$V_{OUT}$	0~ $V_{CC}$	V
Operating Temperature	$T_{opr}$	-40~85	°C
Input Rise and Fall Time	$t_r, t_f$	0~1000 ( $V_{CC} = 2.0\text{V}$ ) 0~500 ( $V_{CC} = 4.5\text{V}$ ) 0~400 ( $V_{CC} = 6.0\text{V}$ )	ns

**DC ELECTRICAL CHARACTERISTICS**

PARAMETER	SYMBOL	TEST CONDITION	$V_{CC}$ (V)	$T_a = 25^{\circ}\text{C}$			$T_a = -40 \sim 85^{\circ}\text{C}$		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	$V_{IH}$		2.0 4.5 6.0	1.50 3.15 4.20	— — —	— — —	1.50 3.15 4.20	— — —	V
Low - Level Input Voltage	$V_{IL}$		2.0 4.5 6.0	— — —	— — —	0.50 1.35 1.80	— — —	0.50 1.35 1.80	V
High - Level Output Voltage	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$ $I_{OH} = -20\mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	— — —	1.9 4.4 5.9	— — —	V
			4.5 6.0	4.18 5.68	4.31 5.80	— —	4.13 5.63	— —	
Low - Level Output Voltage	$V_{OL}$	$V_{IN} = V_{IH}$ or $V_{IL}$ $I_{OL} = 20\mu\text{A}$	2.0 4.5 6.0	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	0.1 0.1 0.1	V
			4.5 6.0	— —	0.17 0.18	0.26 0.26	— —	0.33 0.33	
3 - State Output Off - State Current	$I_{OZ}$	$V_{IN} = V_{IH}$ or $V_{IL}$ $V_{OUT} = V_{CC}$ or GND	6.0	—	—	±0.5	—	±5.0	$\mu\text{A}$
Input Leakage Current	$I_{IN}$	$V_{IN} = V_{CC}$ or GND	6.0	—	—	±0.1	—	±1.0	
Quiescent Supply Current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND	6.0	—	—	4.0	—	40.0	

AC ELECTRICAL CHARACTERISTICS ( Input  $t_r = t_f = 6\text{ns}$  )

PARAMETER	SYMBOL	TEST CONDITION	CL (pF) $V_{CC}$ (V)		Ta = 25°C			Ta = -40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	$t_{TLH}$ $t_{THL}$		50	2.0	—	20	60	—	75	ns
				4.5	—	6	12	—	15	
				6.0	—	5	10	—	13	
Propagation Delay Time	$t_{pLH}$ $t_{pHL}$		50	2.0	—	38	90	—	115	
				4.5	—	12	18	—	23	
				6.0	—	10	15	—	20	
			150	2.0	—	51	130	—	165	
				4.5	—	17	26	—	33	
				6.0	—	14	22	—	28	
Output Enable Time	$t_{pZL}$ $t_{pZH}$	$R_L = 1\text{k}\Omega$	50	2.0	—	56	130	—	165	
				4.5	—	17	26	—	33	
				6.0	—	13	22	—	28	
			150	2.0	—	69	170	—	215	
				4.5	—	22	34	—	44	
				6.0	—	17	29	—	37	
Output Disable Time	$t_{pLZ}$ $t_{pHZ}$	$R_L = 1\text{k}\Omega$	50	2.0	—	42	130	—	165	
				4.5	—	18	26	—	33	
				6.0	—	15	22	—	28	
Input Capacitance	$C_{IN}$				—	5	10	—	pF	
Output Capacitance	$C_{OUT}$				—	10	—	—		
Power Dissipation Capacitance	$C_{PD} (1)$				—	25	—	—		

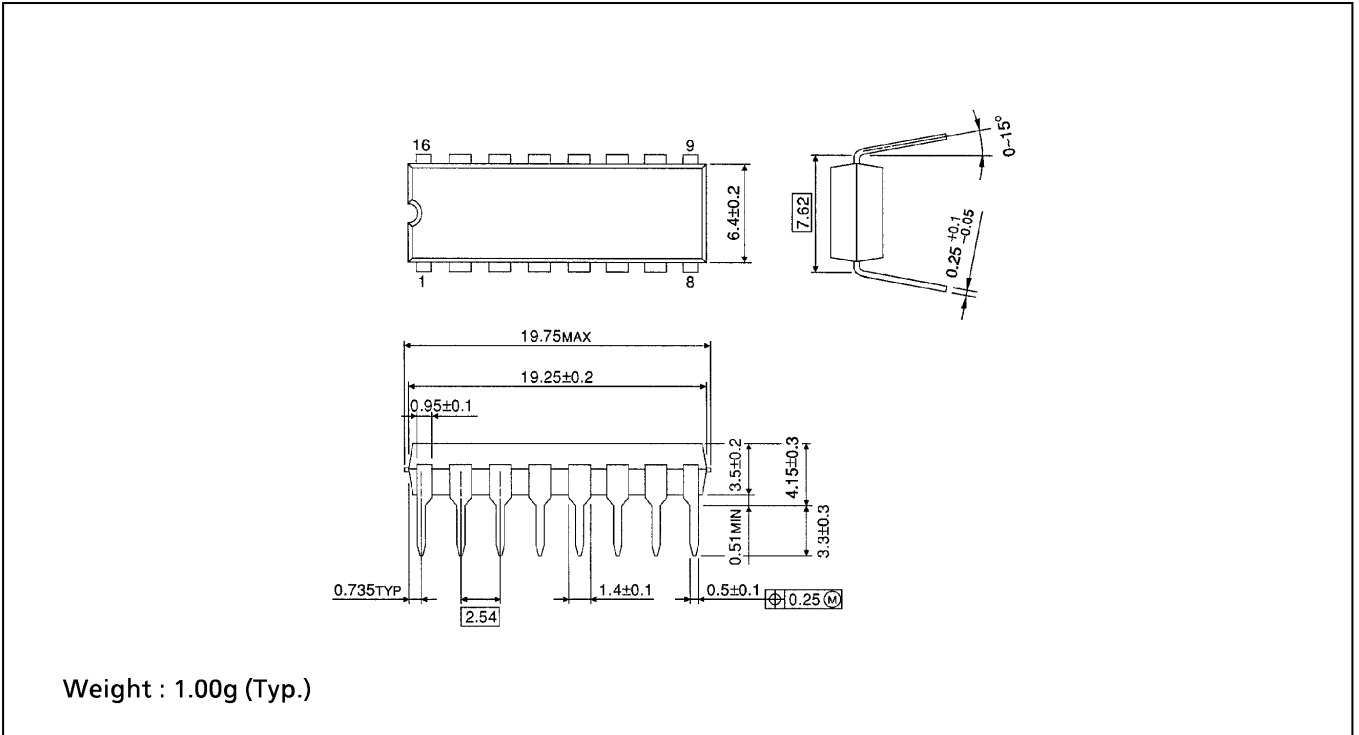
Note (1)  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 6 \text{ (per Gate)}$$

**DIP 16PIN OUTLINE DRAWING (DIP16-P-300-2.54A)**

Unit in mm



**SOP 16PIN (200mil BODY) OUTLINE DRAWING (SOP16-P-300-1.27)**

Unit in mm

