

TOSHIBA

TC74HC390AP/AF/AFN

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74HC390AP, TC74HC390AF, TC74HC390AFN

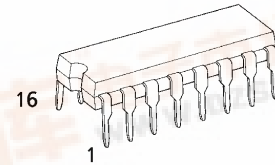
DUAL DECADE COUNTER

The TC74HC390A is a high speed CMOS DUAL DECADE COUNTER fabricated with silicon gate C²MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. It consists of two independent 4-bit counters, each composed of a divide-by-two and a divide-by-five counter. The divide-by-two counter is incremented on the negative going transition of clock A($\overline{CKA}$). The divided-by-five counter is incremented on the negative going transition of clock B($\overline{CKB}$). The counter can be cascaded to form decade, bi-quinary, or various combinations up to a divide-by-100 counter. When the CLR input is set high, the Q outputs are set to low independent of the clock inputs. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

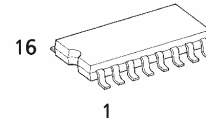
FEATURES:

- High Speed..... $f_{MAX} = 84\text{MHz}(\text{typ.})$
at $V_{CC} = 5\text{V}$
- Low Power Dissipation..... $I_{CC} = 4\mu\text{A}(\text{Max.})$ at $T_a = 25^\circ\text{C}$
- High Noise Immunity..... $V_{NIH} = V_{NIL} = 28\% V_{CC}(\text{Min.})$
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance... $|I_{OH}| = |I_{OL}| = 4\text{mA}(\text{Min.})$
- Balanced Propagation Delays... $t_{PLH} \approx t_{PHL}$
- Wide Operating Voltage Range... $V_{CC}(\text{opr.}) = 2\text{V} \sim 6\text{V}$
- Pin and Function Compatible with 74LS390

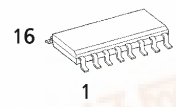
(Note) The JEDEC SOP (FN) is not available in Japan.



P (DIP16-P-300-2.54A)
Weight : 1.00g (Typ.)

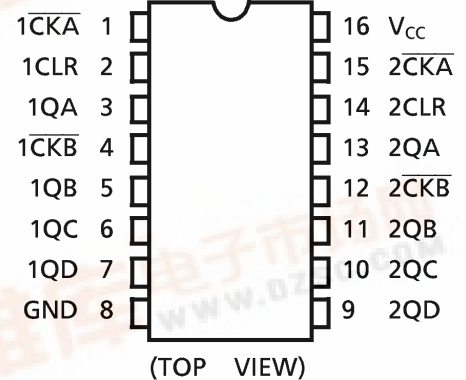


F (SOP16-P-300-1.27)
Weight : 0.18g (Typ.)

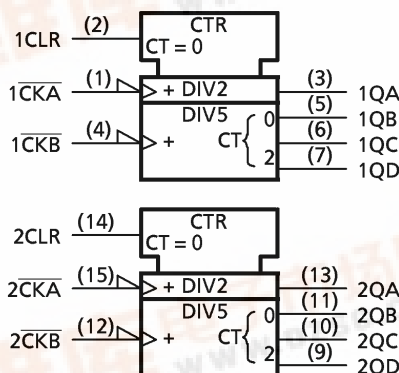


FN (SOL16-P-150-1.27)
Weight : 0.13g (Typ.)

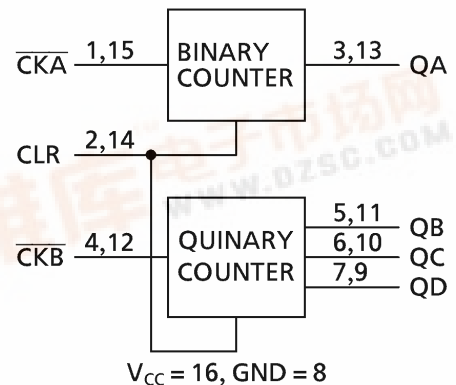
PIN ASSIGNMENT



IEC LOGIC SYMBOL



BLOCK DAIGRAM



961001EBA2

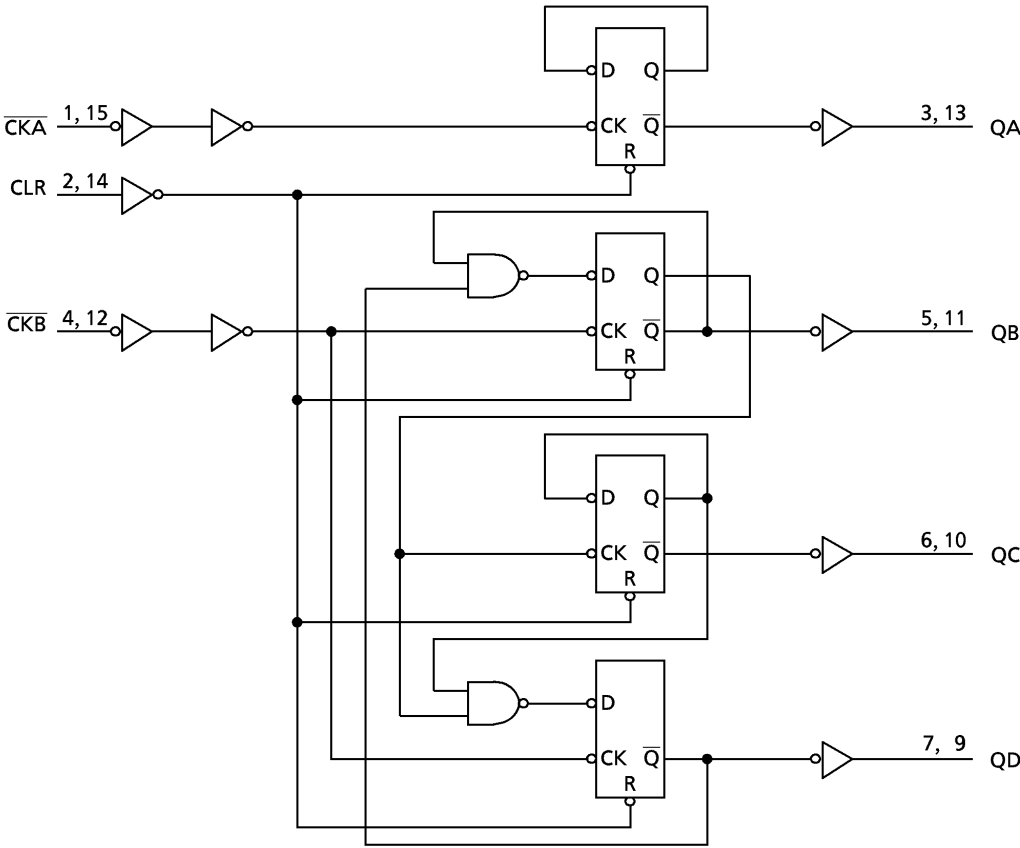
● TOSHIBA is continually working to improve the quality and the reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to observe standards of safety, and to avoid situations in which a malfunction or failure of a TOSHIBA product could cause loss of human life, bodily injury or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent products specifications. Also, please keep in mind the precautions and conditions set forth in the TOSHIBA Semiconductor Reliability Handbook.

TRUTH TABLE

INPUTS			OUTPUTS			
$\overline{\text{CKA}}$	$\overline{\text{CKB}}$	CLR	QA	QB	QC	QD
X	X	H	L	L	L	L
$\downarrow$	X	L	BINARY COUNT UP			
X	$\downarrow$	L	QUINARY COUNT UP			

X : Don't Care

SYSTEM DIAGRAM (1/2 package)

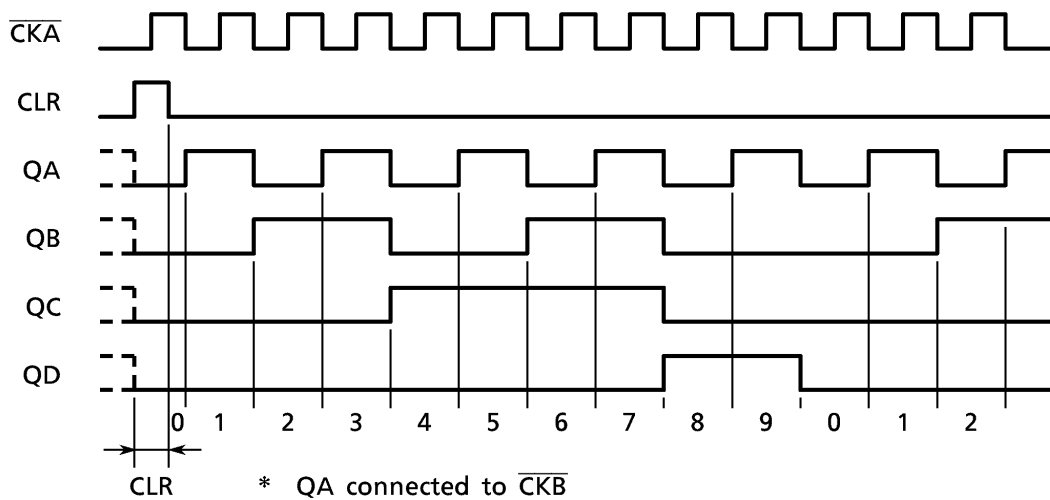


961001EBA2'

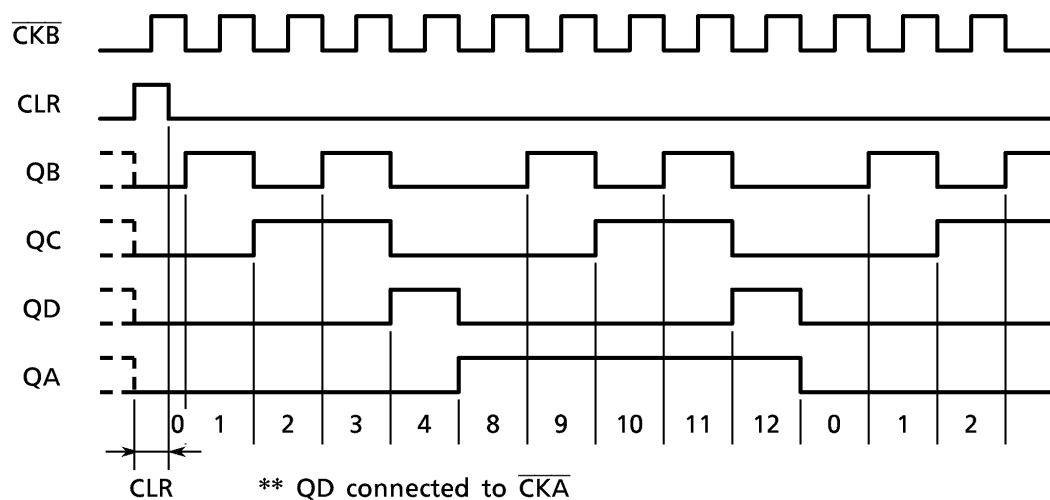
● The products described in this document are subject to foreign exchange and foreign trade control laws.
● The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA CORPORATION for any infringements of intellectual property or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any intellectual property or other rights of TOSHIBA CORPORATION or others.
● The information contained herein is subject to change without notice.

TIMING CHART

(1) BCD COUNT SEQUENCE*



(2) BI-QUINARY COUNT SEQUENCE**



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC} + 0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC} /Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	$^{\circ}\text{C}$

*500mW in the range of $T_a = -40^{\circ}\text{C} \sim 65^{\circ}\text{C}$. From $T_a = 65^{\circ}\text{C}$ to 85°C a derating factor of $-10\text{mW}/^{\circ}\text{C}$ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	$^{\circ}\text{C}$
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000 (V_{CC} = 2.0\text{V})$ $0 \sim 500 (V_{CC} = 4.5\text{V})$ $0 \sim 400 (V_{CC} = 6.0\text{V})$	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	$T_a = 25^{\circ}\text{C}$			$T_a = -40 \sim 85^{\circ}\text{C}$		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}		2.0 4.5 6.0	1.50 3.15 4.20	— — —	— — —	1.50 3.15 4.20	— — —	V
Low - Level Input Voltage	V_{IL}		2.0 4.5 6.0	— — —	— — —	0.50 1.35 1.80	— — —	0.50 1.35 1.80	V
High - Level Output Voltage	V_{OH}	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OH} = -20\mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	— — —	1.9 4.4 5.9	— — —	V
			4.5 6.0	4.18 5.68	4.31 5.80	— —	4.13 5.63	— —	
Low - Level Output Voltage	V_{OL}	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OL} = 20\mu\text{A}$	2.0 4.5 6.0	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	0.1 0.1 0.1	V
			4.5 6.0	— —	0.17 0.18	0.26 0.26	— —	0.33 0.33	
Input Leakage Current	I_{IN}	$V_{IN} = V_{CC} \text{ or } \text{GND}$	6.0	—	—	± 0.1	—	± 1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC} \text{ or } \text{GND}$	6.0	—	—	4.0	—	40.0	

TIMING REQUIREMENTS (Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	Ta = 25°C		Ta = -40~85°C	UNIT
				TYP.	LIMIT	LIMIT	
Minimum Pulse Width (CK)	$t_{W(H)}$ $t_{W(L)}$		2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Pulse Width (CLR)	$t_{W(H)}$		2.0	—	75	95	
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Removal Time	t_{rem}		2.0	—	25	30	
			4.5	—	5	6	
			6.0	—	5	5	
Clock Frequency (CKA)	f		2.0	—	6	5	MHz
			4.5	—	32	26	
			6.0	—	38	31	
Clock Frequency (CKB)	f		2.0	—	6	5	
			4.5	—	31	25	
			6.0	—	36	29	

AC ELECTRICAL CHARACTERISTICS ($C_L = 15\text{pF}$, $V_{CC} = 5\text{V}$, Ta = 25°C, Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		—	4	8	ns
Propagation Delay Time (CKA—QA)	t_{pLH} t_{pHL}		—	10	20	
Propagation Delay Time (CKA—QC)	t_{pLH} t_{pHL}	QA connected to $\overline{\text{CKB}}$	—	29	51	
Propagation Delay Time (CKB—QB, QD)	t_{pLH} t_{pHL}		—	12	22	
Propagation Delay Time (CKB—QC)	t_{pLH} t_{pHL}		—	17	32	
Propagation Delay Time (CLR—Qn)	t_{pHL}		—	12	26	
Maximum Clock Frequency (CKA)	f_{MAX}		35	84	—	MHz
Maximum Clock Frequency (CKB)	f_{MAX}		33	65	—	

AC ELECTRICAL CHARACTERISTICS ($C_L = 50\text{pF}$, Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	$T_a = 25^\circ\text{C}$			$T_a = -40 \sim 85^\circ\text{C}$		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	—	30	75	—	95	ns
			4.5	—	8	15	—	19	
			6.0	—	7	13	—	16	
Propagation Delay Time ($\overline{\text{CKA}} - \text{QA}$)	t_{pLH} t_{pHL}		2.0	—	39	120	—	150	
			4.5	—	13	24	—	30	
			6.0	—	11	20	—	26	
Propagation Delay Time ($\overline{\text{CKA}} - \text{QC}$)	t_{pLH} t_{pHL}	QA connected to CKB	2.0	—	102	290	—	365	
			4.5	—	34	58	—	73	
			6.0	—	29	49	—	62	
Propagation Delay Time ($\overline{\text{CKB}} - \text{QB}, \text{QD}$)	t_{pLH} t_{pHL}		2.0	—	45	130	—	165	
			4.5	—	15	26	—	33	
			6.0	—	13	22	—	28	
Propagation Delay Time ($\overline{\text{CKB}} - \text{QC}$)	t_{pLH} t_{pHL}		2.0	—	63	185	—	230	
			4.5	—	21	37	—	46	
			6.0	—	18	31	—	39	
Propagation Delay Time ($\overline{\text{CLR}} - \text{Qn}$)	t_{pHL}		2.0	—	45	150	—	190	
			4.5	—	15	30	—	38	
			6.0	—	13	26	—	32	
Maximum Clock Frequency ($\overline{\text{CKA}}$)	f_{MAX}		2.0	6	20	—	5	—	MHz
			4.5	32	77	—	26	—	
			6.0	38	90	—	31	—	
Maximum Clock Frequency ($\overline{\text{CKB}}$)	f_{MAX}		2.0	6	15	—	5	—	
			4.5	32	60	—	25	—	
			6.0	36	70	—	29	—	
Input Capacitance	C_{IN}			—	5	10	—	10	pF
Power Dissipation Capacitance	$C_{\text{PD}} (1)$			—	44	—	—	—	

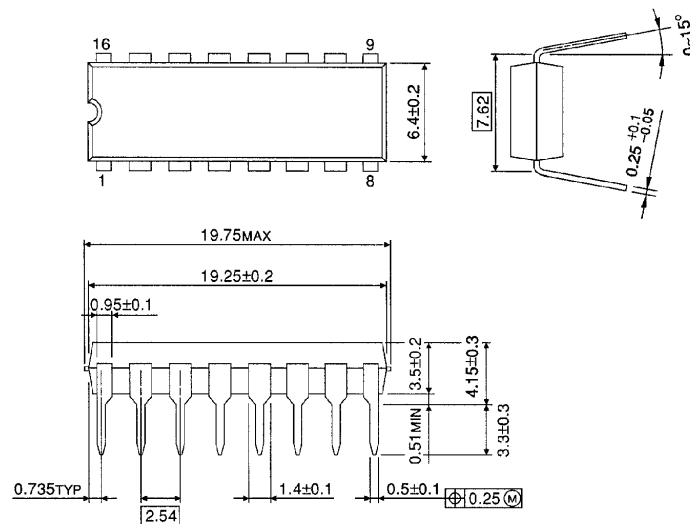
Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{\text{CC}}(\text{opr}) = C_{\text{PD}} \cdot V_{\text{CC}} \cdot f_{\text{IN}} + I_{\text{CC}} / 2 \text{ (per Counter)}$$

DIP 16PIN OUTLINE DRAWING (DIP16-P-300-2.54A)

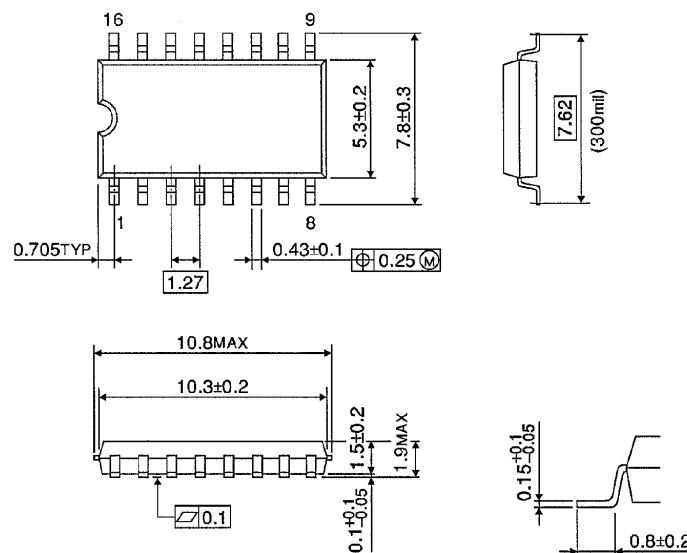
Unit in mm



Weight : 1.00g (Typ.)

SOP 16PIN (200mil BODY) OUTLINE DRAWING (SOP16-P-300-1.27)

Unit in mm

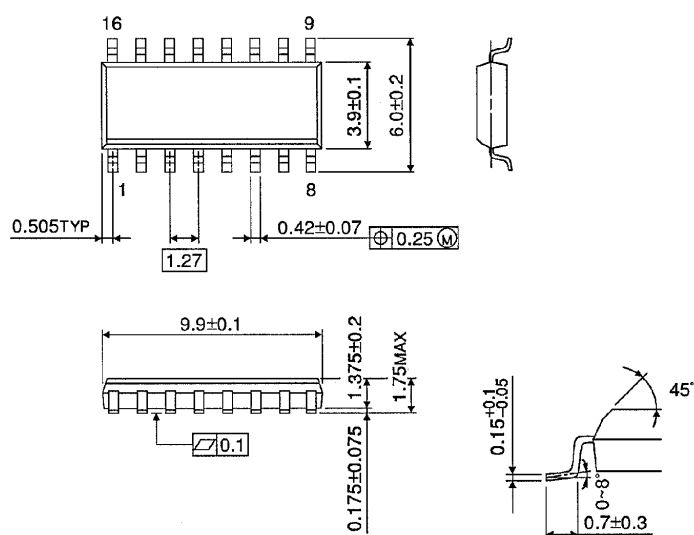


Weight : 0.18g (Typ.)

SOP 16PIN (150mil BODY) OUTLINE DRAWING (SOL16-P-150 -1.27)

Unit in mm

(Note) This package is not available in Japan.



Weight : 0.13g (Typ.)