

**TOSHIBA**

**TC74HCT174AP/AF/AFN**

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

# TC74HCT174AP, TC74HCT174AF, TC74HCT174AFN

## HEX D - TYPE FLIP FLOP WITH CLEAR

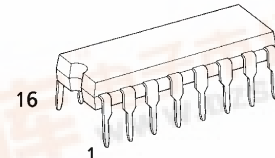
The TC74HCT174A is a high speed CMOS D - TYPE FLIP FLOP fabricated with silicon gate C<sup>2</sup>MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.

Information signals applied to the D inputs are transferred to the Q outputs on the positive going edge of the clock pulse. When the  $\overline{\text{CLR}}$  input is held low, the Q outputs are in the low logic level independent of the other inputs. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

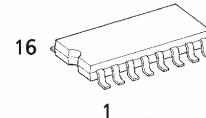
### FEATURES:

- High Speed..... $f_{\text{MAX}} = 56\text{MHz}(\text{typ.})$   
at  $V_{\text{CC}} = 5\text{V}$
- Low Power Dissipation..... $I_{\text{CC}} = 4\mu\text{A}(\text{Max.})$  at  $T_a = 25^\circ\text{C}$
- Compatible with TTL outputs.... $V_{\text{IH}} = 2.0\text{V}(\text{Min.})$   
 $V_{\text{IL}} = 0.8\text{V}(\text{Max.})$
- Wide Interfacing ability.....LSTTL, NMOS, CMOS
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance... $|I_{\text{OH}}| = I_{\text{OL}} = 4\text{mA}(\text{Min.})$
- Balanced Propagation Delays.... $t_{\text{PLH}} \approx t_{\text{PHL}}$
- Pin and Function Compatible with 74LS174

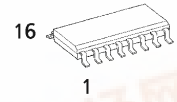
(Note) The JEDEC SOP (FN) is not available in Japan.



P (DIP16-P-300-2.54A)  
Weight : 1.00g (Typ.)

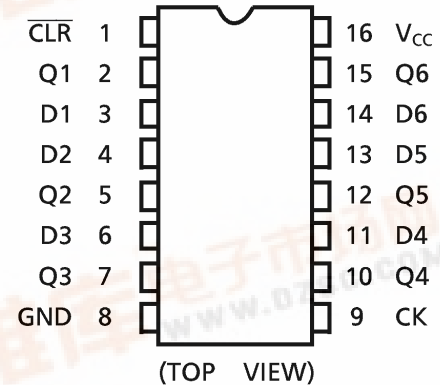


F (SOP16-P-300-1.27)  
Weight : 0.18g (Typ.)



FN (SOL16-P-150-1.27)  
Weight : 0.13g (Typ.)

### PIN ASSIGNMENT

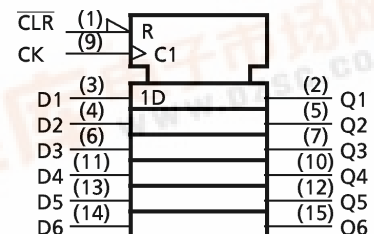


### TRUTH TABLE

INPUTS			OUTPUT	FUNCTION
$\overline{\text{CLR}}$	D	CK	Q	
L	X	X	L	CLEAR
H	L	$\uparrow$	L	—
H	H	$\uparrow$	H	—
H	X	$\downarrow$	$Q_n$	NO CHANGE

X : Don't Care

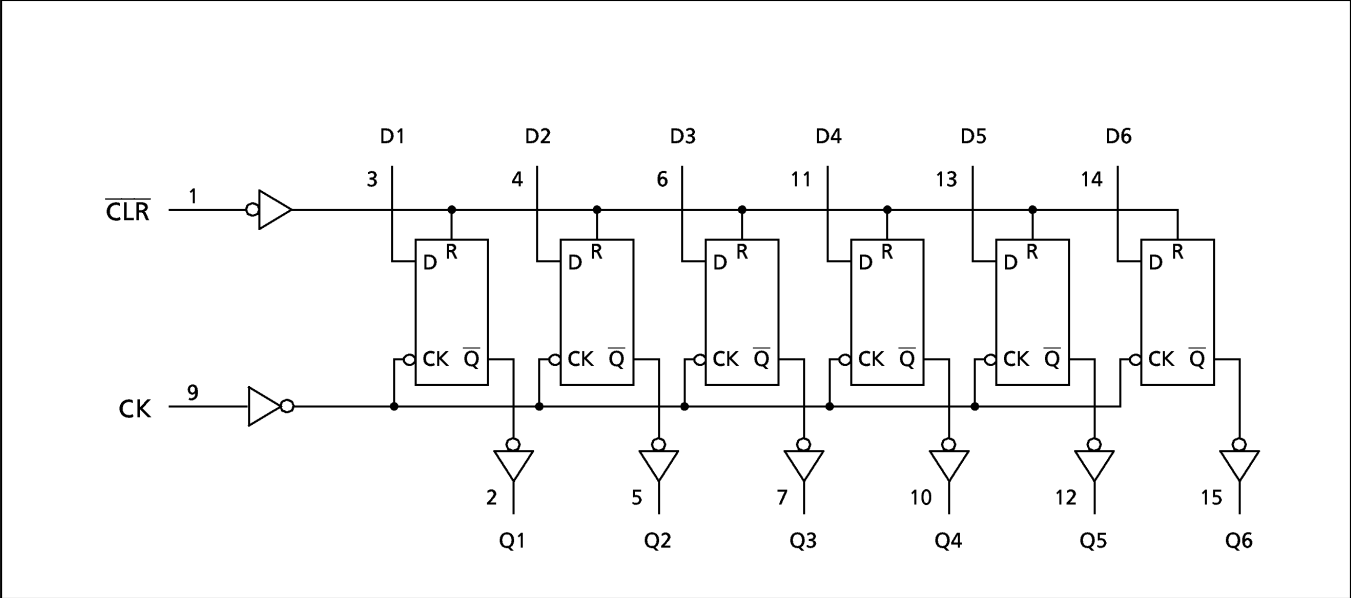
### IEC LOGIC SYMBOL



961001EBA2

● TOSHIBA is continually working to improve the quality and the reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to observe standards of safety, and to avoid situations in which a malfunction or failure of a TOSHIBA product could cause loss of human life, bodily injury or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent products specifications. Also, please keep in mind the precautions and conditions set forth in the TOSHIBA Semiconductor Reliability Handbook.

SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	$V_{CC}$	$-0.5 \sim 7$	V
DC Input Voltage	$V_{IN}$	$-0.5 \sim V_{CC} + 0.5$	V
DC Output Voltage	$V_{OUT}$	$-0.5 \sim V_{CC} + 0.5$	V
Input Diode Current	$I_{IK}$	$\pm 20$	mA
Output Diode Current	$I_{OK}$	$\pm 20$	mA
DC Output Current	$I_{OUT}$	$\pm 25$	mA
DC $V_{CC}$ / Ground Current	$I_{CC}$	$\pm 50$	mA
Power Dissipation	$P_D$	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	$T_{stg}$	$-65 \sim 150$	$^{\circ}\text{C}$

\*500mW in the range of  $T_a = -40^{\circ}\text{C} \sim 65^{\circ}\text{C}$ . From  $T_a = 65^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  a derating factor of  $-10\text{mW}/^{\circ}\text{C}$  shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	$V_{CC}$	$4.5 \sim 5.5$	V
Input Voltage	$V_{IN}$	$0 \sim V_{CC}$	V
Output Voltage	$V_{OUT}$	$0 \sim V_{CC}$	V
Operating Temperature	$T_{opr}$	$-40 \sim 85$	$^{\circ}\text{C}$
Input Rise and Fall Time	$t_r, t_f$	$0 \sim 500$	ns

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- The information contained herein is subject to change without notice.

## DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V <sub>CC</sub> (V)	Ta = 25°C			Ta = -40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V <sub>IH</sub>			4.5 5.5	2.0	—	—	2.0	—	V
Low - Level Input Voltage	V <sub>IL</sub>			4.5 5.5	—	—	0.8	—	0.8	V
High - Level Output Voltage	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -20 µA	4.5	4.4	4.5	—	4.4	—	V
			I <sub>OH</sub> = -4 mA	4.5	4.18	4.31	—	4.13	—	
Low - Level Output Voltage	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20 µA	4.5	—	0.0	0.1	—	0.1	V
			I <sub>OL</sub> = 4 mA	4.5	—	0.17	0.26	—	0.33	
Input Leakage Current	I <sub>IN</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND		5.5	—	—	±0.1	—	±1.0	µA
Quiescent Supply Current	I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND		5.5	—	—	4.0	—	40.0	mA
	I <sub>C</sub>	PER INPUT: V <sub>IN</sub> = 0.5V or 2.4V OTHER INPUT: V <sub>CC</sub> or GND		5.5	—	—	2.0	—	2.9	

TIMING REQUIREMENTS ( Input t<sub>r</sub> = t<sub>f</sub> = 6ns )

PARAMETER	SYMBOL	TEST CONDITION		V <sub>CC</sub> (V)	Ta = 25°C		Ta = -40~85°C	UNIT
					TYP.	LIMIT	LIMIT	
Minimum Pulse Width (CK)	t <sub>W(L)</sub> t <sub>W(H)</sub>			4.5	—	15	19	ns
				5.5	—	14	18	
Minimum Pulse Width (CLR)	t <sub>W(L)</sub>			4.5	—	15	19	
				5.5	—	14	18	
Minimum Set—up Time	t <sub>s</sub>			4.5	—	20	25	
				5.5	—	18	23	
Minimum Hold Time	t <sub>h</sub>			4.5	—	5	5	
				5.5	—	5	5	
Minimum Removal Time (CLR)	t <sub>rem</sub>			4.5	—	10	10	MHz
				5.5	—	10	10	
Clock Frequency	f			4.5	—	30	24	MHz
				5.5	—	33	26	

AC ELECTRICAL CHARACTERISTICS (  $C_L = 15\text{pF}$ ,  $V_{CC} = 5\text{V}$ ,  $T_a = 25^\circ\text{C}$ , Input  $t_r = t_f = 6\text{ns}$  )

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	$t_{TLH}$ $t_{THL}$		—	12	15	ns
Propagation Delay Time (CK—Q)	$t_{pLH}$ $t_{pHL}$		—	29	36	
Propagation Delay Time (CLR—Q)	$t_{pHL}$		—	29	36	
Maximum Clock Frequency	$f_{MAX}$		32	61	—	MHz

AC ELECTRICAL CHARACTERISTICS (  $C_L = 50\text{pF}$ , Input  $t_r = t_f = 6\text{ns}$  )

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C				Ta = -40~85°C		UNIT
			V <sub>CC</sub> (V)	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t <sub>TLH</sub>		4.5	—	8	15	—	19	ns
	t <sub>THL</sub>		5.5	—	7	14	—	18	
Propagation Delay Time (CK—Q)	t <sub>pLH</sub>		4.5	—	20	34	—	43	
	t <sub>pHL</sub>		5.5	—	17	31	—	39	
Propagation Delay Time (CLR—Q)	t <sub>pHL</sub>		4.5	—	20	34	—	43	
			5.5	—	17	31	—	39	
Maximum Clock Frequency	f <sub>MAX</sub>		4.5	30	54	—	24	—	MHz
			5.5	33	57	—	26	—	
Input Capacitance	C <sub>IN</sub>			—	5	10	—	10	pF
Power Dissipation Capacitance	C <sub>PD</sub> (1)			—	30	—	—	—	

Note (1)  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

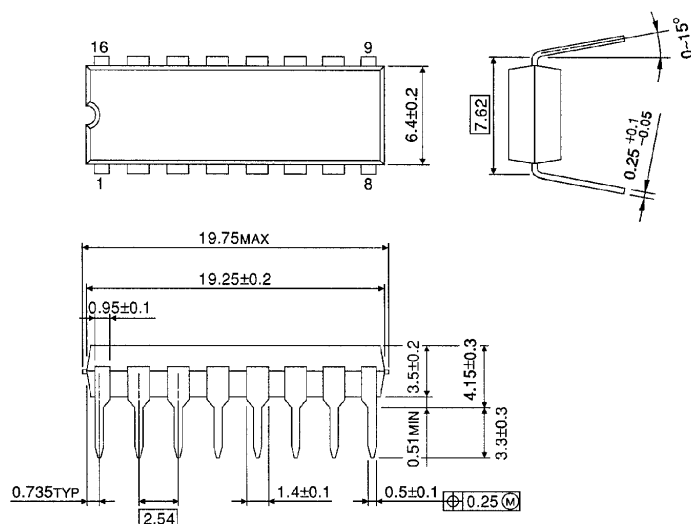
$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6 \text{ (per F/F)}$$

And the total  $C_{PD}$  when n pcs. of Flip Flop operate can be gained by the following equation :

$$C_{PD}(\text{total}) = 18 + 12 \cdot n$$

**DIP 16PIN OUTLINE DRAWING (DIP16-P-300-2.54A)**

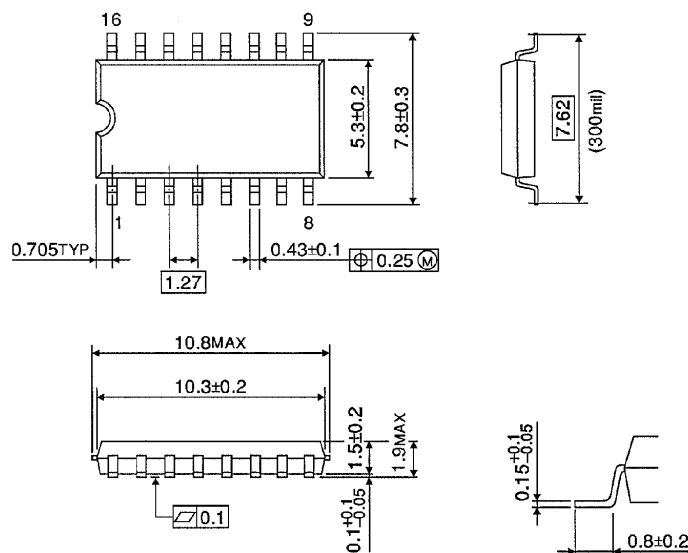
Unit in mm



Weight : 1.00g (Typ.)

**SOP 16PIN (200mil BODY) OUTLINE DRAWING (SOP16-P-300-1.27)**

Unit in mm

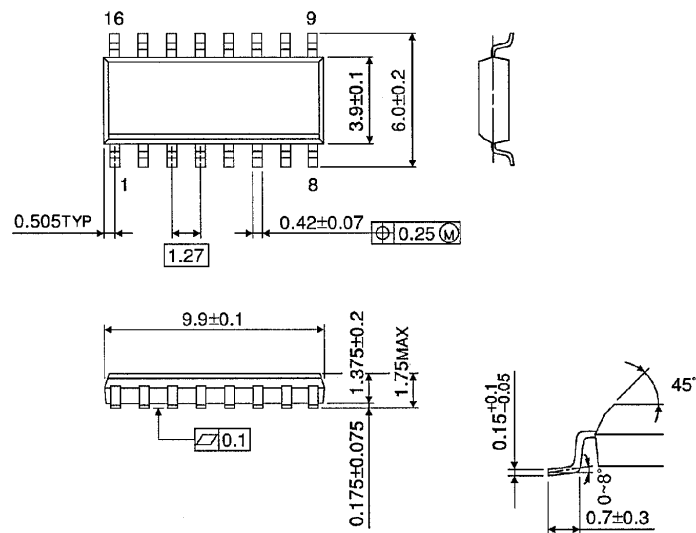


Weight : 0.18g (Typ.)

**SOP 16PIN (150mil BODY) OUTLINE DRAWING (SOL16-P-150 -1.27)**

Unit in mm

(Note) This package is not available in Japan.



Weight : 0.13g (Typ.)