

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

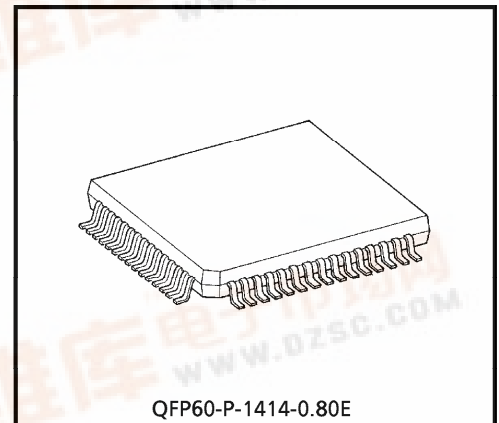
# TC9320F

## Frequency Counter System Microcontroller (DTS-10)

The TC9320F is a 4 bit CMOS microcontroller for frequency counter system with LCD driver.

The CPU has 4 bit parallel addition/subtraction (AI, SI instructions, etc.) logical operation (OR, AN instructions, etc.) multiple bits judgment, comparison instructions (TM, SL instructions, etc.) and time base functions. The TC9320F is housed in an 60 pin mini-flat package and is provided with ample I/O ports and exclusive key input ports which are controlled by powerful I/O instructions (IO, KEY instruction, etc.) and 1/2 duty and 1/2 bias driving ample LCD use exclusive output terminals.

Furthermore, the TC9320F has built in serial bus control function (SIO instruction) to powerfully control peripheral ICs, 6 bit A/D converter and D/A converter that are usable for field strength measurement and electronic volume control, and provides with many functions needed for frequency counter system.



Weight : 0.85 g (Typ.)

### FEATURES

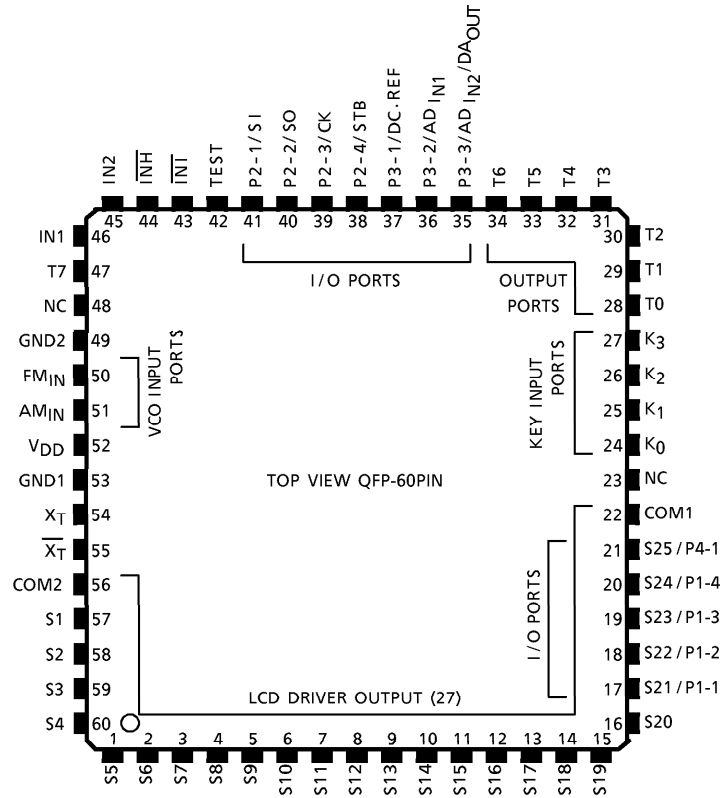
- 4 bit microcontroller frequency counter system
- 5 V  $\pm$  10% single power supply, CMOS structure for low power dissipation.
- Built-in LCD driver (1/2 duty, 1/2 bias, frame frequency : 100 Hz, 50 segments (Max.))
- Easy back up of data memory (RAM) and various ports (by the  $\overline{\text{INH}}$  terminal).
- Program memory (ROM) : 16 bits  $\times$  2048 steps
- Data memory (RAM) : 4 bits  $\times$  192 words
- 61 kinds of powerful instructions sets (all single word instructions)

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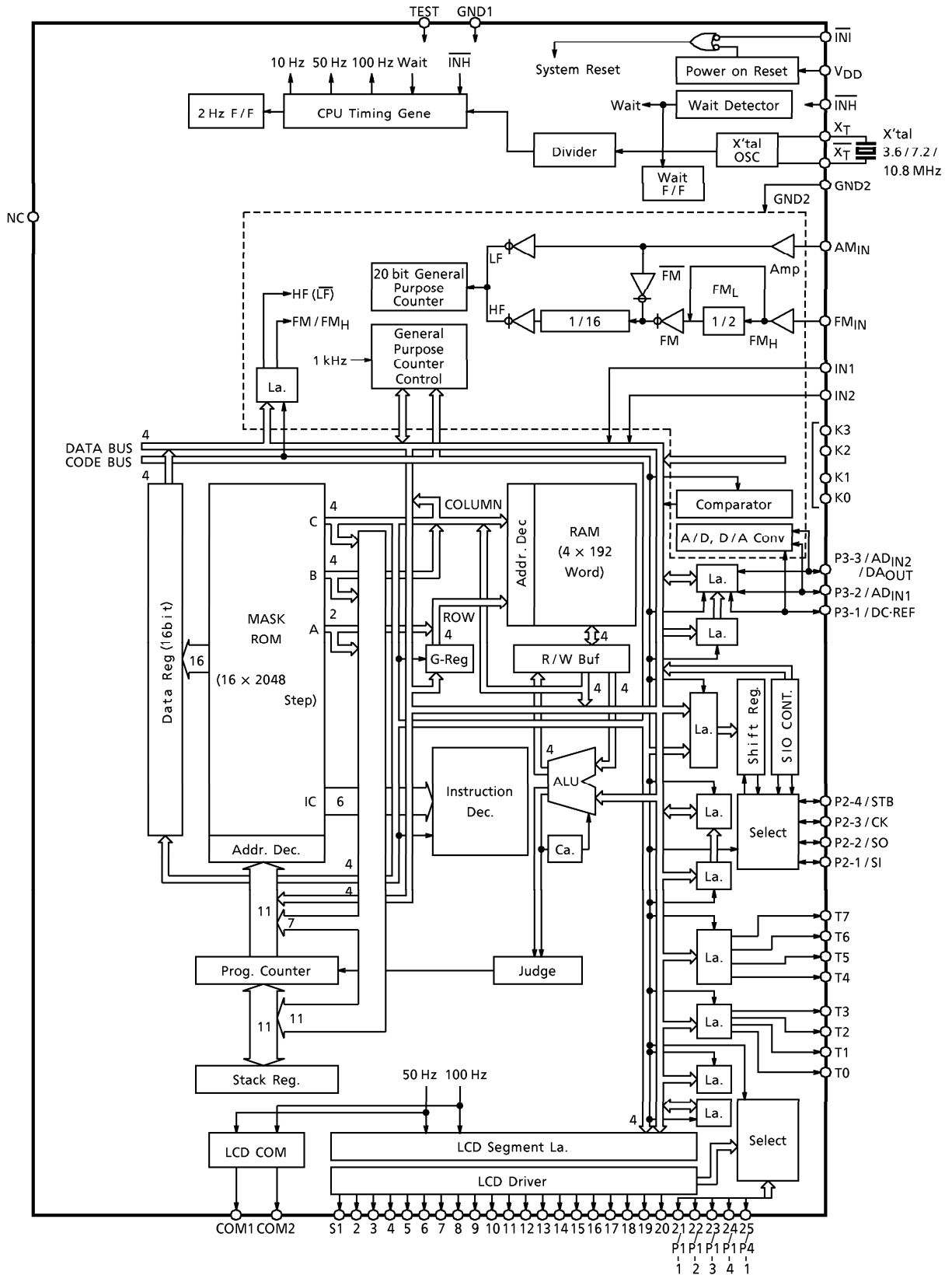
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- Instruction execution time 11.1  $\mu$ s (3.6 MHz or 7.2 MHz or 10.8 MHz crystal connection)
- Abundant add and subtract instructions (Add instruction : 12, subtract instruction : 12)
- Powerful composite judging instructions (TMTR, TMFR, TMT, TMF instructions, etc.)
- Data transfer at the same row address is possible.
- Register indirect transfer is possible (MVGD, MVGS instructions)
- Powerful 16 general registers (arranged in RAM)
- Stack level : 2 levels
- Program memory (ROM) has no conception of page and field, and JUMP and CAL instructions can be freely contained in 2048 steps.  
Further, contents of 16 bits data at any address in 1024 steps can be freely referred (DAL instruction)
- Built-in 20 bit general-use frequency counter (FM<sub>IN</sub>, AM<sub>IN</sub>)
- Independent frequency input terminals for FM and AM (FM<sub>IN</sub>, AM<sub>IN</sub>)
- 3 crystal oscillation frequencies are programmatically selectable. (3.6 MHz, 7.2 MHz, 10.8 MHz)
- Built-in powerful serial bus control function (I/O port-2 terminals are programmatically selectable.)
- Powerful I/O instructions (IO, KEY, SIO instruction, etc.)
- Exclusive key input port (K0~K3), abundant 25 (Max.) terminals LCD driver.
- Max. 27 I/O ports (I/O settable ports : 12 (Max.) output port : 8 (Max.) input port : 7 (Max.))
- Clock stop is possible programmatically (at CKSTP instruction : supply current below 10  $\mu$ A)
- Built-in 2 Hz timer F/F, 10/100 Hz internal pulse output (Internal port for time base)
- LCD driver Terminal (S21~S25) and I/O port (P1-1~P1-4, P4-1) are programmatically selectable.
- Built-in 6 bit A/D and D/A converters (Selectable by selecting I/O port-3 terminals (P3-1~P3-3) programmatically).
- OTP product : TC93P20F

PIN CONNECTION



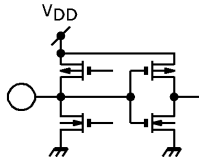
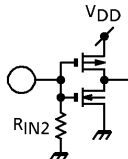
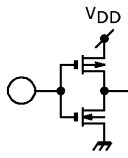
BLOCK DIAGRAM

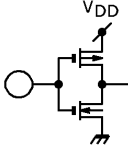
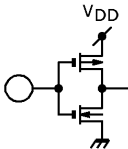
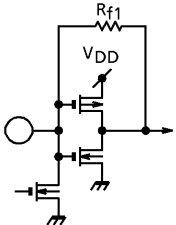


**PIN DESCRIPTION**

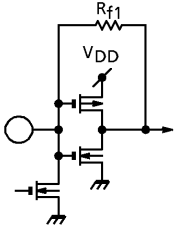
PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
22 56	COM1 COM2	LCD Common Output	<p>Common signal output terminals to LCD. Maximum 50 segments can be displayed in a matrix with S1~S25.</p> <p>Three levels of <math>V_{DD}</math>, <math>1/2 V_{DD}</math> and GND are output to these terminals in a 50Hz cycle at intervals of 5ms.</p> <p>(Note) : At time of system reset and execution of CKSTP and DISP OFF, output is automatically fixed at "L" level.</p>	
57~60 1~16 17~21	S1~S4 S5~S20 S21/P1-1 & S25/P4-1	LCD Segment Output  LCD Segment Output /I/O port 1, 4	<p>Segment signal output terminals to LCD. Maximum 50 segments can be displayed in a matrix with COM1 and COM2.</p> <p>Data are output to these terminals by executing SEG instruction (COM1 system) and MARK instruction (COM2 system).</p> <p>As to segment decoding, it is possible to perform it by creating its decoding pattern in ROM area and using DAL command.</p> <p>S21/P1-1~S25/P4-1 can be used both as 5bit I/O port and segment output.</p> <p>Assignment to I/O port is executed by contents of internal port called TERMINAL CONTROL.</p> <p>I/O designation for every bit can be made for these ports, In case of using I/O port, it can be assigned to input or output for each bit by program.</p> <p>There designate is executed by contents of internal port call PART-1, PORT-4 I/O CONTROL.</p> <p>(Note) : At time of system reset and execution of CKSTP command and DISP OFF, output is automatically fixed at "L" level.</p> <p>(Refer to Note 3.)</p>	
23	NC	No Connection	<p>This terminal must be left open.</p> <p>In case of OTP product TC93P20F, this terminal serves as <math>V_{pp}</math> terminal.</p>	—

PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
24~27	K0~K3	Key Input Port	<p>4 bit input ports for key matrix input. When KEY instruction these ports specified in the operand is executed, data of these terminals are read in RAM.</p> <p>All terminals have built in pull-down resistors. Further, the output ports T0~T6 are normally used for key return timing signal.</p>	
28~34 47	T0~T6 T7	Key Timing Output Port	<p>4 bit (T0~T3), 3 bit (T4~T6) and 1 bit (T7) output terminals.</p> <p>T0~T6 ports are normally used for key return timing signal output of key matrix. (Refer to Notes 2 and 3.)</p>	
35 36 37	P3-3 / AD_IN2 / DA_OUT P3-2 / AD_IN1 P3-1 / DC-REF	I/O Port 3 /AD Analog Voltage Input /DA Analog Voltage Output /DA Analog Voltage Input /Reference Voltage Input	<p>3 bit I/O ports. I/O designation for every bit can be made for these ports. This designation is made according to contents of the internal port called PORT-3 I/O CONTROL.</p> <p>Further, these terminals also serve for the analog input of the built-in 2 channel A/D converter and analog output of 1-channel D/A converter.</p> <p>A/D and D/A converter input/output selection is controlled according to contents of AD_ON, DA_ON or AD_SEL bit. The built-in A/D converter is of programmably sequential comparison type, and P3-1 is the reference voltage input, P3-2 is the analog comparison voltage input, and P3-3 is the analog comparison voltage input or analog voltage output.</p> <p>(Note) : A ladder resistance that generates internal D/A reference voltage is used commonly by the A/D and D/A converters.</p> <p>When both the A/D and D/A converters are used simultaneously, DA_ON bit is set to "0" and D/A output is made to high impedance at time of A/D conversion. It is therefore necessary to hold potential with a capacitor, etc.</p> <p>(Refer to Notes 1, 2 and 3.)</p>	

PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
38~41	P2-4/STB P2-3/CK P2-2/SO P2-1/SI	I/O Port 2 /Strobe Pulse Output /Serial Clock Output /Serial Data Output /Serial Data Input	4 bit I/O ports. I/O designation for every bit can be made for these ports. This designation is made according to contents of the internal port called PORT-2 I/O CONTROL. Further, these terminals are also used as the serial interface (SIO). Selection of SIO is controlled according to contents of SIO ON bit and in case of these serial interface, peripheral optional ICs can be controlled by executing SIO command. Serial transfer in NCD mode is programmably selectable. (Refer to Notes 1, 2 and 3.)	
42	TEST	Test Mode Control Input	Test mode control input terminal. The device is put in the test mode when "H" level signal is input and becomes the normal operating state when "L" level signal is input or in NC state. (A pull-down resistor has been built in.)	
43	$\overline{\text{INI}}$	Initialize Input	Device system reset signal input terminal. As long as the $\overline{\text{INI}}$ terminal is kept at "L" level, a system is kept in the reset state and when it becomes "H" level, a program starts from address 0. Normally, the system is reset when 0~3.5 V is supplied to the $V_{DD}$ terminal (Power ON Reset) and therefore, this terminal is used by fixing at "H" level. (Refer to Notes 1 and 3.)	

PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
44	$\overline{\text{INH}}$	Inhibit Input Terminal	<p>This is the <math>\overline{\text{INH}}</math> port input terminal. Normally, this terminal is used for radio mode selecting signal input or battery detection signal input.</p> <p>When CKSTP instruction is used in a program and this CKSTP instruction is executed while the <math>\overline{\text{INH}}</math> terminal is at "L" level, it is possible to stop the internal clock generator and CPU operation and put a system in the memory backup state with low current consumption (below 10 <math>\mu\text{A}</math>).</p> <p>(Note) : CKSTP instruction is effective when the <math>\overline{\text{INH}}</math> terminal is at "L" level and when this instruction is executed at "H" level, the same operation as NOOP instruction results.</p> <p>(Note) : In the radio OFF mode or back-up mode, it is necessary to set reference internal ports (4 bits) at all "1" (Radio OFF mode).</p>	
45 46	IN2 IN1	Input Port 2 Input Port 1	These terminals are input ports.	
48	NC	No Connection	This terminal must be left open.	—
49	GND2	Analog GND Terminal	GND terminal only for frequency counter and AD/DA converter analog units.	—
50	FM <sub>IN</sub>	FM Band Signal Input	<p>This is an input terminal for FM band. The FM<sub>H</sub> mode and FM<sub>L</sub> mode are selectable by Radio instruction.</p> <p>In case of FM<sub>L</sub> mode, local oscillation output (VCO output) of 30 to 140 MHz (0.3 V<sub>p-p</sub> Min.) is input and in case of FM<sub>H</sub> mode, 30 to 185 MHz (0.5 V<sub>p-p</sub> Min.) is input.</p> <p>Having a built-in input amplifier, operates at small amplitude with a capacitor connected.</p>	



PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
51	AMIN	AM Band Signal Input	<p>This is an input terminal for AM band. The LF mode and HF mode are selectable by Radio instruction.</p> <p>In case of LF mode, local oscillation output (VCO output) of 0.5 to 20 MHz (0.3 V<sub>p-p</sub> Min.) and HF mode, 1 to 40 MHz (0.3 V<sub>p-p</sub> Min.) is input.</p> <p>Having a built-in input amplifier, operates at small amplitude with a capacitor connected.</p> <p>(Note) : When reference internal ports (4 bits) are set at all "1" or FM<sub>H</sub> Mode or FM<sub>L</sub> Mode is set, this input is pulled down.</p>	
52	VDD	Power Supply Terminal	<p>Power supply terminal.</p> <p>At time of Radio operation, 5 V ± 10% is applied.</p> <p>In the back-up state (when executing CKSTP instruction), voltage can be reduced to 2 V.</p> <p>Further, when voltage drops below 3.5 V during the operation of CPU, CPU stops (CPU Wait Mode) to prevent malfunction it restarts when voltage increases above 3.5 V.</p> <p>As (Wait Mode) resulted under this condition can be detected by Wait F/F bit, perform initialization, clock correction, etc. programmatically.</p> <p>Further, when 0 to 3.5 V is applied to this terminal, a device is reset and a program starts from address 0 (power On Reset).</p> <p>(Note) : Rise time of supply voltage on a device shall be 10~100 ms for the power ON reset operation.</p> <p>(Refer to Note 1)</p>	—
53	GND1	Digital GND Terminal	GND terminal for CPU and the logic unit.	—

PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
54	X <sub>T</sub>	Crystal Oscillation Terminal	Crystal resonator connecting terminal. It can be selectable Crystal resonator among 3.6 MHz, 7.2 MHz, 10.8 MHz. Adjust oscillation frequency (7.2 MHz) while observing LCD segment waveform. When CKSTP instruction is executed, oscillation stops automatically. (Refer to Note 1)	
55	$\overline{X_T}$			

(Note 1) : When a device is reset ( $V_{DD} = 0 \rightarrow 3.5V$  and  $\overline{INI} = "L" \rightarrow "H"$ ), I/O ports are set to the input, terminals serving as I/O ports and AD/DA converters are to the input of I/O ports, terminals serving as I/O ports and serial I/O ports are set to the input of I/O ports.

Crystal oscillation signal is designated to 10.8 MHz.

(Note 2) : When CKSTP instruction is executed, outputs of the output ports and I/O ports are all set at "L" level.

(Note 3) : When a device is reset, contents of output ports and internal ports are indefinite and it is therefore necessary to initialize them programmatically.

**MAXIMUM RATINGS** (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V <sub>DD</sub>	-0.3~7.0	V
Input Voltage	V <sub>IN</sub>	-0.3~V <sub>DD</sub> + 0.3	V
Power Dissipation	P <sub>D</sub>	400	mW
Operation Temperature	T <sub>opr</sub>	-40~85	°C
Storage Temperature	T <sub>stg</sub>	-65~150	°C

**ELECTRICAL CHARACTERISTICS** (Unless otherwise specified, Ta = -40~85°C, V<sub>DD</sub> = 4.5~5.5 V)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
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**CPU operation / PLL stop**

Operating Power Supply Voltage Range	V <sub>DD1</sub>	—	Radio Stop / CPU Operation	3.5	5.0	5.5	V
Memory Holding Voltage Range	V <sub>HD</sub>	—	Crystal oscillation stop	2.0	~	5.5	V
Operating Power Supply Current	I <sub>DD1</sub>	—	Radio Stop / CPU Operation V <sub>DD</sub> = 5 V, Ta = 25°C in case of connecting 10.8 MHz X'tal	—	0.7	1.5	mA
Memory Holding Power Supply Current	I <sub>HD1</sub>	—	V <sub>DD</sub> = 5 V, Crystal oscillation stop	—	0.1	10	μA
Memory Holding Power Supply Current	I <sub>HD2</sub>	—	V <sub>DD</sub> = 2 V, Crystal oscillation stop	—	—	5	μA
Crystal Oscillation Frequency	f <sub>X<sub>T</sub></sub>	—	—	3.6	7.2	10.8	MHz

**CPU / Radio operation**

Operating Power Supply Voltage Range	V <sub>DD2</sub>	—	CPU / Radio Operation	4.5	5.0	5.5	V
Operating Power Supply Current	I <sub>DD2</sub>	—	CPU / Radio Operation (FM <sub>IN</sub> = 140 MHz) V <sub>DD</sub> = 5 V, Ta = 25°C	—	10	25	mA

**Radio operating frequency range**

FM <sub>IN</sub> (FM <sub>H</sub> Mode)	f <sub>FMH</sub>	—	V <sub>IN</sub> = 0.5 V <sub>p-p</sub>	30	~	185	MHz
FM <sub>IN</sub> (FM <sub>L</sub> Mode)	f <sub>FML</sub>	—	V <sub>IN</sub> = 0.3 V <sub>p-p</sub>	30	~	140	MHz
AM <sub>IN</sub> (HF Mode)	f <sub>HF</sub>	—	V <sub>IN</sub> = 0.3 V <sub>p-p</sub>	1	~	40	MHz
AM <sub>IN</sub> (LF Mode)	f <sub>LF</sub>	—	V <sub>IN</sub> = 0.3 V <sub>p-p</sub>	0.5	~	20	MHz

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
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Radio operating input amplitude range

FM <sub>IN</sub> (FM <sub>H</sub> Mode)	V <sub>IN</sub> (FM <sub>H</sub> )	—	f <sub>IN</sub> = 30~185 MHz	0.5	~	V <sub>DD</sub> - 0.5	V <sub>p-p</sub>
FM <sub>IN</sub> (FM <sub>L</sub> Mode)	V <sub>IN</sub> (FM <sub>L</sub> )	—	f <sub>IN</sub> = 30~140 MHz	0.3	~	V <sub>DD</sub> - 0.5	V <sub>p-p</sub>
AM <sub>IN</sub> (HF Mode)	V <sub>IN</sub> (HF)	—	f <sub>IN</sub> = 1~40 MHz	0.3	~	V <sub>DD</sub> - 0.5	V <sub>p-p</sub>
AM <sub>IN</sub> (LF Mode)	V <sub>IN</sub> (LF)	—	f <sub>IN</sub> = 0.5~20 MHz	0.3	~	V <sub>DD</sub> - 0.5	V <sub>p-p</sub>

LCD common output (COM1, COM2)

Output Current	High Level	I <sub>OH1</sub>	—	V <sub>OH</sub> = 4.5 V, V <sub>DD</sub> = 5 V	- 250	- 750	—	μA
	Low Level	I <sub>OL1</sub>	—	V <sub>OH</sub> = 0.5 V, V <sub>DD</sub> = 5 V	250	750	—	
1/2 Bias Voltage		V <sub>BS</sub>	—	V <sub>DD</sub> = 5 V, No Load	2.30	2.50	2.70	V

LCD segment output (S1~S25)

Output Current	High Level	I <sub>OH2</sub>	—	V <sub>OH</sub> = 4.5 V, V <sub>DD</sub> = 5 V	- 100	- 300	—	μA
	Low Level	I <sub>OL2</sub>	—	V <sub>OH</sub> = 0.5 V, V <sub>DD</sub> = 5 V	100	300	—	

P1-1~P1-4, P2-1~P2-4 (SO, CK, STB), P3-1~P3-3, P4-1, T0~T7 output port

Output Current	High Level	I <sub>OH3</sub>	—	V <sub>OH</sub> = 4.5 V, V <sub>DD</sub> = 5 V	- 1.0	- 3.0	—	mA
	Low Level	I <sub>OL3</sub>	—	V <sub>OH</sub> = 0.5 V, V <sub>DD</sub> = 5 V	1.0	3.0	—	

$\overline{\text{INH}}$  input port

$\overline{\text{INH}}$ Input Voltage	High Level	V <sub>IH2</sub>	—	—	V <sub>DD</sub> × 0.85	~	V <sub>DD</sub>	V
	Low Level	V <sub>IL2</sub>	—	—	0	~	V <sub>DD</sub> × 0.5	
Input Leak Current	High Level	I <sub>IH1</sub>	—	V <sub>IH</sub> = V <sub>DD</sub> = 5.5 V	—	—	± 2	μA
	Low Level	I <sub>IL1</sub>	—	V <sub>IL</sub> = 0 V, V <sub>DD</sub> = 5.5 V	—	—	± 2	

Key input port (K0~K3)

Input Voltage	High Level	V <sub>IH1</sub>	—	—	V <sub>DD</sub> × 0.7	~	V <sub>DD</sub>	V
	Low Level	V <sub>IL1</sub>	—	—	0	~	V <sub>DD</sub> × 0.3	
Pull-down Resistance		R <sub>IN1</sub>	—	V <sub>IH</sub> = V <sub>DD</sub> = 5 V, T <sub>a</sub> = 25°C	50	100	150	kΩ

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
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$\overline{INI}$ , IN1, IN2, P1-1~P1-4, P2-1~P2-4 (SI), P3-1~P3-3, P4-1 port

Input Voltage	High Level	$V_{IH1}$	—	—	$V_{DD} \times 0.7$	~	$V_{DD}$	V
	Low Level	$V_{IL1}$	—	—	0	~	$V_{DD} \times 0.3$	
Input Leak Current	High Level	$I_{IH1}$	—	$V_{IH} = V_{DD} = 5.5\text{ V}$	—	—	$\pm 2$	$\mu\text{A}$
	Low Level	$I_{IL1}$	—	$V_{IL} = 0\text{ V},$ $V_{DD} = 5.5\text{ V}$	—	—	$\pm 2$	

A/D, D/A converter (DC·REF, A/D<sub>IN1</sub>, A/D<sub>IN2</sub>, D/A<sub>OUT</sub>)

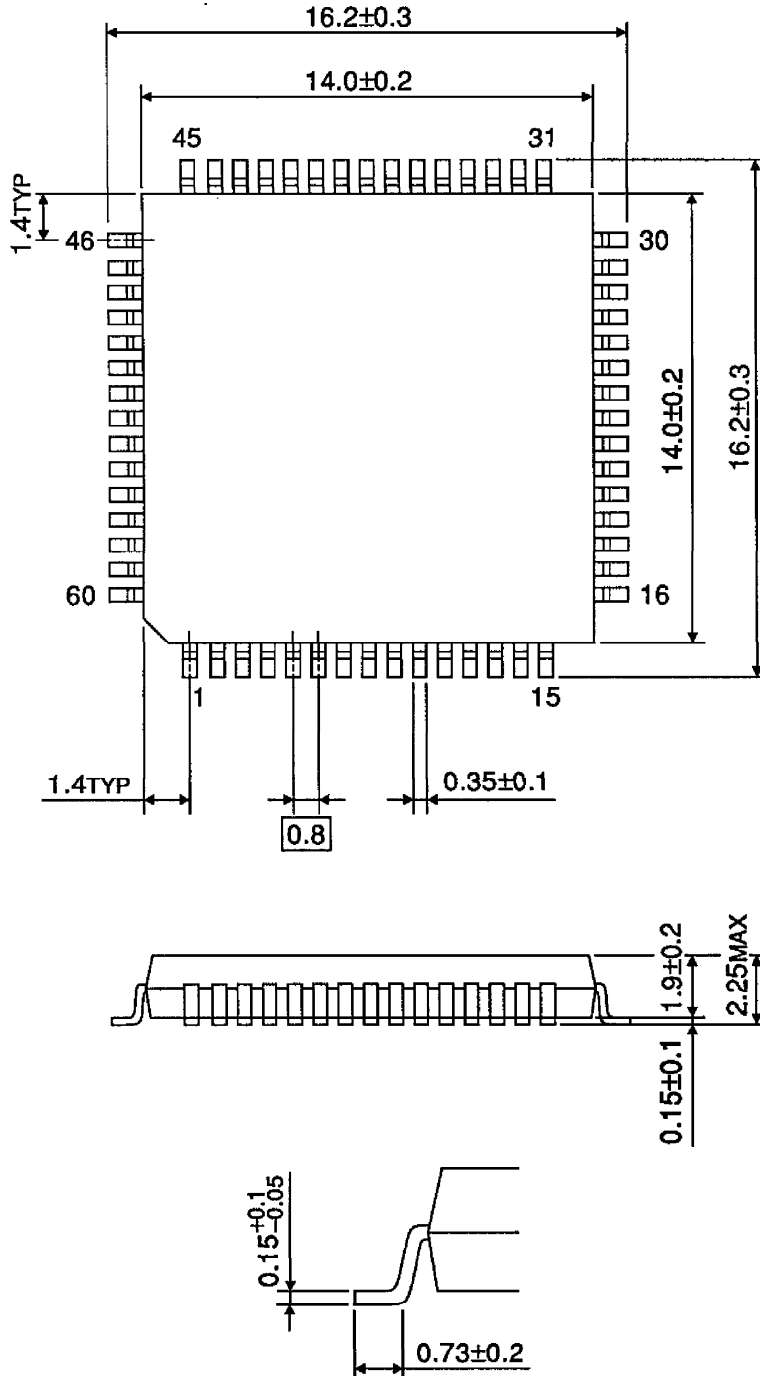
Analogue Input Voltage Range	$V_{ADI}$	—	AD <sub>IN1</sub> , AD <sub>IN2</sub>	0	~	$V_{DD}$	V
Analogue Reference Voltage Range	$V_{REF}$	—	DC·REF	1.5	~	$V_{DD}$	V
Resolution	$V_{RES}$	—	—	—	—	6	bit
Analogue Reference Voltage Input Current	$I_{REF}$	—	DC·REF, $T_a = 25^\circ\text{C},$ $V_{IH} = V_{DD} = 5\text{ V}$	—	0.5	1.0	mA
Analogue Output Voltage Range	$V_{DAO}$	—	DA <sub>OUT</sub>	0	~	$V_{DD} - 1.0$	V
Analogue Output Voltage Deviation	$\Delta V_{DA}$	—	$I_{DA} = \pm 100\ \mu\text{A},$ $V_{DD} = 5\text{ V}, T_a = 25^\circ\text{C}$	—	$\pm 50$	$\pm 150$	mV
Conversion Total Error	—	—	—	—	$\pm 0.5$	$\pm 1.5$	LSB

Other

FM <sub>IN</sub> , AM <sub>IN</sub> Input Feedback Resistance	$R_{f1}$	—	$V_{DD} = 5\text{ V}, T_a = 25^\circ\text{C}$	250	500	1000	k $\Omega$
X <sub>T</sub> Input Feedback Resistance	$R_{f2}$	—	$V_{DD} = 5\text{ V}, T_a = 25^\circ\text{C}$	500	1000	1750	k $\Omega$
TEST Input Pull-down Resistance	$R_{IN2}$	—	$V_{IH} = V_{DD} = 5\text{ V},$ $T_a = 25^\circ\text{C}$	15	30	60	k $\Omega$

**PACKAGE DIMENSIONS**  
**QFP60-P-1414-0.80E**

Unit : mm



Weight : 0.85 g (Typ.)