TOSHIBA   T6C63

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT   SILICON MONOLITHIC

T6C63

COLUMN DRIVER FOR A DOT MATRIX LCD

The T6C63 is a 240-channel-output column driver for an STN dot matrix LCD.

The T6C63 features a 42-V LCD drive voltage and a 20-MHz maximum operating frequency. The T6C63 is able to drive LCD panels with a duty ratio of up to 1/480.

It is recommended for use with the T6C14.

Unit: mm

T6C63	LEAD PITCH	
	IN	OUT
(UAN, 3NS)	0.60	0.074

Please contact Toshiba or an authorized Toshiba dealer for information on package dimensions.

TCP (Tape Carrier Package)

FEATURES

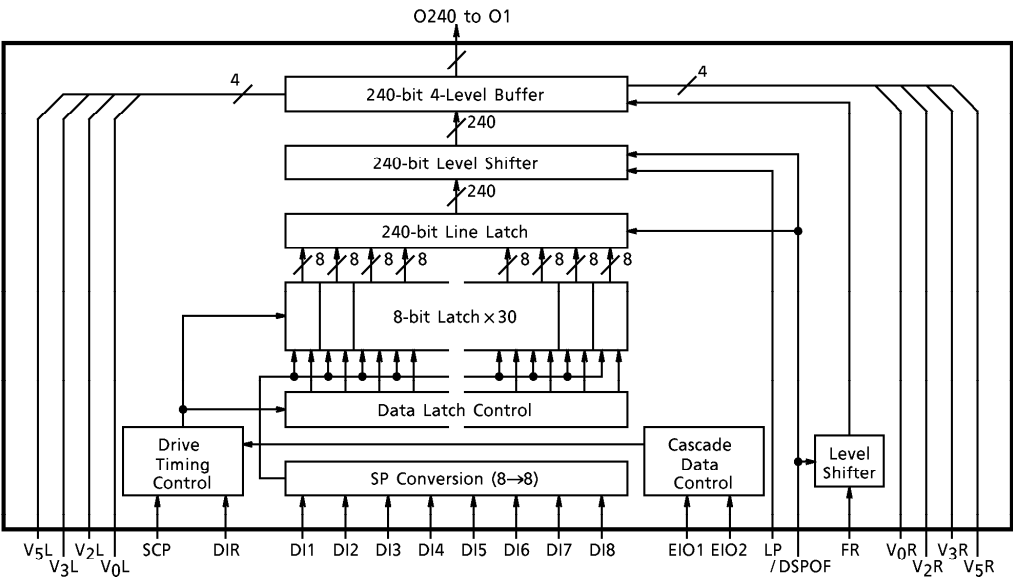- Display duty application : to 1/480

- LCD drive signal : 240

- Data transfer : 8-bit bidirectional

- Operating frequency : 20MHz (V_{DD} = 4.5V)
  12.5MHz (V_{DD} = 2.7V)

- LCD drive voltage : 14 to 42V (max 45V)

- Power supply voltage : 2.7 to 5.5V

- Operating temperature : −20 to 75°C

- LCD drive output resistance : 700Ω (typ.), 1200Ω (max) (20V, 1/13 bias)

- Display-off function : When /DSPOF is L, all LCD drive outputs (O1 to O240) remain at the V_5 level.

- Low power consumption : Cascade connection and auto enable transfer functions are available.
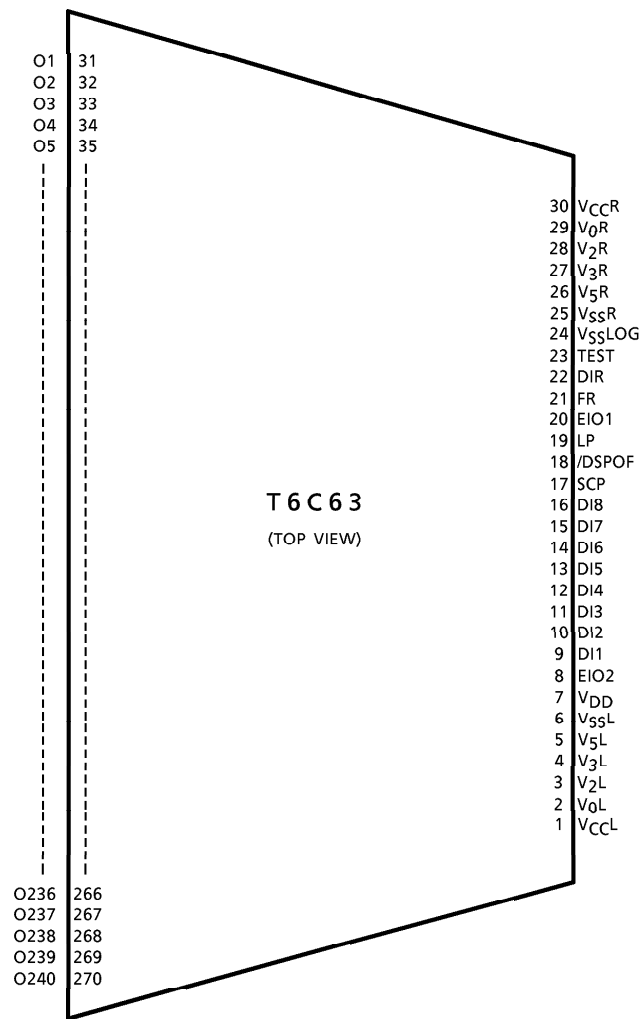
970917EBE2

BLOCK DIAGRAM

PIN ASSIGNMENT

```
O1   31
O2   32
O3   33
O4   34
O5   35
                                        30  VCCR
                                        29  V0R
                                        28  V2R
                                        27  V3R
                                        26  V5R
                                        25  VSSR
                                        24  VSSLOG
                                        23  TEST
                                        22  DIR
                                        21  FR
                                        20  EIO1
                                        19  LP
                                        18  /DSPOF
                                        17  SCP
              T6C63                     16  DI8
                                        15  DI7
            (TOP VIEW)                  14  DI6
                                        13  DI5
                                        12  DI4
                                        11  DI3
                                        10  DI2
                                         9  DI1
                                         8  EIO2
                                         7  VDD
                                         6  VSSL
                                         5  V5L
                                         4  V3L
                                         3  V2L
                                         2  V0L
                                         1  VCCL

O236  266
O237  267
O238  268
O239  269
O240  270
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(*) The above diagram shows the pin configuration of the LSI Chip, not that of the tape carrier package.

PIN FUNCTIONS

PIN NAME	I/O	FUNCTIONS	LEVEL
O1 to O240	Output	Output for LCD drive signal	V_0 to V_5
EIO1, EIO2	I/O	Input/output for enable signal DIR selects In or Out. Connect EIO (IN) of 1st LSI to L. For a cascade connection, connect EIO (OUT) to EIO (IN) of next LSI (refer to page 6).	V_{DD} to V_{SS}
DI1 to DI8	Input	Input for data signal Input for data signal	
DIR	Input	(Direction) Input for data flow direction select	
/DSPOF	Input	(Display off) /DSPOF = L : Display-off mode, (O1 to O240) remain at the V_5 level /DSPOF = H : Display-on mode, (O1 to O240) are operational.	
LP	Input	(Latch pulse) Display data is latched on falling edges of LP. When EIO (IN) = L, SCP·LP = H enables the 1st LSI.	
FR	Input	(Frame) Input for frame signal	
SCP	Input	(Shift clock pulse) Input for shift clock pulse	
TEST	Input	(Test) Fix to L or open	
V_{DD}	—	Power supply for internal logic (5.0V)	
$V_{SS}LOG$	—	Power supply for internal logic (0V)	
$V_{SS}L·R$	—	Power supply for LCD drive circuit	—
$V_5L·R$	—	Power supply for LCD drive circuit	
$V_{3/4}L·R$	—	Power supply for LCD drive circuit	
$V_{2/1}L·R$	—	Power supply for LCD drive circuit	
$V_0L·R$	—	Power supply for LCD drive circuit	
$V_{CC}L·R$	—	Power supply for LCD drive circuit	

RELATION BETWEEN FR, DATA INPUT AND OUTPUT LEVEL

FR	DATA INPUT (DI1 to DI8)	/DSPOF	OUTPUT LEVEL
H	L	H	V_2
H	H	H	V_0
L	L	H	V_3
L	H	H	V_5
—	—	L	V_5

DATA INPUT FORMAT

DIR	ENABLE PIN		(*1)	INPUT DATA LINE AND OUTPUT BUFFERS							
	(EIO1)	(EIO2)		DI1	DI2	DI3	DI4	DI5	DI6	DI7	DI8
H	IN	OUT	L	O240	O239	O238	O237	O236	O235	O234	O233
			F	O8	O7	O6	O5	O4	O3	O2	O1
L	OUT	IN	L	O1	O2	O3	O4	O5	O6	O7	O8
			F	O233	O234	O235	O236	O237	O238	O239	O240

(*1) L : Last data   F : First data

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TIMING DIAGRAM

DIR = H

T6C63 - 6
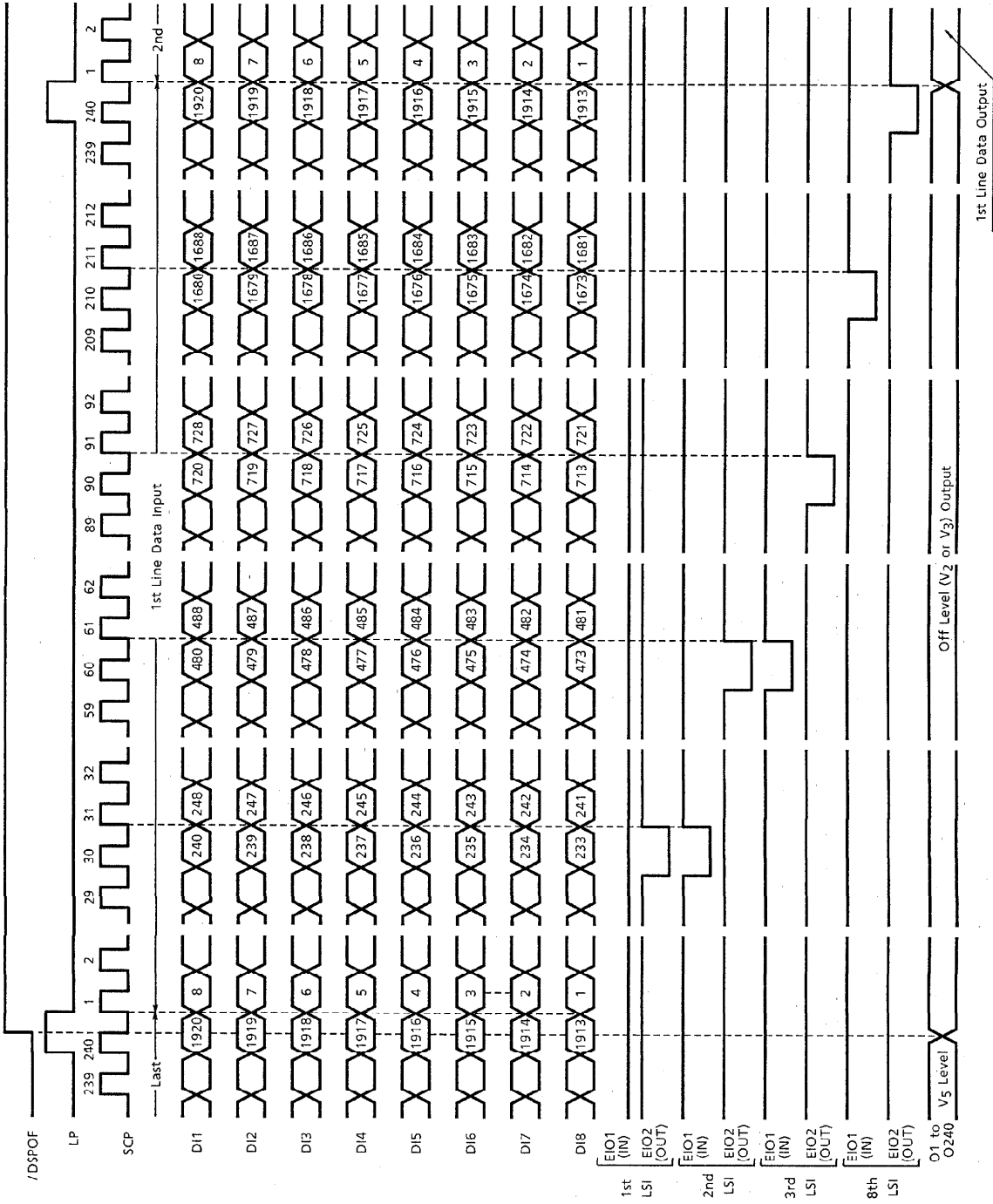
ABSOLUTE MAXIMUM RATINGS

(Ensure that the following conditions are maintained : $V_{CC} \geqq V_0 \geqq V_2 \geqq V_3 \geqq V_5 \geqq V_{SS}$)

ITEM	SYMBOL	PIN NAME	RATING	UNIT
Supply Voltage 1	V_{DD}	V_{DD}	-0.3 to 6.5	V
Supply Voltage 2	V_{CC}	$V_{CC}L/R$	-0.3 to 45.0	V
Supply Voltage 3	V_0, V_2	V_0L/R, $V_{2,1}L/R$	-0.3 to $V_{CC}+0.3$	V
Supply Voltage 4	V_3, V_5	$V_{3,4}L/R$, V_5L/R	-0.3 to $V_{CC}+0.3$	V
Input Voltage	V_{IN}	(*2)	-0.3 to $V_{DD}+0.3$	V
Operating Temperature	T_{opr}	—	-20 to 75	°C
Storage Temperature	T_{stg}	—	-40 to 125	°C

(*2) SCP, FR, LP, DIR, EIO1, EIO2, DI1 to DI8, /DSPOF, TEST

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS (Unless otherwise noted, $V_{SS}=0V$, $V_{DD}=2.7$ to $5.5V$, $Ta=-20$ to $75°C$)

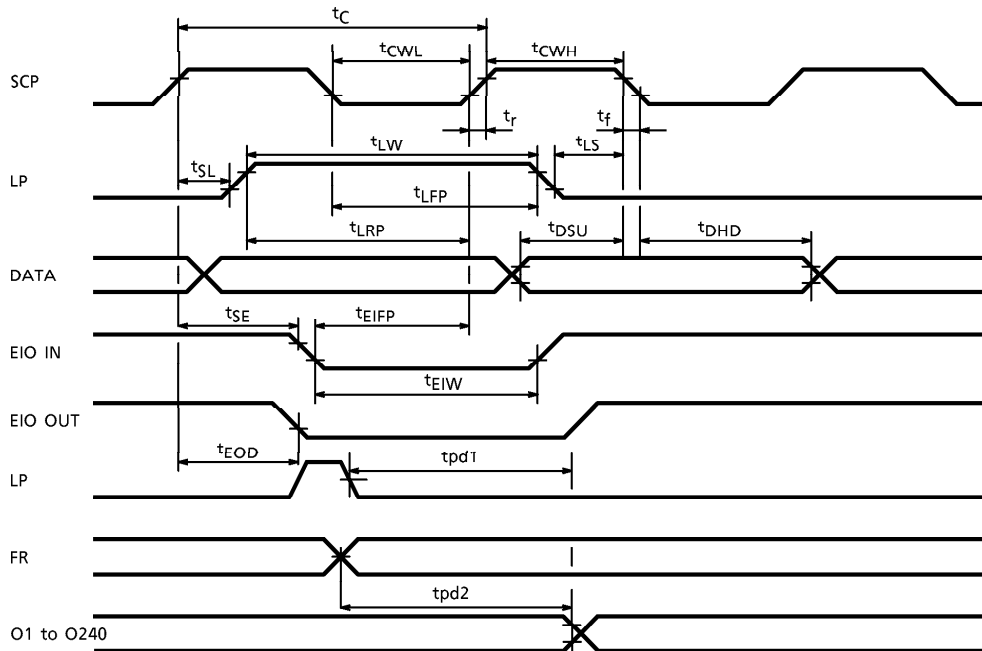| ITEM		SYMBOL	TEST CIR-CUIT	TEST CONDITION				MIN	TYP.	MAX	UNIT	PIN NAME
Supply Voltage 1		V_{DD}	—	—				2.7	5.0	5.5		V_{DD}
Supply Voltage 2		V_{CC}	—	—				14.0	—	42.0		$V_{CC}L/R$
Input Voltage	H Level	V_{IH}	—	—				$0.8 V_{DD}$	—	V_{DD}	V	SCP, FR, LP, DIR, EIO1, EIO2, DI1 to DI8, /DSPOF, TEST
	L Level	V_{IL}	—	—				0	—	$0.2 V_{DD}$		
Output Voltage	H Level	V_{OH}	—	$I_{OH}=-0.5mA$				$V_{DD}-0.5$	—	V_{DD}		EIO1, EIO2
	L Level	V_{OL}	—	$I_{OL}=0.5mA$				0	—	0.5		
Output Resistance	H Level	R_{OH}	—	$V_{OUT}=V_0-0.5V$ (*3)				—	700	1200	Ω	O1 to O240
	M Level	R_{OM}	—	$V_{OUT}=V_2\pm0.5V$ (*3)				—	700	1200		
		R_{OM}	—	$V_{OUT}=V_3\pm0.5V$ (*3)				—	700	1200		
	H Level	R_{OL}	—	$V_{OUT}=V_5+0.5V$ (*3)				—	700	1200		
Input Current		I_{IL}	—	V_{DD}	V_{CC}	CONDITION		-10	—	10	μA	V_0L/R V_2L/R V_3L/R V_5L/R
				5.0	42	Standby						
Current Consumption		I_{DD} Ope	—	5.0	20	Function (*4)		—	—	5.0	mA	V_{DD}
				2.7	20			—	—	2.5		
		I_{DD} St/by		5.0	20	Function (*5)		—	—	2.0		
				2.7	20			—	—	1.0		
		I_{CC} Leak		5.0	42	Standby		-10	—	10	μA	$V_{CC}L/R$

(*3) $V_{CC}=20V$, $1/13$ bias

(*4) $f_{SCP}=13MHz$, $f_{LP}=54kHz$, $f_{FR}=13.5kHz$, $f_{EIO}=650kHz$,
Data Format : every bit inverted, while internal data receriver is operating

(*5) $f_{SCP}=13MHz$, $f_{LP}=54kHz$, $f_{FR}=13.5kHz$,
Data Format : every bit inverted, Internal data receriver is sleeping

AC ELECTRICAL CHARACTERISTICS

TEST CONDITIONS (1) ($V_{SS} = 0V$, $V_{DD} = 4.5$ to $5.5V$, $V_{CC} = 14$ to $42V$, Ta = -20 to $75°C$)

ITEM	SYMBOL	TEST CONDITION	MIN	TYP.	MAX	UNIT
Clock Cycle	t_C	—	50	—	—	
SCP Pulse Width	t_{CWH}, t_{CWL}	—	10	—	—	
Data Set-up Time	t_{DSU}	—	8	—	—	
Data Hold Time	t_{DHD}	—	10	—	—	
SCP Rise / Fall Time	t_r, t_f	—	—	—	(*6)	
LP Rise Time	t_{LRP}	—	11	—	—	
LP Fall Time	t_{LFP}	—	7	—	—	
LP Pulse Width	t_{LW}	—	7	—	—	
SCP-to-LP Delay Time (SCP→LP)	t_{SL}	—	0	—	—	ns
LP-to-SCP Delay Time (LP→SCP)	t_{LS}	—	7	—	—	
EIO IN Rise Time	t_{EIFP}	—	20	—	—	
EIO IN Pulse Width	t_{EIW}	—	9	—	—	
SCP-to-EIO Delay Time (SCP→EIO)	t_{SE}	—	1	—	—	
EIO OUT Delay Time	t_{EOD}	(*7)	—	—	20	
Output Delay Time 1 (LP→OUT)	t_{pd1}	—	—	—	400	
Output Delay Time 2 (FR→OUT)	t_{pd2}	—	—	—	400	
Output Delay Time Variation	(*8)	—	—	—	0	30	

(*6) t_r, $t_f \le (t_C - t_{CWH} - t_{CWL})/2$ and t_r, $t_f \le 50ns$
(*7) $C_L = 10pF$
(*8) Variation between output pins in t_{pd1} or t_{pd2}.

TEST CONDITIONS (2) (V_{SS} = 0V, V_{DD} = 2.7 to 4.5V, V_{CC} = 14 to 42V, Ta = −20 to 75°C)

ITEM	SYMBOL	TEST CONDITION	MIN	TYP.	MAX	UNIT
Clock Cycle	t_C	—	80	—	—	ns
SCP Pulse Width	t_{CWH}, t_{CWL}	—	20	—	—	
Data Set-up Time	t_{DSU}	—	15	—	—	
Data Hold Time	t_{DHD}	—	10	—	—	
SCP Rise / Fall Time	t_r, t_f	—	—	—	(*9)	
LP Rise Time	t_{LRP}	—	15	—	—	
LP Fall Time	t_{LFP}	—	14	—	—	
LP Pulse Width	t_{LW}	—	14	—	—	
SCP-to-LP Delay Time	t_{SL}	—	2	—	—	
LP-to-SCP Delay Time	t_{LS}	—	14	—	—	
EIO IN Fall Time	t_{EIFP}	—	20	—	—	
EIO IN Pulse Width	t_{EIW}	—	14	—	—	
SCP-to-EIO Delay Time	t_{SE}	—	2	—	—	
EIO OUT Delay Time	t_{EOD}	(*10)	—	—	36	
Output Delay Time 1 (LP→OUT)	t_{pd1}	—	—	—	500	
Output Delay Time 2 (FR→OUT)	t_{pd2}	—	—	—	500	
Output Delay Time Variations	(*11)	—	—	0	50	

(*9) t_r, $t_f \leq (t_C - t_{CWH} - t_{CWL}) / 2$ and t_r, $t_f \leq 50$ns
(*10) C_L = 10pF
(*11) Variation between output pins in t_{pd1} or t_{pd2}.

NOTE

Insert the bypass capacitor (0.1μF) between V_{DD} and V_{SS}, and between V_{CC} and V_{SS} to decrease power supply noise.

Place the bypass capacitor as close to the LSI as possible.