TENTATIVE TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

T6K04

COLUMN ROW DRIVER LSI FOR A DOT MATRIX GRAPHIC LCD

The TOSHIBA T6K04 is a driver for a small or medium scale dot matrix graphic LCD. It has a 8 bit interface circuit. It generates all timing signals for display with on-chip oscillator. It receives 8 bit data from a MPU, laches the data to on-chip RAM, and display the image on LCD (The data on the display RAM correspond to the dots of display.). It has 128 column driver outputs and 64 row driver outputs so as to drive 128 dots by 64 dots LCD on a single. The other functions, It has resistors to divide bias voltage, power supply OP-Amp, DC-DC converter (doubler, tripler, quadrupler) and contrast control circuit so as to drive LCD with a single power supply.

Unit : mm

T6K04	LEAD PITCH	
	IN	OUT
(UAW, 5NS)	0.6	0.23

Please contact with TOSHIBA Agents for each Packaging Outline Dimensions.

TCP (Tape Carrier Package)

FEATURES

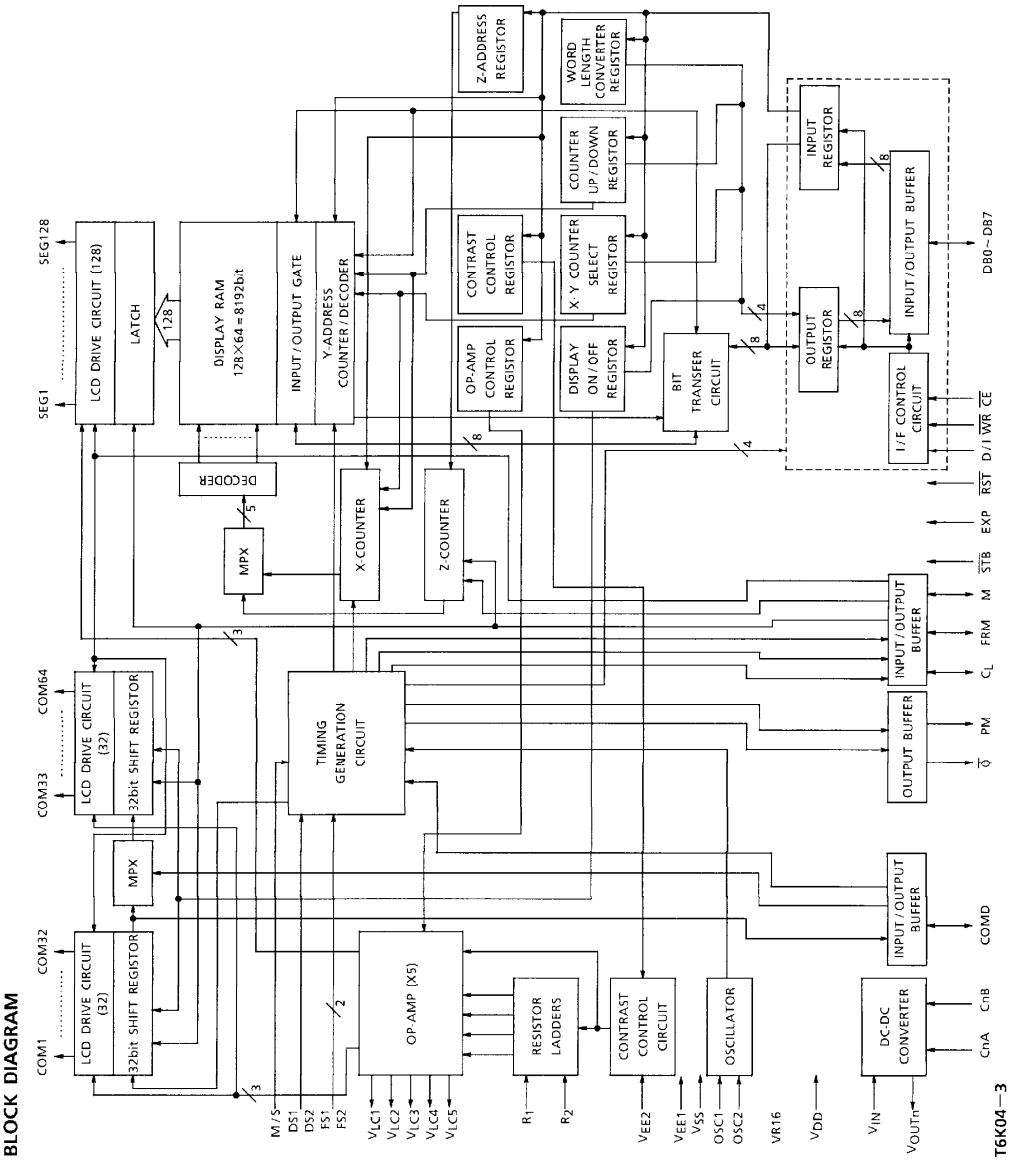
- On-chip display RAM Capacity : 128 × 64 = 8192 bit
- Display RAM data
  - ① Display data = "1" ..... LCD turn on.
  - ② Display data = "0" ..... LCD turn off.
- 1/32, 1/48, 1/56, 1/64 duty cycle
- Word length of display data can changed 8bit/word or 6bit/word in compliance with a character font.
- LCD driver outputs 128 column driver outputs and 64 row driver outputs.
- Interfacing with 80 series MPU.

E

Polyimide base film is hard and thin. Be careful not to injure yourself on the film or to scratch any other parts with the film. Try to design and manufacture products so that there is no chance of users touching the film after assembly, or if they do, that there is no chance of them injuring themselves. When cutting out the film, try to ensure that the film shavings do not cause accidents. After use, treat the leftover film and reel spacers as industrial waste.

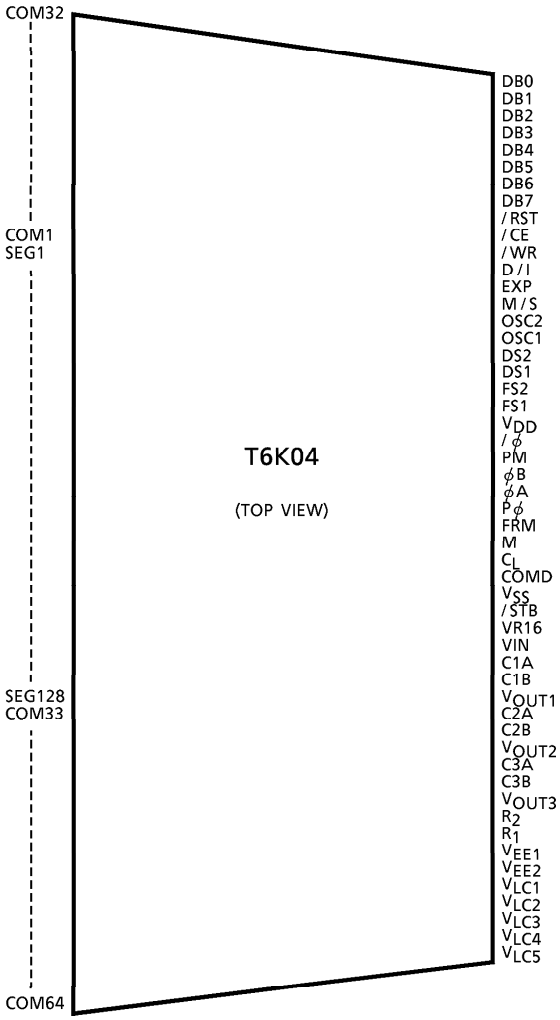
- On-chip oscillator with one external resistor.
- Low power consumption
- On-chip resistors to divide bias voltage, on-chip OP-Amp for LCD supply, on-chip DC-DC converter, on-chip contrast control circuit.
- CMOS process.
- Operating voltage expect LCD drive signal : 2.7~5.5 V
- Operating voltage of LCD drive signal.
  Must maintain V_{DD}-$V_{EE1} \leqq 16.5$ V, V_{DD}-$V_{EE2} \leqq 16.5$ V, $V_{EE1} \leqq V_{EE2}$
- Package : TCP

BLOCK DIAGRAM



T6K04—3

PIN CONFIGURATION



(*) : Above drawing describes pin configuration of the LSI Chip, it doesn't define the tape carrier package.

PIN FUNCTION

PIN NAME	I/O	FUNCTION
SEG1~SEG128	O	Column driver output
COM1~COM64	O	Row driver output
C_L	I/O	Input/Output for shift clock pulse ● Master mode (M/S = "H") → Output ● Slave mode (M/S = "L") → Input
M	I/O	Input/Output for frame signal ● Master mode (M/S = "H") → Output ● Slave mode (M/S = "L") → Input
FRM	I/O	Input/Output for display synchronous signal ● Master mode (M/S = "H") → Output ● Slave mode (M/S = "L") → Input
Pϕ, ϕA, ϕB	I/O	Input/Output system clock signal ● Master mode (M/S = "H") → Output ● Slave mode (M/S = "L") → Input
COMD	I/O	Input/Output row signal data ● Master mode (M/S = "H") → Output ● Slave mode (M/S = "L") → Input
DB0~DB7	I/O	Data bus
D/I	I	Input for Data/Instruction select signal ● D/I = "H" → Indicates that the data of DB0 to DB7 is the display data ● D/I = "L" → Indicates that the data of DB0 to DB7 is the control data
/WR	I	Input for write select signal ● /WR = "H" → Selected read ● /WR = "L" → Selected write
/CE	I	Input for chip enable signal ● At write → Data of DB0 to DB7 is latched at the rising edge of /CE
/RST	I	Input for reset signal ● /RST = "L" → State of reset
/STB	I	Input for standby signal ● Usually connect to V_{DD} ● /STB = "L" → T6K04 is the state of standby and it cannot accept the command or data Column driver signal and row driver signal is V_{DD} level
FS1, FS2	I	Input for frequency selects

<table>
<tr><th>PIN NAME</th><th>I/O</th><th>FUNCTION</th></tr>
<tr><td>EXP</td><td>I</td><td>Input for expansion mode selects
● M/S = "H" → Enable expansion mode, it can be used in two chip
● M/S = "L" → Disable expansion mode</td></tr>
<tr><td>M/S</td><td>I</td><td>Input for Master/Slave selects
● M/S = "H" → T6K04 is master chip
● M/S = "L" → T6K04 is slave chip</td></tr>
<tr><td>OSC1, OSC2</td><td>—</td><td>When using a internal clock oscillator, connect a resistor between OSC1 and OSC2.
When using external clock, input the clock to OSC1.</td></tr>
<tr><td>R_1, R_2</td><td>—</td><td>Input for LCD drive bias selects
● LCD drive bias is shown in the table as follows.
<table>
<tr><th>R_2</th><th>R_1</th><th>Bias</th></tr>
<tr><td>0</td><td>0</td><td>1/6</td></tr>
<tr><td>0</td><td>1</td><td>1/7</td></tr>
<tr><td>1</td><td>0</td><td>1/8</td></tr>
<tr><td>1</td><td>1</td><td>1/9</td></tr>
</table></td></tr>
<tr><td>DS1, DS2</td><td>I</td><td>Input for duty selects
● LCD drive duty is shown in the table as follows.
<table>
<tr><th>DS1</th><th>DS2</th><th>DUTY</th></tr>
<tr><td>0</td><td>0</td><td>1/32 duty</td></tr>
<tr><td>0</td><td>1</td><td>1/48 duty</td></tr>
<tr><td>1</td><td>0</td><td>1/56 duty</td></tr>
<tr><td>1</td><td>1</td><td>1/64 duty</td></tr>
</table></td></tr>
<tr><td>V_{IN}</td><td>—</td><td>Power supply for DC-DC converter. Normaly connect to V_{SS}.</td></tr>
<tr><td>C1A, C1B</td><td>—</td><td>Connect with capacitance for doubler</td></tr>
<tr><td>V_{OUT1}</td><td>—</td><td>DC-DC converter output (×2 level)</td></tr>
<tr><td>C2A, C2B</td><td>—</td><td>Connect with capacitance for tripler</td></tr>
<tr><td>V_{OUT2}</td><td>—</td><td>DC-DC converter output (×3 level)</td></tr>
<tr><td>C3A, C3B</td><td>—</td><td>Connect with capacitance for quadrupler</td></tr>
<tr><td>V_{OUT3}</td><td>—</td><td>DC-DC converter output (×4 level)</td></tr>
<tr><td>V_{EE1}, V_{EE2}</td><td>—</td><td>Power supply for LCD driver circuit.
● When using on-chip DC-DC converter, connect $V_{EE}1$, 2 to V_{OUT}</td></tr>
<tr><td>V_{LC1}~V_{LC5}</td><td>—</td><td>Power supply for LCD driver circuit.
● M/S = "H" → bias voltage output
● M/S = "L" → bias voltage input</td></tr>
<tr><td>VR16</td><td>O</td><td>Don't connect it.</td></tr>
<tr><td>V_{DD}</td><td>—</td><td>Power supply for logic circuit.</td></tr>
<tr><td>V_{SS}</td><td>—</td><td>Ground : Reference</td></tr>
<tr><td>PM</td><td>O</td><td>Pre-frame signal</td></tr>
<tr><td>/ϕ</td><td>O</td><td>Output system clock</td></tr>
</table>

FUNCTION OF EACH BLOCK

- Interface logic

  The T6K04 can be operated with 80 series MPU.
  Fig.1 shows an example of interface.

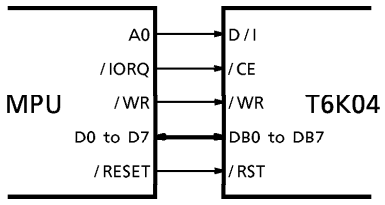


Fig.1

- Input register

  The register stores 8 bit data from MPU. D/I signal discriminate between command data and display data.

- Output register

  This register stores 8 bit data from the display RAM. When display data is read, the display data specified by the address of Address Counter is set in this register. After that, the address is automatically incremented or decremented. Therefore, when an address is set, the correct data does not appear at the first data read. The data at a specified address appears at the second data read.

- X-address counter

  X-address counter is 64-Up/Down counter. It holds the row address for the display RAM. Then it is selected by the command, writing to or reading the data of display RAM causes the X-address to automatically increment or decrement.

- Y (Page) -address counter

  The Y (Page) -address counter is changed by word length of the display data. In case of 8 bits per word, it is 16-Up/Down counter. And in case of 6 bits per word, it is 22-Up/Down counter. It holds the column address for the display RAM. This counter is selected by the command. Writing to or reading the display RAM causes the Y-address to automatically increment or decrement.

- Z-address counter

  The Z-address counter is 64-Up counter that provide the display RAM data for the LCD drive circuit. The data stored in Z-Address Register is send to Z-Address counter as Z start address.
  For instance, when Z start address is 16, the counter increment like this : 16, 17, 18···, 62, 63, 0, 1, 2···14, 15, 16. Therefore, the display start line is 16-line of the display RAM.

- Up/Down register

  The 1bit data stored in this register selects Up or Down mode of X and Y (Page) -address counter.

●Counter select resister

The 1 bit data stored in this register selects X-address counter or Y (Page) -address counter.

- Display ON / OFF register

  This 1 bit register holds the display ON or OFF state. In the OFF state, the output data turn to V_{DD} level. In the On state, the display data appears according to the display RAM data. The display ON or OFF state does not affect the data of display RAM.

- Z-address register

  This 6 bit register holds the data that indicates the display start line.

- Word length register

  The 1 bit data stored in this register selects the word length, 8 bits per word or 6 bits per word.

- Word length change circuit

  This circuit is controlled by the word length register. In case of 8 bits per word, data is transferred by 8 bits. In case of 6 bits per word, the way of data transfer is show in Fig.2 as follows.

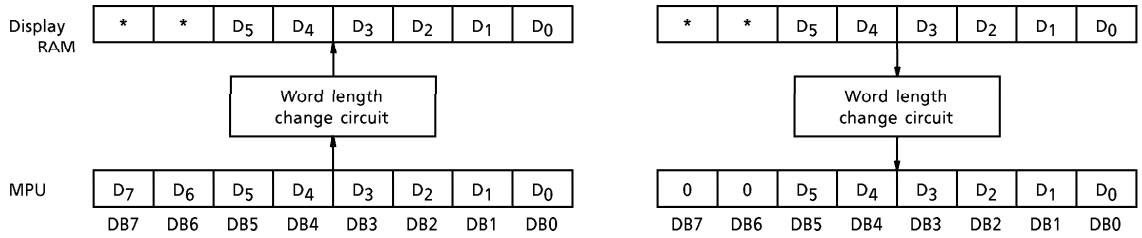


Fig.2

- Oscillator

  The T6K04 has an on-chip oscillator. When using this oscillator, connect an external resistor between OSC1 and OSC2, when using external clock, input the clock to OSC1 and open OSC2, as shown in Fig.3.

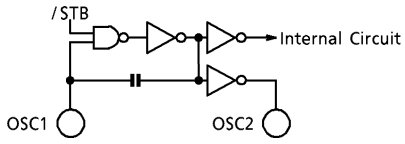


Fig.3

- Timing generation circuit

  The circuit divides the signals from the oscillator and generates display timing signals and operating clock.

- Shift-register

  The T6K04 has two 32 bit shift-register. These shift-register construct 64 bits shift-register.

- Latch circuit

  This latch circuit latches the data from the display RAM.

- Column driver circuit

  Column driver circuit consists of 128 driver circuits. One of the four LCD driving level is selected by the combination of M (internal signal) and the display data transferred from the latch circuit. Details of column driver circuit are shown in Fig.4.

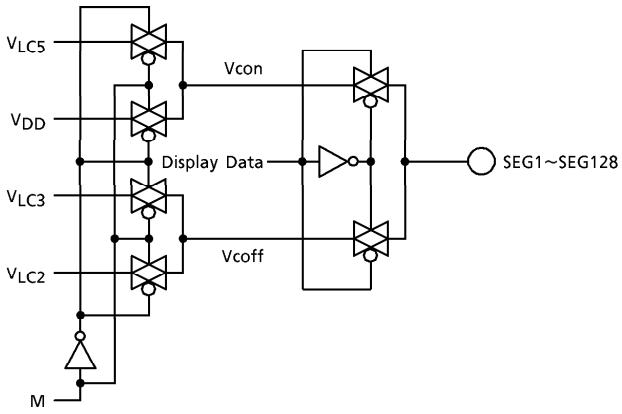


Fig.4

- Row driver circuit

  Row driver circuit consists of 64 drive circuits. One of the four LCD driving level is selected by the combination of M (internal signal) and the data from the sift register. Details of row driver circuit are shown in Fig.5.

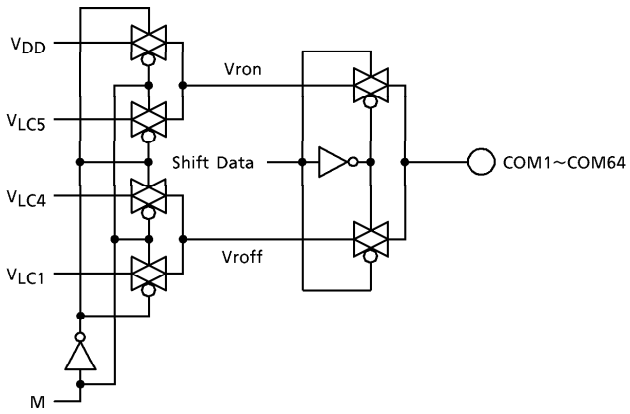


Fig.5

- DC-DC converter

  The T6K04 has an on-chip DC-DC converter. The DC-DC converter generates ×2 (V_{IN} × 2) level, ×3 (V_{IN} × 3) level and ×4 (V_{IN} × 4) level. See Fig.6
  When STB = L, V_{OUT1}, V_{OUT2} and V_{OUT3} = 0 (V).
  Recommended value of the capacitance is 1.0 μF.

Doubler (×2) mode

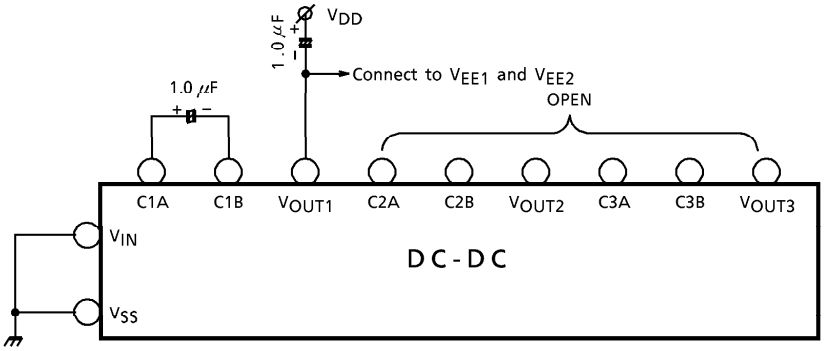


Fig.6 (1)

Tripler (×3) mode

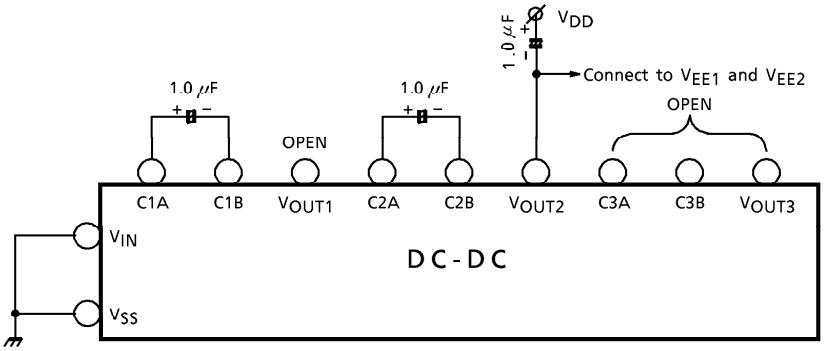


Fig.6 (2)

Quadrupler (×4) mode

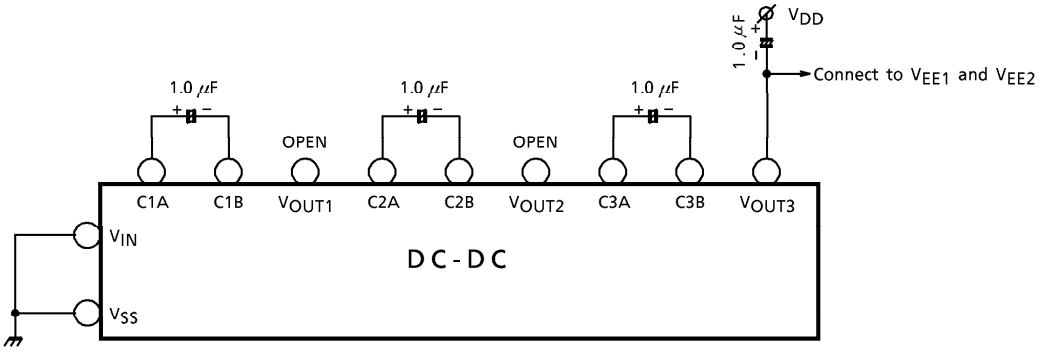


Fig.6 (3)

When using external power supply, input the voltage to V_{EE1} and V_{EE2} and Unconnect the capacitance.

- Voltage divider resistors, contrast control circuit

  The T6K04 has on-chip resistors to divide bias voltage with OP-Amp., and a contrast control circuit. The voltage bias is changed by the value of R_1 and R_2. Details of resisters to divide bias voltage and contrast control circuit are shown in Fig.7 as follows.

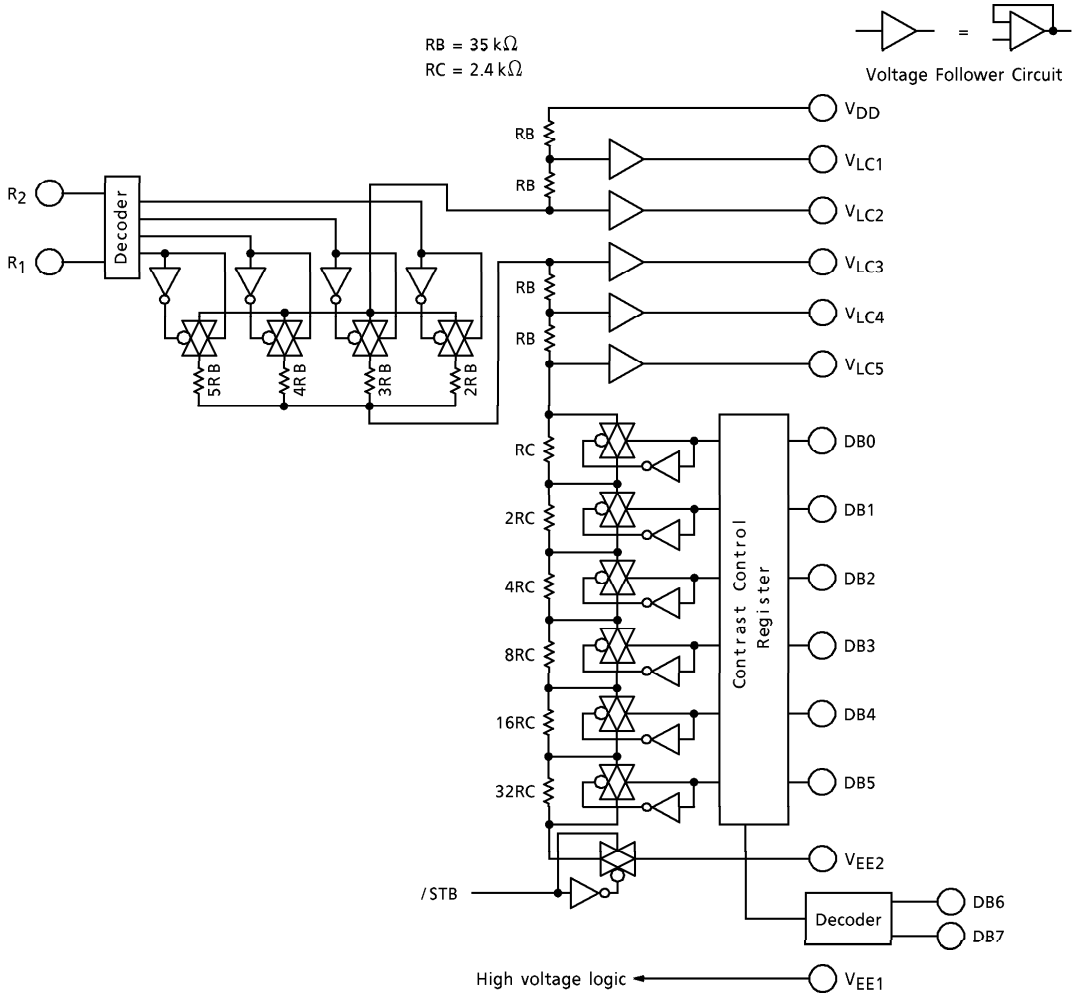


Fig.7

- OP-Amp., OP-Amp. control register

  The T6K04 has 5 operational amplifier for supplying LCD driving levels. Power supplying ability of these OP-Amp. are controlled by the contents of OP-amp. control register so as to match for various LCD panels. And, as the other way of controlling operational amplifier, there are the way that ability of operation amplifier is maximum on a short period from the rising edge of SEG signal and the ability is down on the other period.

- Display RAM

  The display RAM consists of 64 (row) × 128 (column) cells. It is 8192 bits. It is directly bit mapped to the LCD. The relation of display RAM to LCD is shown in Fig.8.
  When selecting 8 bits per word mode, the display RAM is arranged as 16 pages and each page contains 48 words. When selecting 6 bits per word mode, the display RAM is arranged as 22 pages and each page contains 34 words. See Fig.9.

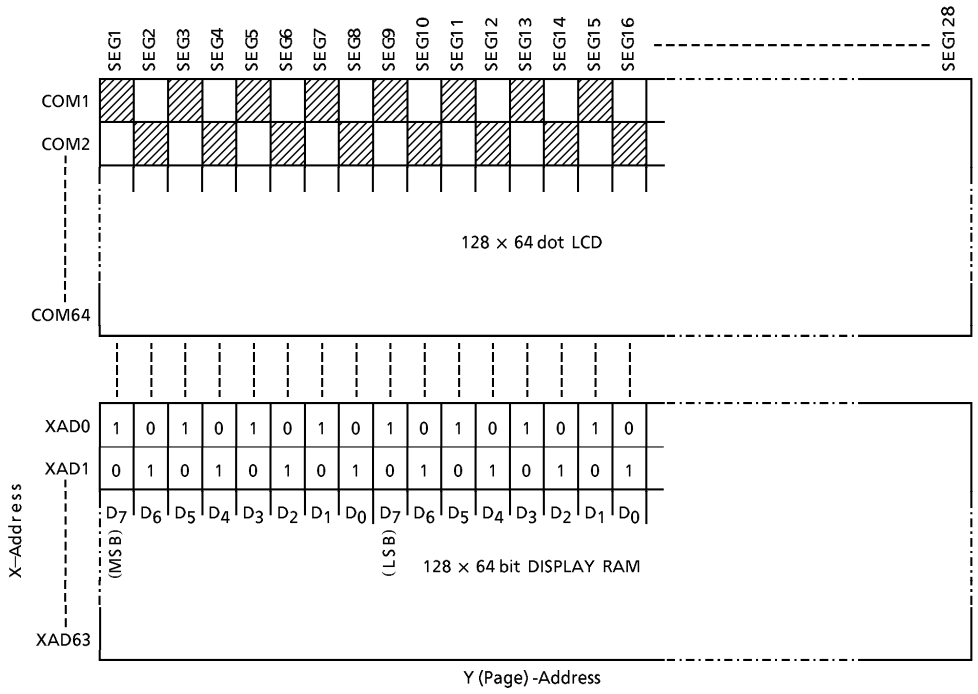
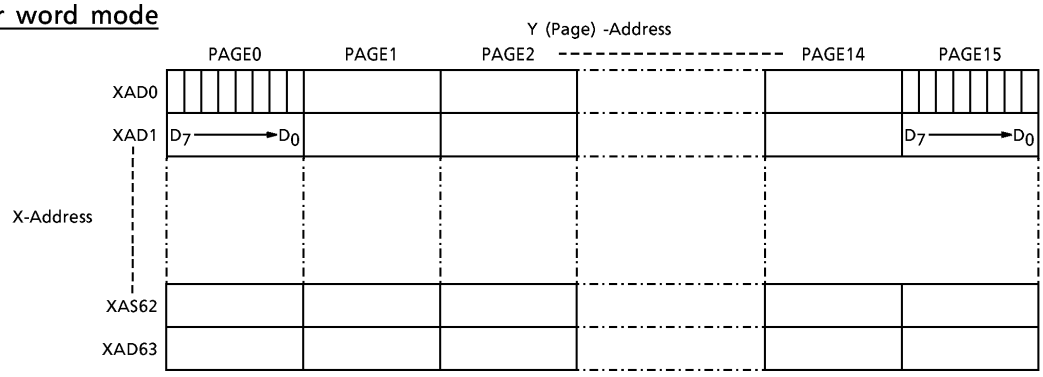


Fig.8

8 bits per word mode



6 bits per word mode

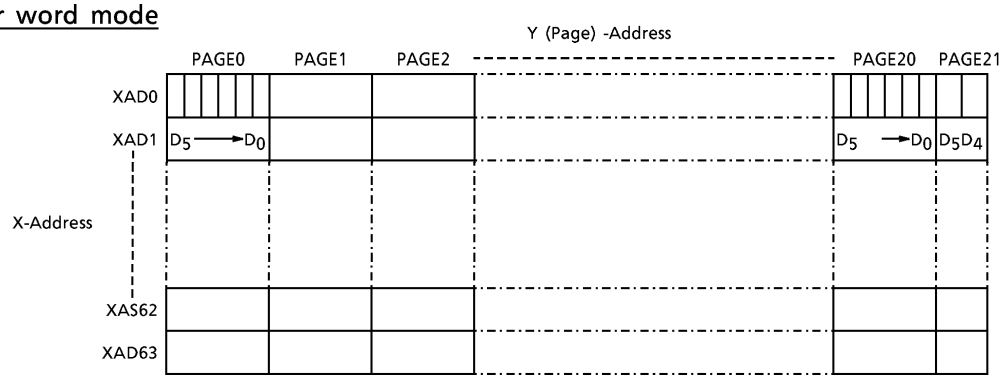


Fig.9

COMMAND DEFINITIONS

COMMAND NAME	D / I	/ WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	FUNCTION
86E	0	0	0	0	0	0	0	0	0	1 / 0	Word Length 8 bit / 6 bit
DPE	0	0	0	0	0	0	0	0	1	1 / 0	Display ON / OFF
UDE	0	0	0	0	0	0	0	1	1 / 0	1 / 0	Counter Select : DB1 Y (1) / X (0) Mode Select : DB0 UP (1) / DOWN (0)
CHE	0	0	0	0	0	1	1	*	*	*	Test Mode Select
OPA1	0	0	0	0	0	1	0	1 / 0	1 / 0	1 / 0	Ability of Op-Amp Control 1
OPA2	0	0	0	0	0	0	1	0	1 / 0	1 / 0	Ability of Op-Amp Control 2
SYE	0	0	0	0	1	Y-Address (0~21)					Y (Page) -Address Set
SZE	0	0	0	1	Z-Address (0~63)						Z-Address Set
SXE	0	0	1	0	X-Address (0~63)						X-Address Set
SCE	0	0	1	1	CONTRAST CONTROL (0~63)						Contrast Set
STRD	0	1	B	8 / 6	D	R	OP	0	Y / X	U / D	Status Read
DAWR	1	0	Write Data								Display Data Write
DARD	1	1	Read Data								Display Data Read

* : INVALID

- Display ON / OFF select (DPE)

D / I	/ WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	0	0	1	0

Display ON (03H)
Display OFF (02H)

This command controls display ON / OFF. It does not affect the data of the display RAM. When input the display OFF command, V_{LC1}~V_{LC5} is all V_{DD} level.

(Note) : Inputting "L" level to / RST makes display OFF.

- Word length 8 bits / 6 bits select (86E)

D / I	/ WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	0	0

Word Length 8 bits / Word mode (01H)
Word Length 6 bits / Word mode (00H)

This command set up 8 bits per word or 6 bits per word of the display RAM data.

(Note) : Inputting "L" level to / RST makes word length 8 bits per word.

- X / Y (Page) counter, Up / Down mode select (UDE)

D / I	/ WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	0	0
0	0	0	0	0	0	0	1	0	1
0	0	0	0	0	0	0	1	1	0
0	0	0	0	0	0	0	1	1	1

X-Counter / Down mode (04H)
X-Counter / Up mode (05H)
Y-Counter / Down mode (06H)
Y-Counter / Up mode (07H)

This command selects the counter and UP / DOWN mode. For instance, when selecting X-counter / UP mode, X-address is increment in response to every data reading and writing. But when X-Counter / UP mode is selected, The address of Y (Page) -counter will not change. So setting Y-address (by command SYE) is needed before changing Y-address.

(Note) : When Inputting "L" level to / RST, Y-counter is selected UP mode.

- Test mode select (CHE)

D / I	/ WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	1	*	*	*

This command selects the test mode. Don't use this command.

- Y (Page) -address set (SYE)

D / I	/ WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	A	A	A	A	A

Set Up Range : 8 bit / WORD : 20H to 2FH (0 Page to 15 Page)
6 bit / WORD : 20H to 35H (0 Page to 21 Page)

When operating in 8 bits per word mode, this command selects one of the 16 pages from the display RAM. (Don't instruct more than 9th page.) When operating in 6 bits per word mode, this command selects one of the 22 pages from the display RAM.

(Note) : When inputting "L" level to $\overline{RST}$, Y-address is set up as 0 page.

- Z-Address set (SZE)

D / I	/ WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	A	A	A	A	A	A

Set Up Range : 40H to 7FH (ZAD0 to ZAD63)

This command set a voluntary X-address of the display RAM as the top row of LCD screen.
For instance, when Z-address is 16, the top row of LCD screen is 16 (X) address of the display RAM, and the bottom row of LCD screen is 15 (Z) address of the display RAM.

(Note) : When inputting "L" level to $\overline{RST}$, X-address is set up as 0 page.

- X-Address set (SXE)

D / I	/ WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	A	A	A	A	A	A

Set Up Range : 80H to BFH (XAD0 to XAD63)

This command set X-address (0 to 63). When inputting "L" level to $\overline{RST}$, X-address is set up as 0 address.

- Contrast set (SCE)

D / I	/ WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	A	A	A	A	A	A

Set Up Range : C0H to FFH

This command set the contrast of LCD. The contrast of LCD are 64 steps and command C0H is the brightest or command FFH is the darkest.

- OP-Amp control 1 (OPA1)

D / I	/ WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	0	A	A	A

Set Up Range : 14H to 17H

This command set the power supplying ability of operational amplifier. This command selects one of four steps of ability. 14H of this command corresponds to maximum ability and 17H corresponds to minimum. This command can turn off OP-Amp by inputting "0" to DB2.

(Note) : When inputting "L" level to $\overline{RST}$, OP-Amp. is set up to minimum ability and OP-Amp ON.

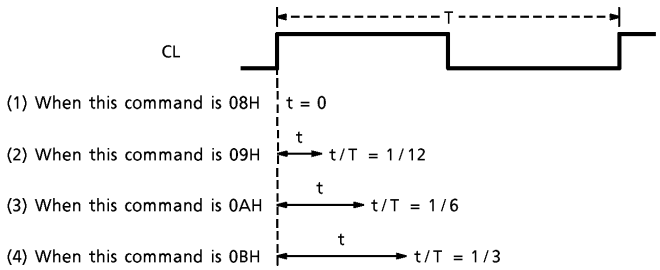
- OP-Amp control 2 (OPA2)

D / I	/ WR	/ RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	0	1	0	A	A

Set Up Range : 08H to 0BH

This command enhances the power supplying ability of OP-Amp in a shot period from the rising edge of CL signal. This command selects one of four steps of ability.

(Note) : When inputting "L" level to $\overline{RST}$, OP-Amp. is set up as t = 0. See Fig.10



The ability of operation amplifier is enhanced on the period (⇔on Fig.10) from the rising edge CL signal.

Fig.10

- Status read (STRD)

D/I	/WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	B	8/6	D	R	OP	0	Y/X	U/D

B (Busy) : When B = "1", the T6K04 is executing an internal operation and no instruction will be accepted except STRD.
When B = "0", the T6K04 can accept an instruction.

8/6 (Word Length) : When 8/6 = "1", Word Length of the display data is 8 bits per word.
When 8/6 = "0", Word Length of the display data is 6 bits per word.

D (Display) : When D = "1", display ON
When D = "0", display OFF

R (Reset) : When R = "1", the T6K04 is in reset state.
When R = "0", the T6K04 is operating state.

OP (OP-Amp) : When OP = "1", OP-Amp ON
When OP = "0", OP-Amp OFF

Y/X (Counter) : When Y/X = "1", Y counter is selected.
When Y/X = "0", X counter is selected.

U/D (UP/DOWN) : When U/D = "1", X and Y counter are up mode.
When U/D = "0", X and Y counter are down mode.

- Write/read display data (DAWR/DARD)

D/I	/WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D	D	D	D	D	D	D	D
1	1	D	D	D	D	D	D	D	D

DAWR : Display Data Write
DARD : Display Data Read

The command DAWR writes the display data to the display RAM. The command DARD output the display data from the display RAM. But, In case of executing data read, the correct data not appear at the first data reading. Therefore, be careful that the T6K04 needed dummy data read before the data reading.

DETAIL OF PERFORMANCE

- X-address counter and Y (Page) -address counter

Fig.11 shows a sample operating procedure for the X-address counter.
After Reset is executed, X-address becomes XAD = 0, then select X-counter / UP mode. Next set the X-address to 62 by commanding SXE.
After data has been written to or read, the X-address is automatically incremented by one.
After X-counter / Down mode has been selected and data has been written to or read, the X-address is automatically decremented by one.
When the X-counter is selected, Y-counter does not count up or down.

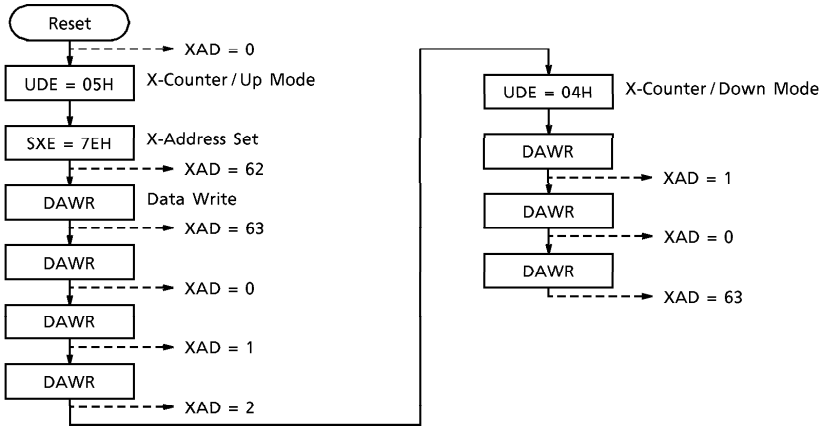


Fig.11

Fig.12 shows a sample operating procedure for the Y-address counter in the 8bits words length mode.
After Reset is executed, Y (Page) -address becomes Page = 0, then select Y (Page) -Up mode and 8bits words length mode. After data has been written to or read, the Y (Page) -address counter is automatically incremented by one.
After Y (Page) -counter / Down mode has been selected and data has been written to or read, the Y (Page) -address is automatically decremented by one.
When the Y (Page) -counter is selected, X-counter doesn't count up or down.

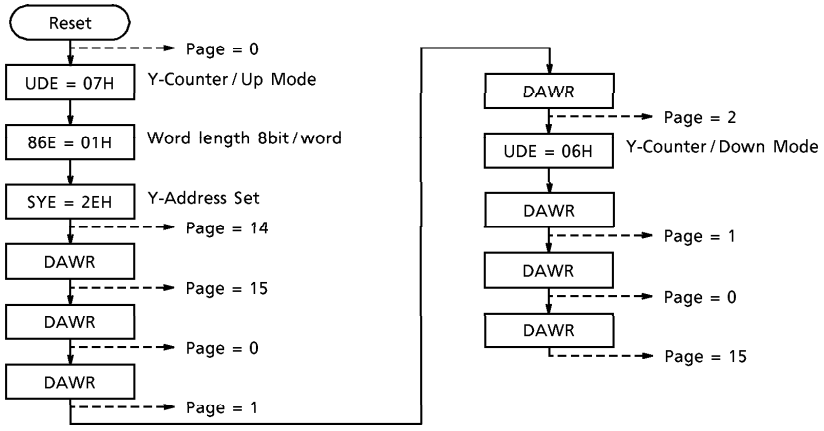


Fig.12

When operating in 6bits mode length mode, Y (Page) -address counter becomes 22 counter.
In Up-mode and Page = 21, after data has been written to or read, Y (Page) -address becomes Page = 0.
In Down-mode and Page = 0, after data has been written to or read, Y (Page) -address becomes Page = 21.

- Data read

When reading data, there are some occasions that dummy data read is needed. That is because when the data read command is written into, the data corresponding to address counter is moved to the Output Resister, and the contents of the output resister is transferred by the next data read command
Therefore when reading data next to power-on or next to address set (command SYE or SXE), dummy data read is needed. See Fig.13.

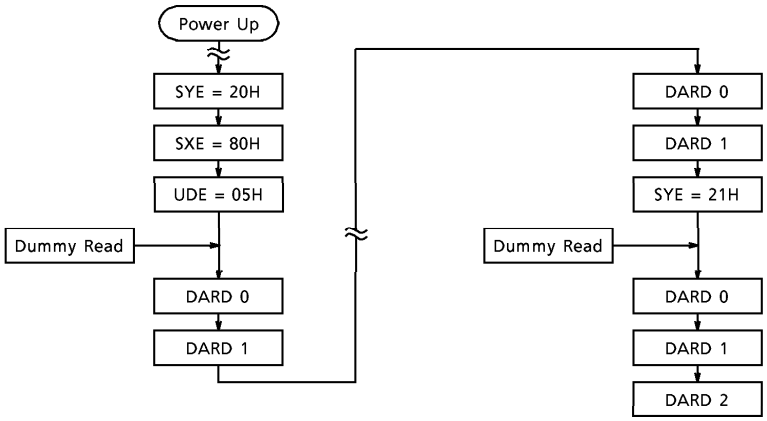


Fig.13

- Reset function

  When $\overline{RST}$ = L, reset function is executed and the following instruction are executed.

  - Display ..... OFF
  - Word length ..... 8 bit / Word
  - Counter mode ..... Y counter / Up mode
  - Y (Page) -address ..... Page = 0
  - X-address ..... Xad = 0
  - Z-address ..... Zad = 0
  - OP-Amp ..... ON
  - OPA1 ..... Min.
  - OPA2 ..... Min.
  - CONTRAST ..... Min. ($V_{LC5} = V_{EE1, 2}$)

- Stand-by function

  When $\overline{STB}$ = L, the T6K04 is in stand-by state. The internal oscillation is stopped, power consumption is reduced, and power supply for LCD (V_{LC1}~V_{LC5}) become V_{DD}.

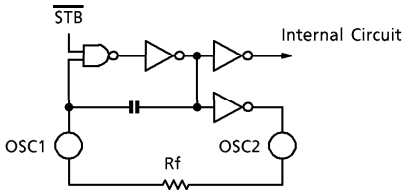
- Busy flag

  When the T6K04 is executing an internal operation (except command STRD), the busy flag is set at logical "H". The state of busy flag is output on data in response to the command STRD. During the busy flag is "H", no instruction will be accepted (except command STRD). The busy state period (T) is shown as follows.

  $2 / f_{OSC} \leqq T \leqq 4 / f_{OSC}$ [sec] f_{OSC} : Frequency of OSC1

- Oscillation frequency

  By using the frequency select pins (FS1, FS2), the T6K04 set the relation between oscillation frequency (f_{OSC}) and frame frequency (f_M).
  Next table shows the choice of the frequency select pins (FS1, FS2) and oscillation frequency to set f_{COM} = 35 (Hz). The resistance values are typical values. The oscillation frequency depends on the mounting condition. So it is necessary to adjust the oscillation frequency to a target value.



Rf (kΩ)	f_{OSC} (kHz)	f_{COM} (Hz)	FS1	FS2
1100	28.56	35	0	0
530	57.12	35	1	0
140	228.48	35	0	1
70	456.96	35	1	1

- Expansion function

The T6K04 has expansion function, when using this function, the T6A04 (2 chips) can drive 240 × 64 dots LCD panel (maximum).
Next table shows the selectable function by using M / S, EXP pins.

		M / S	
		"H"	"L"
EXP	"H"	• Two chips mode (Enable expansion mode) • Master chip COM1~COM64 are available.	• Two chips mode (Enable expansion mode) • Slave chip • COM1~COM64 are available. • Timing signals and power voltage are supplied from Master Chip.
	"L"	• One chip mode (Disable expansion mode) • COM1~COM64 are available.	• Do not select

Fig.13-1 and -2 illustrate the application example of Disable expansion mode and enable expansion mode.
In Enable Expansion Mode (Two chips mode)
As shown in Fig.13-2, Fig.14 Master chip supplies LCD drive signals and power voltage to Slave chip (The Oscillator, the timing circuits, Op-Amp. and Contrast control circuit are disabled)

(1) Disable expansion mode

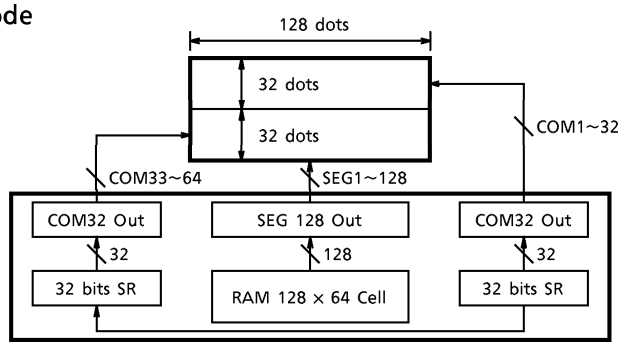


Fig.13-1

(2) Expansion mode

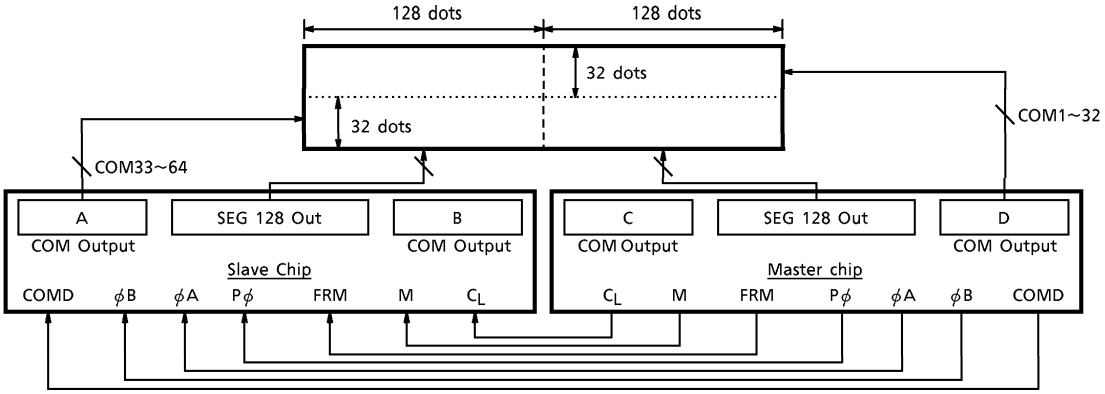


Fig.13-2

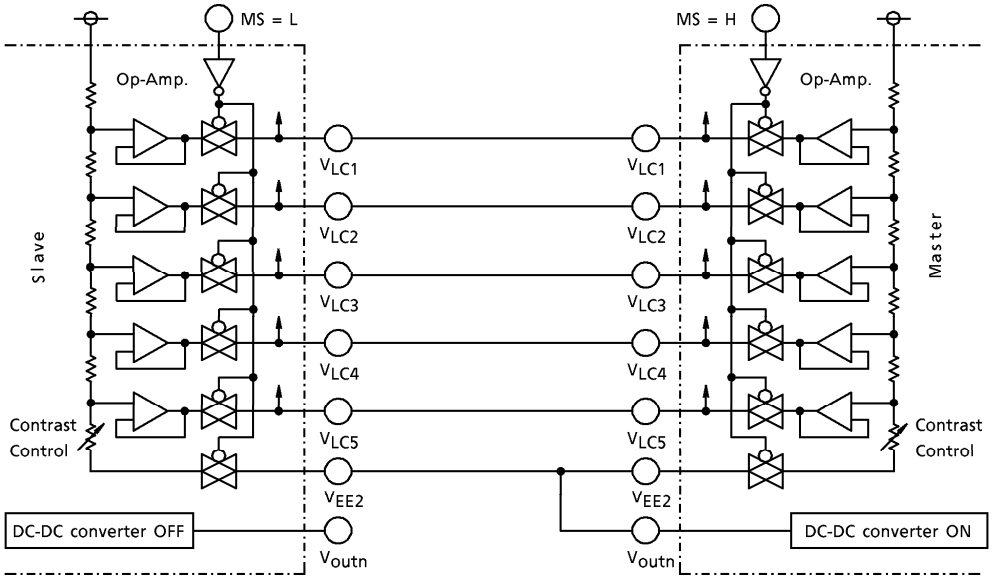
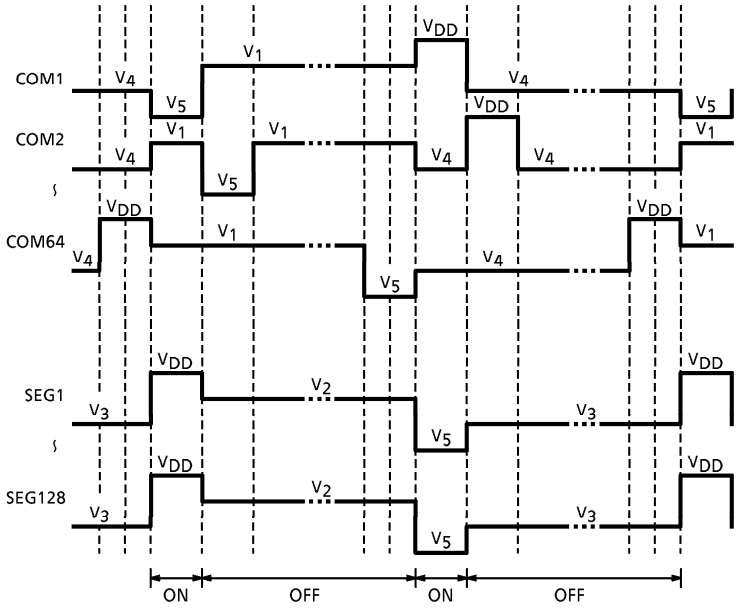


Fig.14

- **LCD DRIVER WAVEFORM**



LCD driver timing chart (1/64 duty)

MAXIMUM RATINGS (Ta = 25°C)

ITEM	SYMBOL	RATING	UNIT
Supply Voltage (1)	V_{DD} (Note 1)	−0.3~7.0	V
Supply Voltage (2)	$V_{LC1, 2, 3, 4, 5}$ V_{EE1}, V_{EE2}	V_{DD} − 18.0~V_{DD} + 0.3	V
Input Voltage	V_{INP} (Note 1, 2)	−0.3~V_{DD} + 0.3	V
Operating Temperature	T_{opr}	−20~75	°C
Storage Temperature	T_{stg}	−55~125	°C

(Note 1) : Referred to V_{SS} = 0 V
(Note 2) : Applied data bus terminals and Input terminals expect V_{EE1}, V_{EE2}, V_{LC1}, V_{LC2}, V_{LC3}, V_{LC4}, V_{LC5}.

ELECTRICAL CHARACTERISTICS (1)
(Test condition : If not specified, V_{SS} = 0 V, V_{DD} = 3.0 V ± 10%, V_{LC5} = 0 V, Ta = 25°C)

ITEM		SYMBOL	TEST CIR-CUIT	CONDITION	MIN.	TYP.	MAX.	UNIT	APPLICABLE TERMINAL
Operating Supply (1)		V_{DD}	—	—	2.7	—	3.3	V	V_{DD}, V_{IN}
Operating Supply (2)		V_{LC5} $V_{EE1, 2}$	—	—	V_{DD} − 16.5	—	V_{DD} − 4.0	V	V_{LC5}, V_{EE1}, V_{EE2}
Input Level	"H" Level	V_{IH}	—	—	0.8 V_{DD}	—	V_{DD}	V	DB0~7, D/I, /WR, ICE, /RST, /STB, M/S, EXP, CL, M, FRM, ϕA, ϕB, COMD, FS1, FS2, DS1, DS2, Pϕ
	"L" Level	V_{IL}	—	—	0	—	0.2V_{DD}	V	
Output Level	"H" Level	V_{OH}	—	I_{OH} = −400 μA	V_{DD} − 0.2	—	V_{DD}	V	DB0~DB7
	"L" Level	V_{OL}	—	I_{OL} = 400 μA	0	—	0.2	V	
Column Driver On Resistance		Rcol	—	V_{DD} − V_{LC5} = 11.0 V Load current = ±100 μA	—	—	7.5	kΩ	SEG1~SEG128
Row Driver On Resistance		Rrow	—	V_{DD} − V_{LC5} = 11.0 V Load current = ±100 μA	—	—	1.5	kΩ	COM1~COM64
Input Leakage		I_{IL}	—	V_{IN} = V_{DD}~GND	−1	—	1	μA	DB0~7, D/I, /WR, ICE, /RST, /STB, M/S, EXP, CL, M, FRM, ϕA, ϕB, COMD, FS1, FS2, DS1, DS2, Pϕ
Operating Freq		f_{OSC}	—	—	20	—	500	kHz	OSC1
External Clock Freq		f_{ex}	—	—	20	—	500	kHz	OSC1
External Clock Duty		f_{duty}	—	—	45	50	55	%	OSC1
External Clock Rise / Fall Time		t_r / t_f	—	—	—	—	50	ns	OSC1
Current Consumption (1)		I_{DD1}	—	—	—	300	420	μA	V_{DD} (Note 1)
Current Consumption (2)		I_{DD2}	—	—	—	400	530	μA	V_{DD} (Note 2)
Current Consumption (3)		I_{DDSTB}	—	—	−1	—	1	μA	V_{DD} (Note 3)
Output Voltage (Tripler Mode)		VO2	(2)	—	−4.50	−4.90	—	V	V_{OUT2} (Note 4)
Output Voltage (Quadruplexer Mode)		VO3	(3)	—	−6.75	−7.50	—	V	V_{OUT3} (Note 5)

(Note 1) : V_{DD} = 3.0 ± 10%, $V_{EE1, 2}$ = V_{OUT2} (Tripler mode), No data access
R_f = 62 kΩ, LCD out pin No Load, 1/9 bias, FS1, 2 = H, OP-Amp. = 14H/08H

(Note 2) : V_{DD} = 3.0 ± 10%, $V_{EE1, 2}$ = V_{OUT2} (Tripler mode), Data access cycle $f_{\overline{CE}}$ = 1 MHz,
R_f = 62 kΩ, LCD out pin No Load, 1/9 bias, FS1, 2 = H, OP-Amp. = 14H/08H

(Note 3) : V_{DD} = 3.0 ± 10%, V_{DD} − $V_{EE1, 2}$ = 16.0 V, /STB = L

(Note 4) : V_{DD} = 3.0 V, I_{Load} = 500 μA, $V_{EE1, 2}$ = −6.0 V (external power supply)
CnA − CnB = 1.0 μF, V_{DD} − V_{OUT2} = 1.0 μF, R_f = 62 kΩ, Ta = 25°C

(Note 5) : V_{DD} = 3.0 V, I_{Load} = 500 μA, $V_{EE1, 2}$ = −9.0 V (external power supply)
CnA − CnB = 1.0 μF, V_{DD} − V_{OUT3} = 1.0 μF, R_f = 62 kΩ, Ta = 25°C

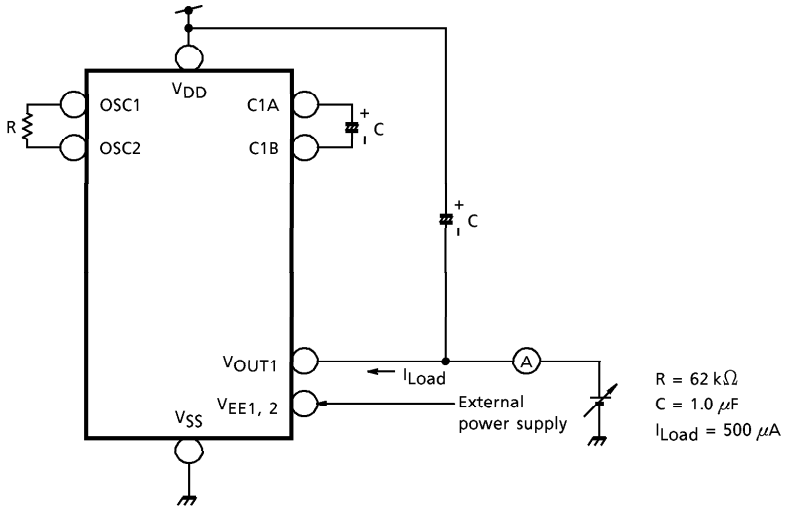
ELECTRICAL CHARACTERISTICS (2)
(Test condition : If not specified, V_{SS} = 0 V, V_{DD} = 5.0 V ± 10%, V_{LC5} = 0 V, Ta = 25°C)

ITEM		SYMBOL	TEST CIR-CUIT	CONDITION	MIN.	TYP.	MAX.	UNIT	APPLICABLE TERMINAL
Operating Supply (1)		V_{DD}	—	—	4.7	—	5.5	V	V_{DD}
Operating Supply (2)		V_{LC5} $V_{EE1, 2}$	—	—	V_{DD} − 16.5	—	V_{DD} − 4.0	V	V_{LC5}, V_{EE1}, V_{EE2}
Input Level	"H" Level	V_{IH}	—	—	0.7 V_{DD}	—	V_{DD}	V	DB0~7, D/I, /WR, ICE, /RST, /STB, M/S, EXP, CL, M, FRM, ϕA, ϕB, COMB, FS1, FS2, DS1, DS2, Pϕ
	"L" Level	V_{IL}	—	—	0	—	0.3V_{DD}	V	
Output Level	"H" Level	V_{OH}	—	I_{OH} = −400 μA	V_{DD} − 0.2	—	V_{DD}	V	DB0~DB7
	"L" Level	V_{OL}	—	I_{OL} = 400 μA	0	—	0.2	V	
Column Driver On Resistance		Rcol	—	V_{DD} − V_{LC5} = 11.0 V Load current = ±100 μA	—	—	7.5	kΩ	SEG1~SEG128
Row Driver On Resistance		Rrow	—	V_{DD} − V_{LC5} = 11.0 V Load current = ±100 μA	—	—	1.5	kΩ	COM1~COM64
Input Leakage		I_{IL}	—	V_{IN} = V_{DD}~GND	−1	—	1	μA	DB0~7, D/I, /WR, ICE, /RST, /STB, M/S, EXP, CL, M, FRM, ϕA, ϕB, COMB, FS1, FS2, DS1, DS2, Pϕ
Operating Freq		f_{OSC}	—	—	20	—	500	kHz	OSC1
External Clock Freq		f_{ex}	—	—	20	—	500	kHz	OSC1
External Clock Duty		f_{duty}	—	—	45	50	55	%	OSC1
External Clock Rise/Fall Time		t_r/t_f	—	—	—	—	50	ns	OSC1
Current Consumption (1)		I_{DD1}	—	—	—	510	640	μA	V_{DD} (Note 1)
Current Consumption (2)		I_{DD2}	—	—	—	620	830	μA	V_{DD} (Note 2)
Current Consumption (3)		I_{DDSTB}	—	—	−1	—	1	μA	V_{DD} (Note 3)
Output Voltage (Doubler Mode)		VO1	(1)	—	−4.25	−4.50	—	V	V_{OUT1} (Note 4)
Output Voltage (Tripler Mode)		VO2	(2)	—	−8.50	−9.00	—	V	V_{OUT2} (Note 5)

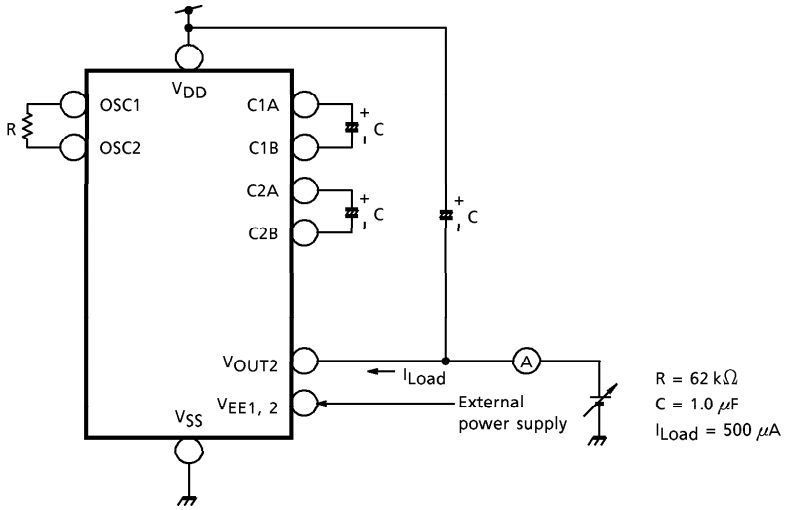
(Note 1) : V_{DD} = 5.0 ± 10%, $V_{EE1, 2}$ = V_{OUT1} (Doubler mode), No data access
R_f = 62 kΩ, LCD out pin No Load, 1/9 bias, FS1, 2 = H, OP-Amp. = 14H/08H
(Note 2) : V_{DD} = 5.0 ± 10%, $V_{EE1, 2}$ = V_{OUT1} (Doubler mode), Data access cycle $f_{\overline{CE}}$ = 1 MHz,
R_f = 62 kΩ, LCD out pin No Load, 1/9 bias, FS1, 2 = H, OP-Amp. = 14H/08H
(Note 3) : V_{DD} = 5.0 ± 10%, V_{DD}, /STB = L
(Note 4) : V_{DD} = 5.0 V, I_{Load} = 500 μA, $V_{EE1, 2}$ = −5.0 V (external power supply)
CnA − CnB = 1.0 μF, V_{DD} − V_{OUT1} = 1.0 μF, R_f = 62 kΩ, Ta = 25°C
(Note 5) : V_{DD} = 5.0 V, I_{Load} = 500 μA, $V_{EE1, 2}$ = −10.0 V (external power supply)
CnA − CnB = 1.0 μF, V_{DD} − V_{OUT2} = 1.0 μF, R_f = 62 kΩ, Ta = 25°C

TEST CIRCUIT

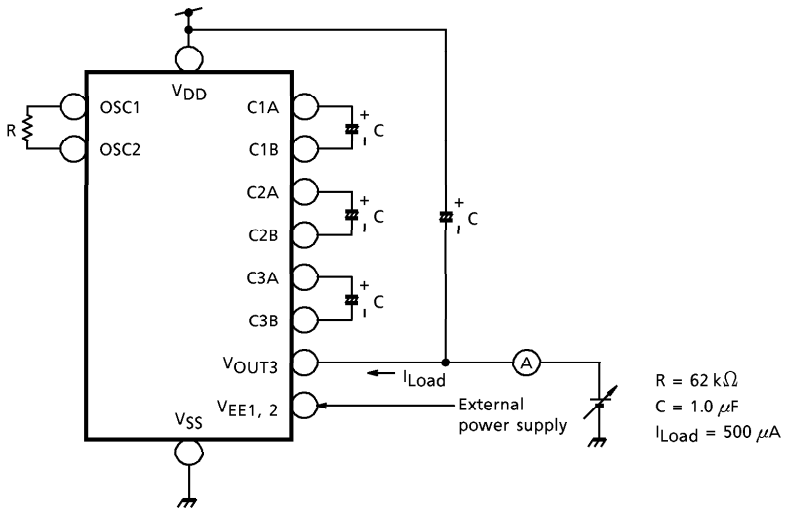
(1) Doubler mode



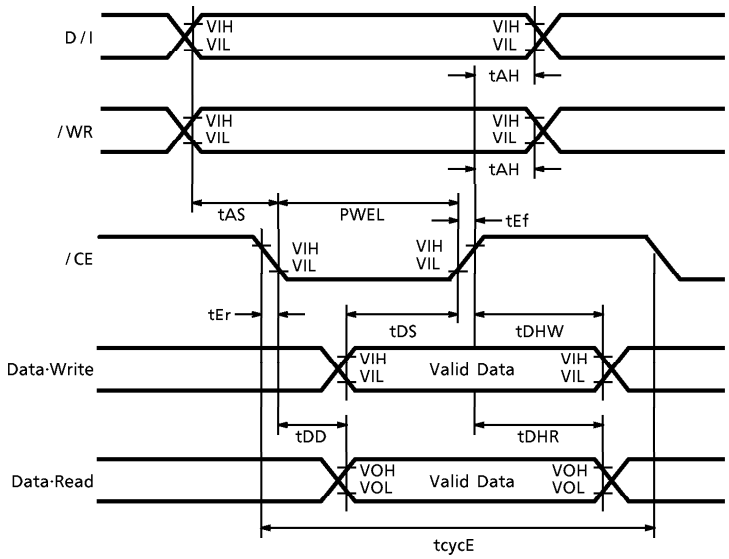
(2) Tripler mode



(3) Quadrupler mode



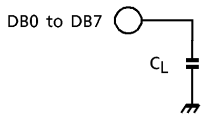
SWITCHING CHARACTERISTICS



(V_{SS} = 0 V, V_{DD} = 5.0 V ± 10%, V_{LC5} = 0 V, Ta = 25°C)

ITEM	SYMBOL	MIN.	MAX.	UNIT
Enable Cycle Time	tcycE	500		ns
Enable Pulse Width	PWEL	220		ns
Enable Rise / Fall Time	tEr, tEf		20	ns
Address Set-up Time	tAS	60		ns
Address Hold Time	tAH	0		ns
Data Set-up Time	tDS	60		ns
Data Hold Time	tDHW	10		ns
Data Delay Time	tDD (Note)		160	ns
Data Hold Time	tDHR (Note)	20		ns

LOAD CIRCUIT



C_L = 100 pF
(Including wiring capacity)

(V_{SS} = 0 V, V_{DD} = 3.0 V ± 10%, V_{LC5} = 0 V, Ta = 25°C)

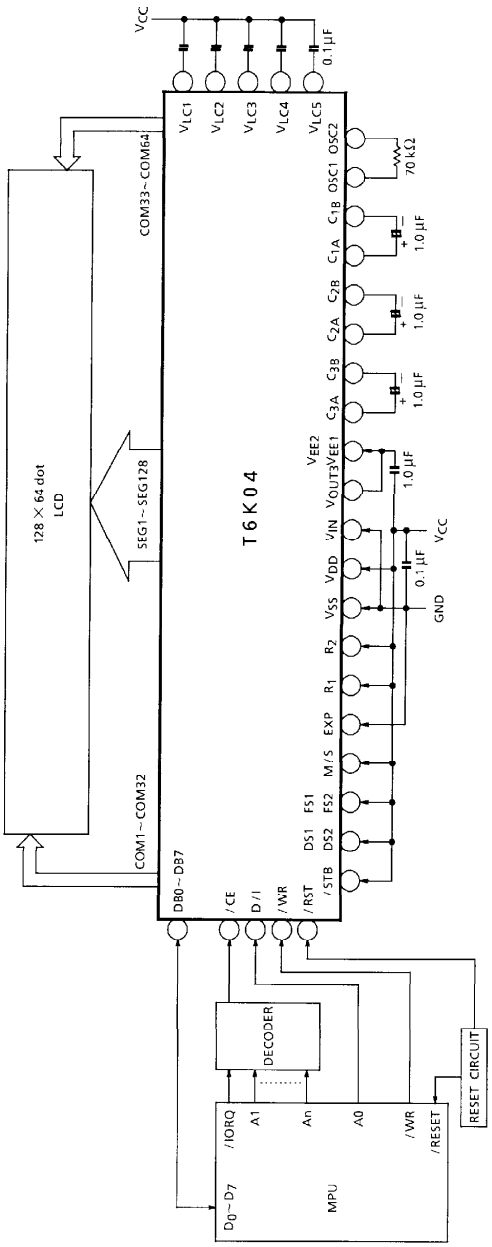
ITEM	SYMBOL	MIN.	MAX.	UNIT
Enable Cycle Time	tcycE	1000		ns
Enable Pulse Width	PWEL	450		ns
Enable Rise / Fall Time	tEr, tEf		25	ns
Address Set-up Time	tAS	100		ns
Address Hold Time	tAH	0		ns
Data Set-up Time	tDS	280		ns
Data Hold Time	tDHW	20		ns
Data Delay Time	tDD (Note)		350	ns
Data Hold Time	tDHR (Note)	20		ns

(Note) : Connect to Load circuit.

APPLICATION

(1) T6K04 One chip mode

- Oscillation frequency maxmum
- LCD drive bias 1 / 9
- Using DC-DC Converter



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