

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

# TC74VHCT74AF, TC74VHCT74AFN, TC74VHCT74AFT

## DUAL D - TYPE FLIP - FLOP WITH PRESET AND CLEAR

The TC74VHCT74 is an advanced high speed CMOS D - FLIP FLOP fabricated with silicon gate C<sup>2</sup>MOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The signal level applied to the D INPUT is transferred to Q OUTPUT during the positive going transition of the CK pulse.

CLR and PR are independent of the CK and are accomplished by setting the appropriate input low.

The input voltage are compatible with TTL output voltage.

This device may be used as a level converter for interfacing 3.3V to 5V system.

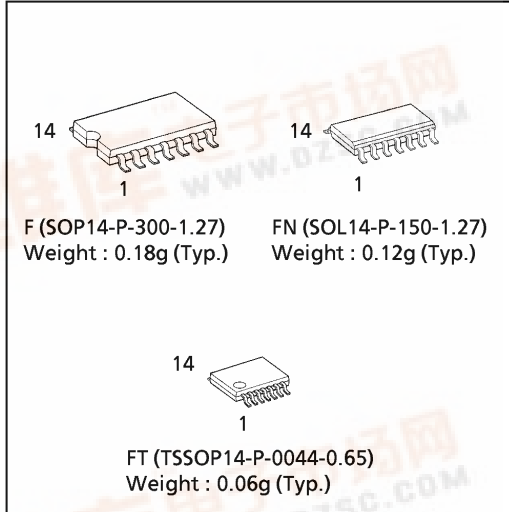
Input protection and output circuit ensure that 0 to 5.5V can be applied to the input and output\*1 pins without regard to the supply voltage. These structure prevents device destruction due to mismatched supply and input / output voltages such as battery back up, hot board insertion, etc.

\*1 : V<sub>CC</sub>=0V

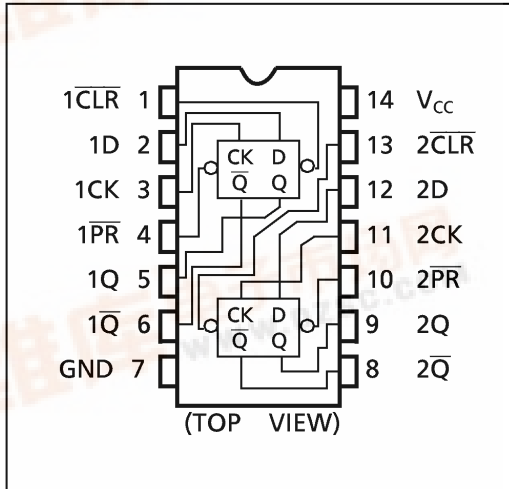
### FEATURES :

- High Speed ..... f<sub>MAX</sub> = 160MHz(typ.)  
at V<sub>CC</sub> = 5V
- Low Power Dissipation..... I<sub>CC</sub> = 2μA(Max.) at Ta = 25°C
- Compatible with TTL outputs ... V<sub>IL</sub> = 0.8V (Max.)  
V<sub>IH</sub> = 2.0V (Min.)
- Power Down Protection is provided on all inputs and outputs
- Balanced Propagation Delays..... t<sub>pLH</sub> ≈ t<sub>pHL</sub>
- Pin and Function Compatible with the 74 series (74AC / HC / F / ALS / LS etc.) 74 type.

(Note) The JEDEC SOP (FN) is not available in Japan.



### PIN ASSIGNMENT

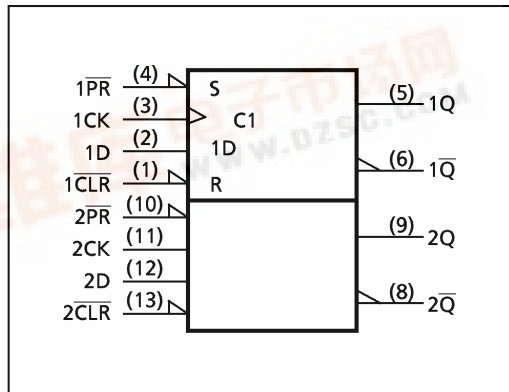


### TRUTH TABLE

INPUTS				OUTPUTS		FUNCTION
CLR	PR	D	CK	Q	Q̄	
L	H	X	X	L	H	CLEAR
H	L	X	X	H	L	PRESET
L	L	X	X	H	H	—
H	H	L	⏚	L	H	—
H	H	H	⏚	H	L	—
H	H	X	⏚	Q <sub>n</sub>	Q̄ <sub>n</sub>	NO CHANGE

X : Don't Care

### IEC LOGIC SYMBOL



980910EBA2

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## ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	$V_{CC}$	-0.5~7.0	V
DC Input Voltage	$V_{IN}$	-0.5~7.0	V
DC Output Voltage	$V_{OUT}$	-0.5~7.0 (Note 1)	V
		-0.5~ $V_{CC} + 0.5$ (Note 2)	
Input Diode Current	$I_{IK}$	-20	mA
Output Diode Current	$I_{OK}$	$\pm 20$ (Note 3)	mA
DC Output Current	$I_{OUT}$	$\pm 25$	mA
DC $V_{CC}$ /Ground Current	$I_{CC}$	$\pm 50$	mA
Power Dissipation	$P_D$	180	mW
Storage Temperature	$T_{stg}$	-65~150	$^{\circ}C$

(Note 1)  $V_{CC} = 0V$

(Note 2) High or Low State.  $I_{OUT}$  absolute maximum rating must be observed.

(Note 3)  $V_{OUT} < GND$ ,  $V_{OUT} > V_{CC}$

## RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	$V_{CC}$	4.5~5.5	V
Input Voltage	$V_{IN}$	0~5.5	V
Output Voltage	$V_{OUT}$	0~5.5 (Note 4)	V
		0~ $V_{CC}$ (Note 5)	
Operating Temperature	$T_{opr}$	-40~85	$^{\circ}C$
Input Rise and Fall Time	$dt/dV$	0~20	ns/V

(Note 4)  $V_{CC} = 0V$

(Note 5) High or Low State.

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**DC ELECTRICAL CHARACTERISTICS**

PARAMETER	SYMBOL	CONDITON		V <sub>CC</sub> (V)	Ta = 25°C			Ta = -40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V <sub>IH</sub>			4.5~5.5	2.0	—	—	2.0	—	V
Low - Level Input Voltage	V <sub>IL</sub>			4.5~5.5	—	—	0.8	—	0.8	V
High - Level Output Voltage	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -50μA	4.5	4.40	4.50	—	4.40	—	V
			I <sub>OH</sub> = -8mA	4.5	3.94	—	—	3.80	—	
Low - Level Output Voltage	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 50μA	4.5	—	0.0	0.1	—	0.1	V
			I <sub>OL</sub> = 8mA	4.5	—	—	0.36	—	0.44	
Input Leakage Current	I <sub>IN</sub>	V <sub>IN</sub> = 5.5V or GND		0~5.5	—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND		5.5	—	—	2.0	—	20.0	
		I <sub>CCT</sub>	PER INPUT : V <sub>IN</sub> = 3.4V OTHER INPUT : V <sub>CC</sub> or GND	5.5	—	—	1.35	—	1.50	mA
Output Leakage Current	I <sub>OPD</sub>	V <sub>OUT</sub> = 5.5V		0	—	—	0.5	—	5.0	μA

**TIMING REQUIREMENTS ( Input  $t_r = t_f = 3ns$  )**

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C		Ta = -40~85°C		UNIT
			V <sub>CC</sub> (V)	LIMIT	LIMIT	LIMIT	
Minimum Pulse Width (CK)	t <sub>W(L)</sub>		5.0 ± 0.5	5.0	5.0	5.0	ns
	t <sub>W(H)</sub>						
Minimum Pulse Width (CLR, PR)	t <sub>W(L)</sub>		5.0 ± 0.5	5.0	5.0	5.0	
Minimum Set-up Time	t <sub>s</sub>		5.0 ± 0.5	5.0	5.0	5.0	
Minimum Hold Time	t <sub>h</sub>		5.0 ± 0.5	0.0	0.0	0.0	
Minimum Removal Time (CLR, PR)	t <sub>rem</sub>		5.0 ± 0.5	3.5	3.5	3.5	

**AC ELECTRICAL CHARACTERISTICS ( Input  $t_r = t_f = 3ns$  )**

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C			Ta = -40~85°C		UNIT
		V <sub>CC</sub> (V)	CL (pF)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (CK - Q, Q)	t <sub>pLH</sub>	5.0 ± 0.5	15	—	5.8	7.8	1.0	9.0	ns
	t <sub>pHL</sub>		50	—	6.3	8.8	1.0	10.0	
Propagation Delay Time (CLR, PR - Q, Q)	t <sub>pLH</sub>	5.0 ± 0.5	15	—	7.6	10.4	1.0	12.0	
	t <sub>pHL</sub>		50	—	8.1	11.4	1.0	13.0	
Maximum Clock Frequency	f <sub>MAX</sub>	5.0 ± 0.5	15	100	160	—	80	—	MHz
			50	80	140	—	65	—	
Input Capacitance	C <sub>IN</sub>			—	4	10	—	10	pF
Power Dissipation Capacitance	C <sub>PD</sub>	(Note 6)		—	24	—	—	—	

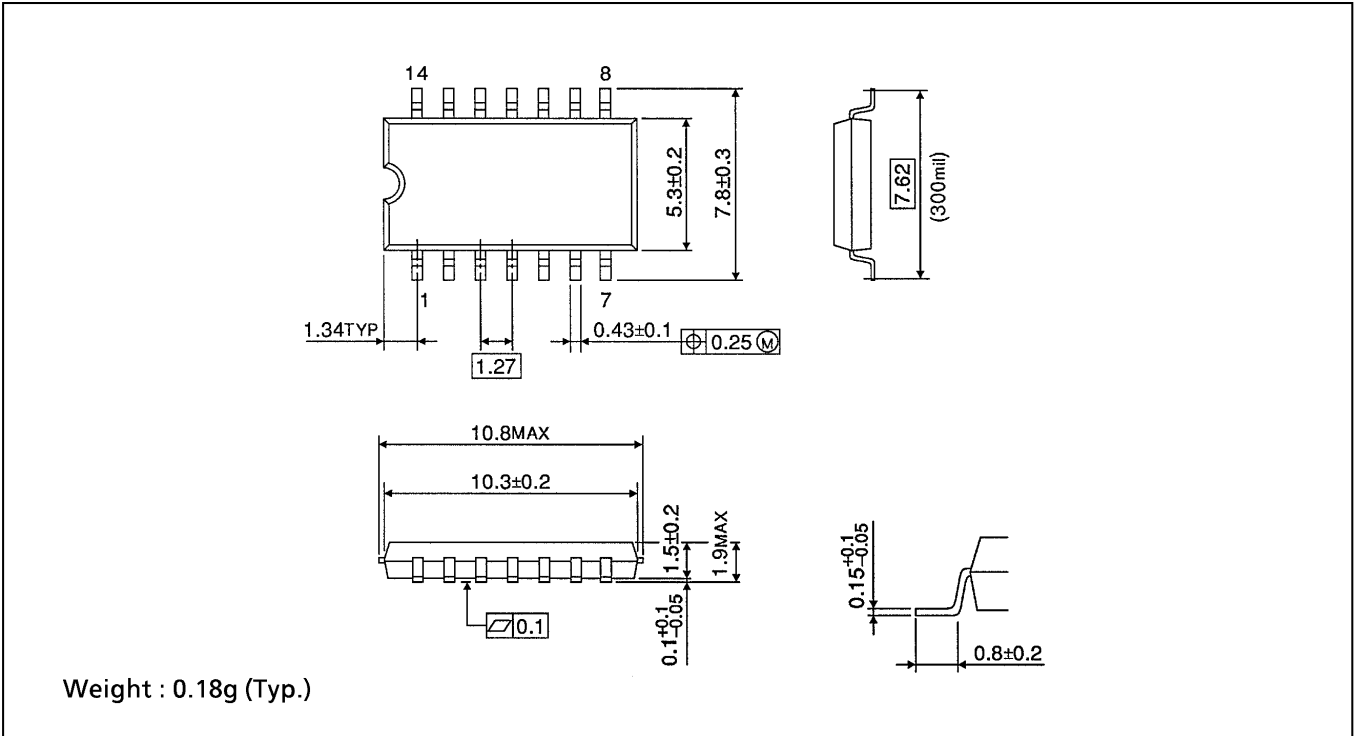
Note (6) C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 2 \text{ ( per F / F )}$$

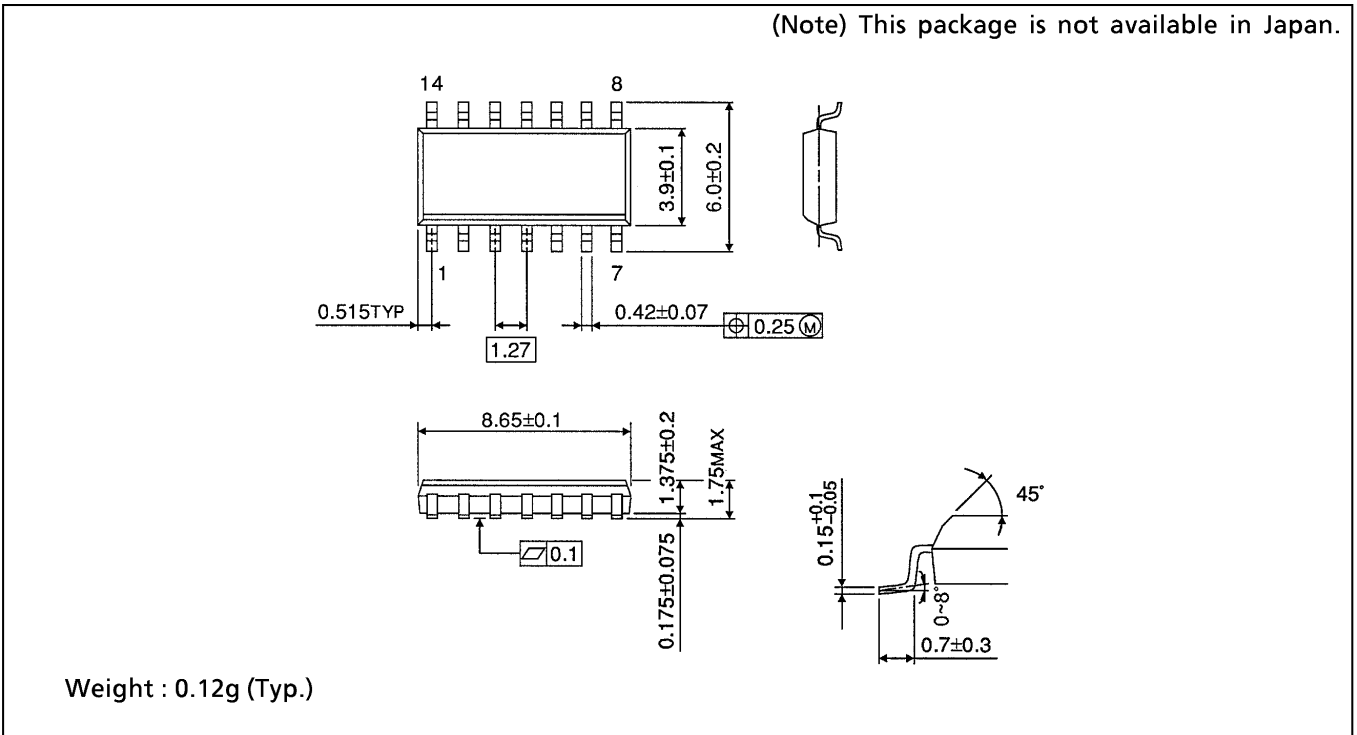
**SOP 14PIN (200mil BODY) PACKAGE DIMENSIONS (SOP14-P-300-1.27)**

Unit in mm



**SOP 14PIN (150mil BODY) PACKAGE DIMENSIONS (SOP14-P-150-1.27)**

Unit in mm



TSSOP 14PIN PACKAGE DIMENSIONS (TSSOP14-P-0044-0.65)

Unit in mm

