

**TOSHIBA**

**MIG20J106L**

TOSHIBA INTELLIGENT POWER MODULE

# MIG20J106L

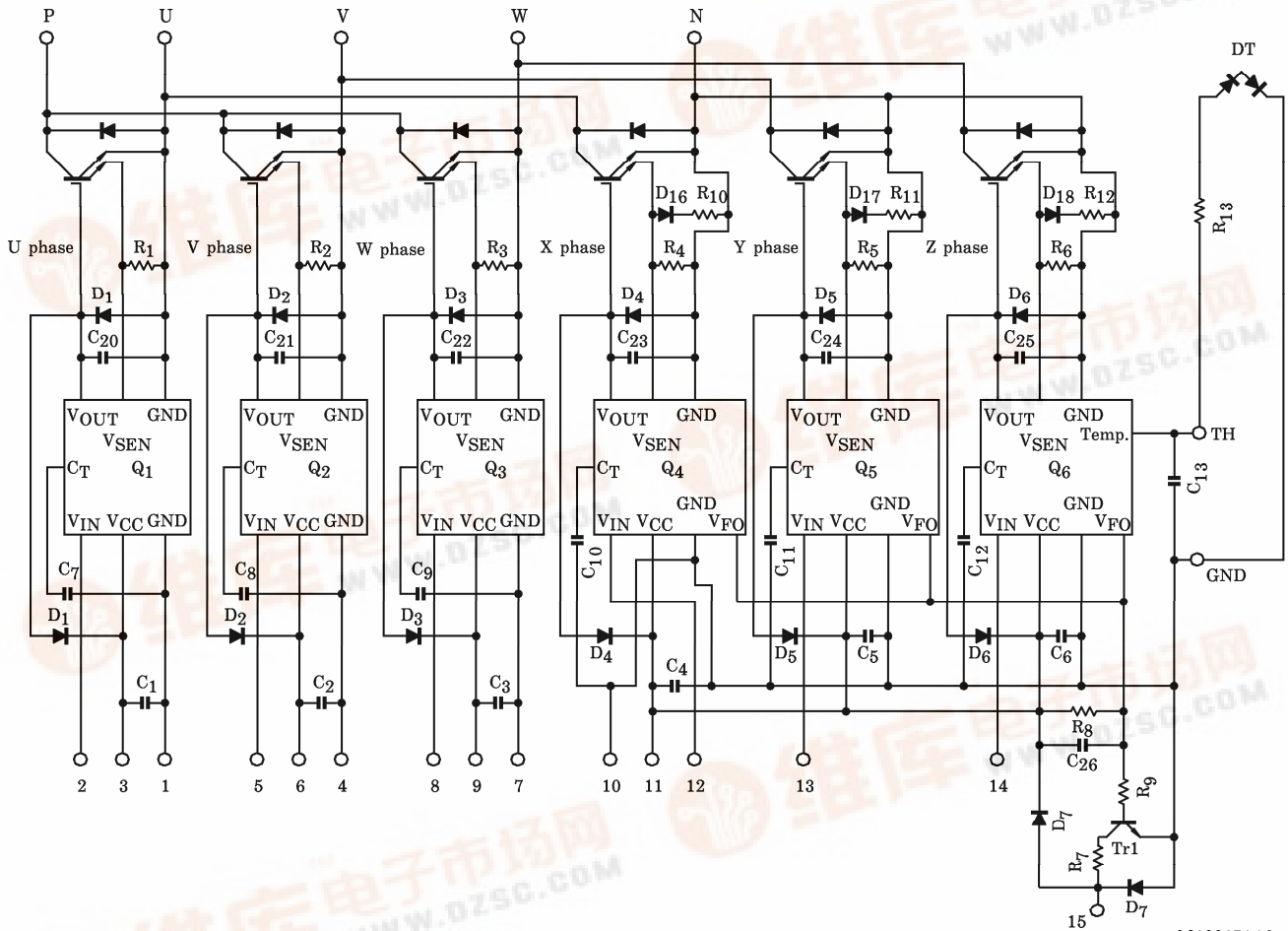
HIGH POWER SWITCHING APPLICATIONS

MOTOR CONTROL APPLICATIONS

The Electrodes are Isolated from Case

- Three Phase IGBT Inverter Output
- Gate Drive Circuit
- Protection Logic
  - Over Current
  - Over Temperature
  - Under Voltage

EQUIVALENT CIRCUIT

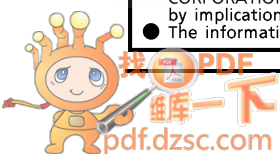


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MAXIMUM RATINGS ( $T_j = 25^\circ\text{C}$ )

	ITEM	SYMBOL	CONDITION	RATING	UNIT
Inverter Part	Supply Voltage	$V_{CC}$	P-N	450	V
	Collector Emitter Voltage	$V_{CES}$	—	600	V
	Collector Current (DC)	$\pm I_C$	$T_c = 25^\circ\text{C}$	20	A
	Collector Current (Peak)	$\pm I_{CP}$	$T_c = 25^\circ\text{C}$	40	A
	Collector Power Dissipation	$P_C$	$T_c = 25^\circ\text{C}$	50	W
	Junction Temperature	$T_j$	—	150	$^\circ\text{C}$
Control Part	Supply Voltage	$V_D$		20	V
	Input Current	$I_{IN}$	—	30	mA
	Fault Output Voltage	$V_{FO}$	—	20	V
	Fault Output Current	$I_{FO}$	—	10	mA
All System	Operating Temperature	$T_c$	—	-20~+90	$^\circ\text{C}$
	Storage Temperature Range	$T_{stg}$	—	-40~+125	$^\circ\text{C}$
	Isolation Voltage	$V_{ISO}$	(*)	2500	$V_{rms}$

(\*) AC 1 minute, Defect Current 1mA.

ELECTRICAL CHARACTERISTICS ( $T_j = 25^\circ\text{C}$ )

Inverter part

ITEM	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	$V_{CC}$	—	P-N	—	300	—	V
Collector-Emitter Saturation Voltage	$V_{CE}(\text{sat})$	—	$V_D = 15\text{V}$ $I_C = 20\text{A}$	—	1.8	2.3	V
		—	$I_{IN} = 10\text{mA}$ $I_C = 20\text{A}, T_j = 125^\circ\text{C}$	—	—	3.0	
		—	—	—	—	—	
Forward Voltage	$V_F$	—	$I_F = 20\text{A}$	—	2.0	2.7	V
Switching Time	$t_{on}$	—	$V_{CC} = 300\text{V}$ $I_C = 20\text{A}$ $V_D = 15\text{V}$ $I_{IN} = 10\text{mA}$ L-Load	—	2.0	3.0	$\mu\text{s}$
	$t_{rr}$			—	0.1	0.2	
	$t_c(\text{on})$			—	1.0	2.0	
	$t_{off}$			—	1.2	2.5	
	$t_c(\text{off})$			—	0.6	1.0	
Collector Cut-off Current	$I_{CEX}$	—	$V_{CE} = 600\text{V}$ —	—	—	1.0	mA
		—	$T_j = 125^\circ\text{C}$	—	—	20	

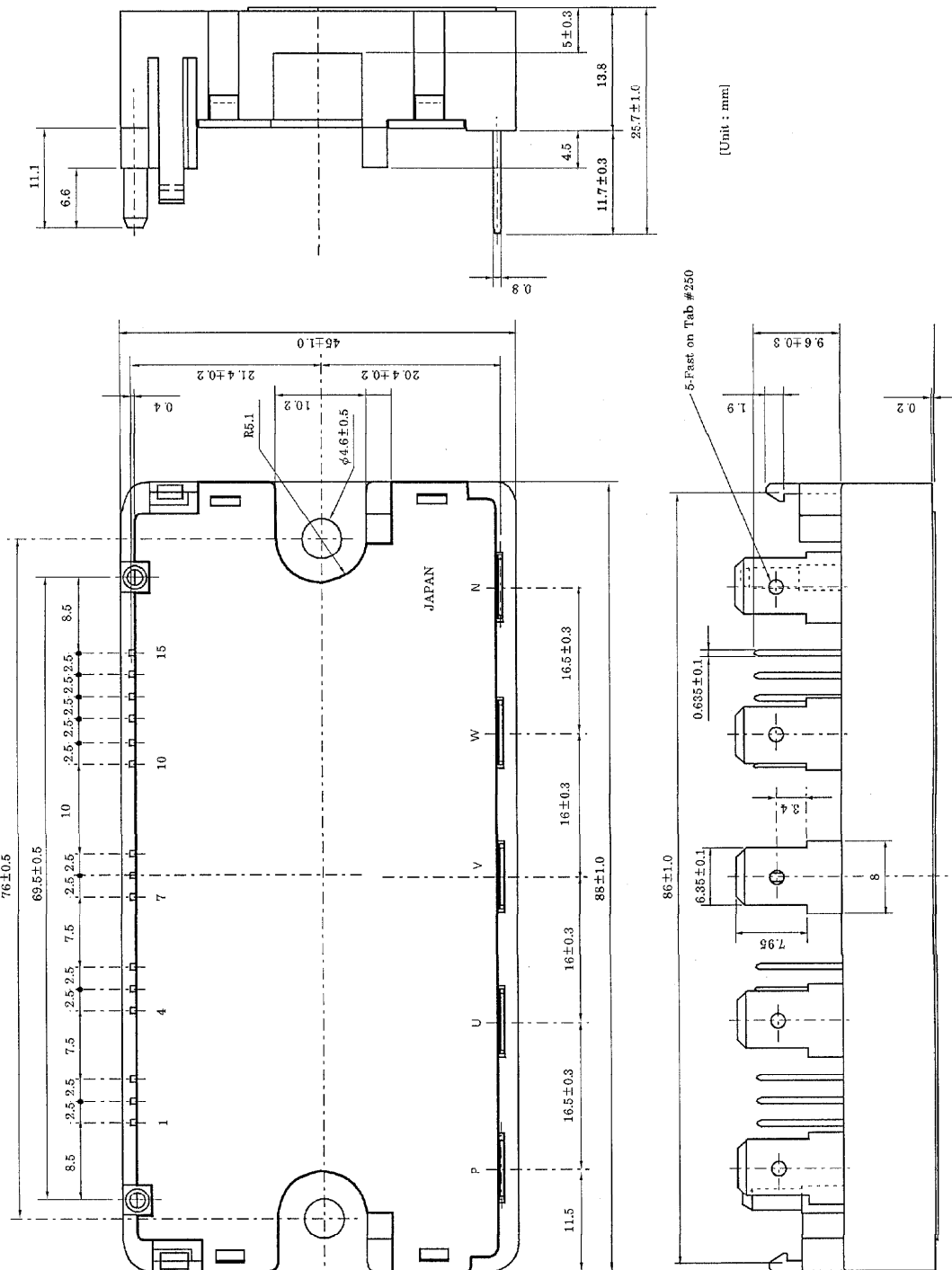
Control part (T<sub>j</sub> = 25°C)

ITEM		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Circuit Current		I <sub>D</sub>	—	V <sub>D</sub> = 15V	—	7	—	mA
				I <sub>IN</sub> = 10mA				
Input On Current		I <sub>IN</sub> (ON)	—	V <sub>D</sub> = 15V	—	5.0	—	mA
Input Off Current		I <sub>IN</sub> (OFF)	—	V <sub>D</sub> = 15V	—	4.0	—	mA
Fault Output Current (Normal Operation)		I <sub>FO</sub>	—	V <sub>D</sub> = 15V, V <sub>FO</sub> = 15V	—	10	—	mA
Over Current Trip Level		OC	—	V <sub>D</sub> = 15V (Low Side)	20	24	—	A
				V <sub>D</sub> = 15V (High Side)	36	42	—	
Over Current Cut Off Time		t <sub>off</sub> (OC)	—	V <sub>D</sub> = 15V	—	10	—	μs
Over Temperature Protection	Trip Level	OT	—	—	100	110	—	°C
	Reset Level (Hys.)				—	15	—	
Under Voltage Protection	Trip Level	UV	—	—	—	12.0	—	V
	Reset Level	UV <sub>r</sub>	—	—	—	12.5	—	
Fault Output Pulse Width		t <sub>FO</sub>	—	V <sub>D</sub> = 15V	8	13	—	ms

Others

ITEM		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Junction to Case Thermal Resistance		R <sub>th(j-c)</sub>	—	INV, IGBT	—	1.8	2.5	°C / W
		R <sub>th(j-c)</sub>	—	INV, FWD	—	3.2	4.5	
Capacitance (Electrodes-Case)			—	—	—	450	900	pF

OUTLINE



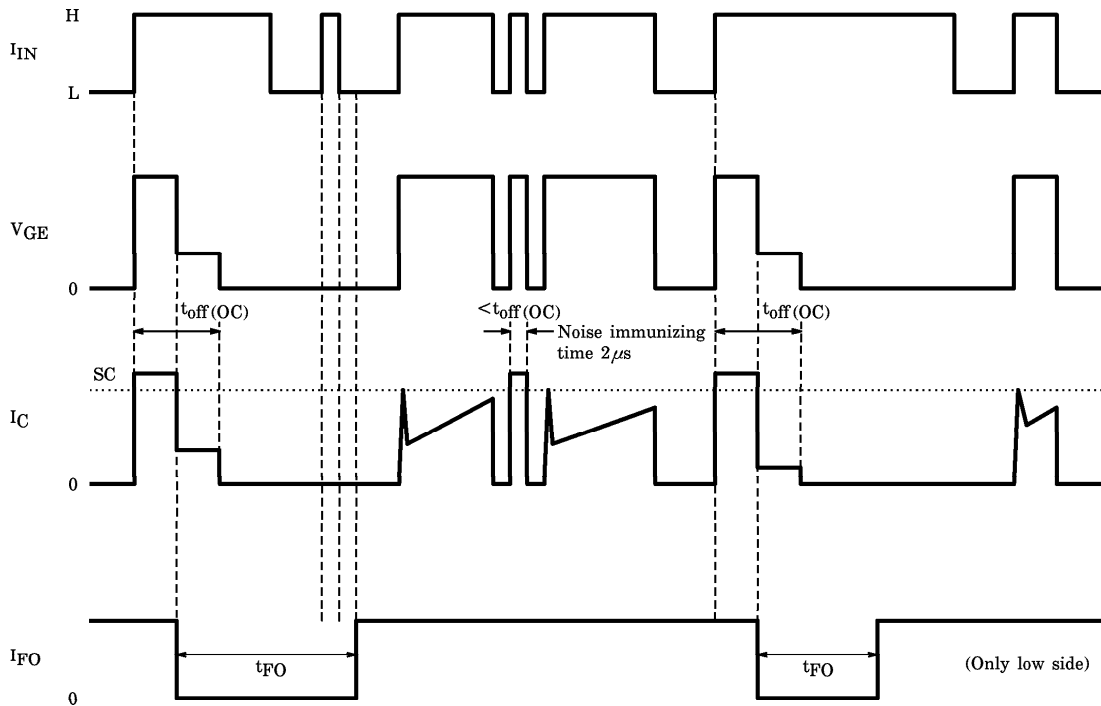
Signal Pin distribution

1	GND (U)
2	VIN (U)
3	VCC (U)
4	GND (V)
5	VIN (V)
6	VCC (V)
7	GND (W)
8	VIN (W)
9	VCC (W)
10	GND
11	VCC
12	VIN (X)
13	VIN (Y)
14	VIN (Z)
15	VFO

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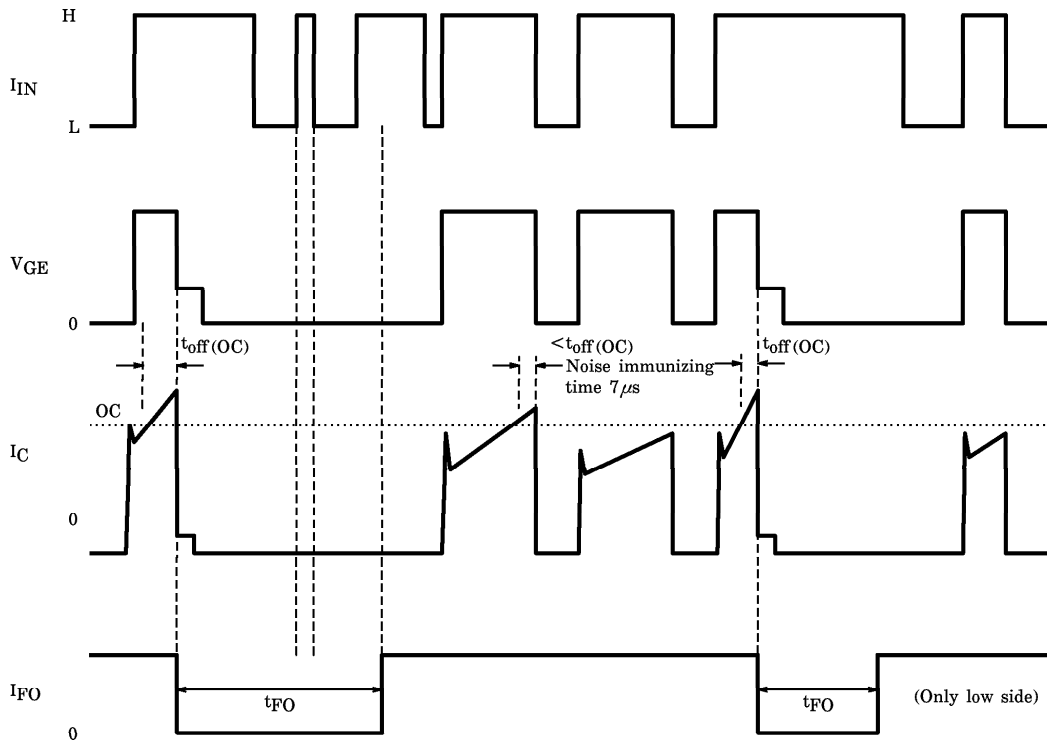
TIMING CHART FOR SHORT CURRENT PROTECTION SEQUENCE

1. Upon occasion of short current condition, at first step,  $V_{GE}$  is step-down to one-half of nominal value in order to reduce IGBT saturation current and finally,  $V_{GE}$  is completely interrupted after some certain time,  $t_{off}(OC)$ .
2. An error signal output ( $V_{FO}$ ) goes into 'H' level when the lower arm IGBT is subjected to over current condition. The timing of  $V_{FO}$  output ('H' level) is provided at complete interruption of  $V_{GE}$  and the 'H' level is maintained during some certain time duration ( $t_{FO}$ ).
3. The reset operation is provided on condition that error signal output return to 'L' level after certain time duration and over current or short current condition is removed, and next input signal turns from operation "off" to "on".



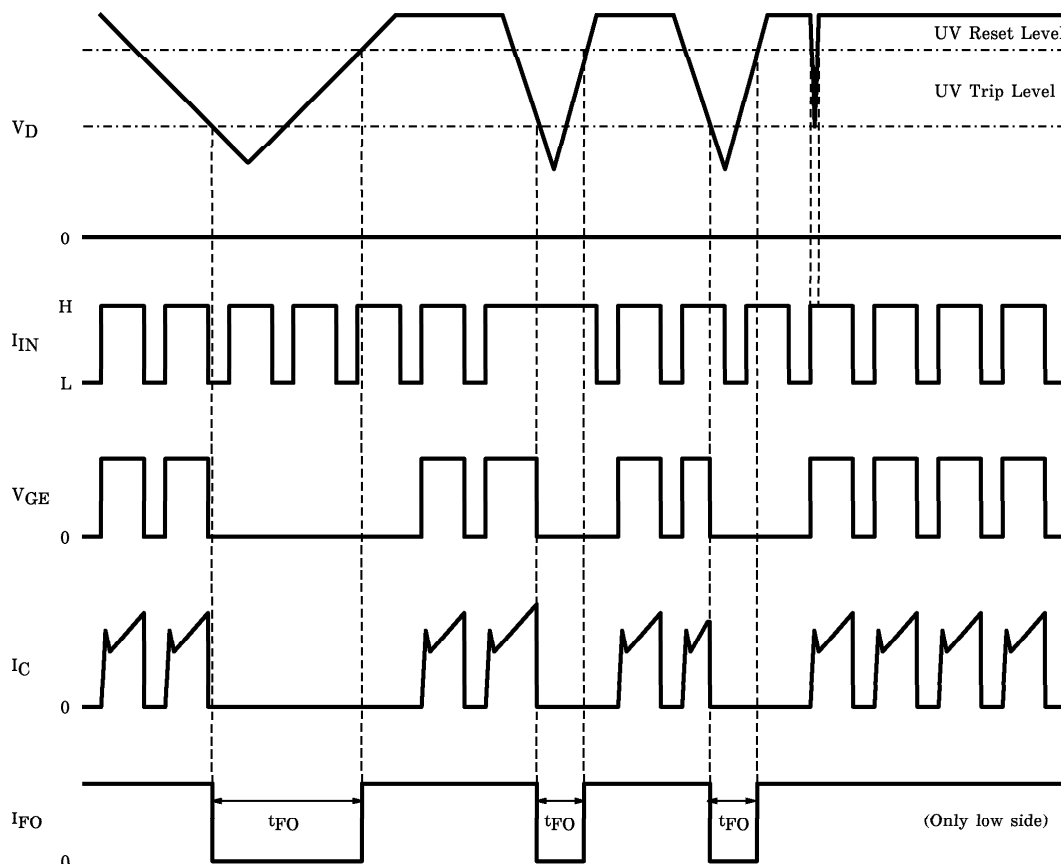
TIMING CHART FOR OVER CURRENT PROTECTION SEQUENCE

1. Upon occasion of over current condition, at first step,  $V_{GE}$  is step-down to one-half of nominal value in order to reduce IGBT saturation current and finally,  $V_{GE}$  is completely interrupted after some certain time,  $t_{off}(OC)$ .
2. An error signal output ( $V_{FO}$ ) goes into 'H' level when the lower arm IGBT is subjected to over current condition. The timing of  $V_{FO}$  output ('H' level) is provided at complete interruption of  $V_{GE}$  and the 'H' level is maintained during some certain time duration ( $t_{FO}$ ).
3. The reset operation is provided on condition that error signal output return to 'L' level after certain time duration and over current condition is removed and input signal turns from operation "off" to "on".



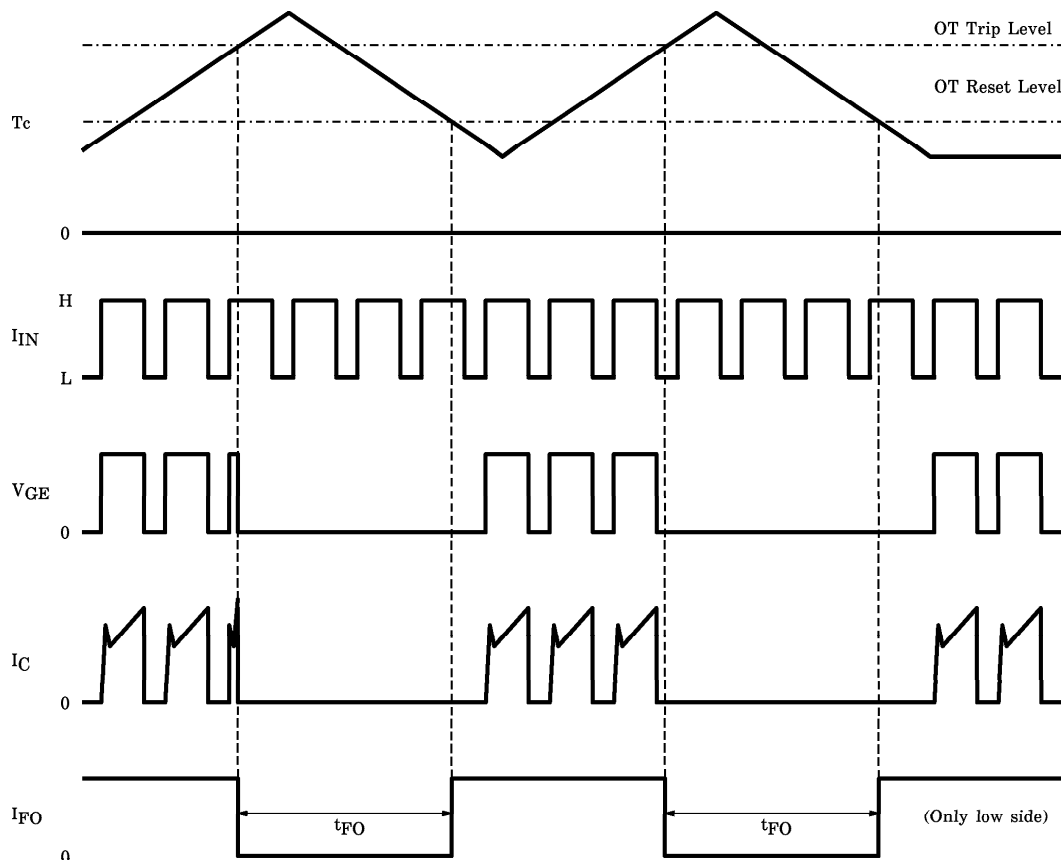
TIMING CHART FOR CONTROL POWER SUPPLY UNDER VOLTAGE PROTECTION SEQUENCE

1. Upon occasion of control power supply under voltage, gate voltage ( $V_{GE}$ ) is interrupted and IGBT moves into 'off-stage'.  
(This condition continues between UV Trip Level and UV Reset Level as shown in the chart)
2. An error signal output ( $V_{FO}$ ) stays in 'H' level until the power supply voltage returns to the reset level after the voltage reaches to the trip level.
3. The reset operation is provided on condition that power supply voltage returns to the UV reset level and input signal turns from operation "off" to "on".



TIMING CHART FOR OVER TEMPERATURE PROTECTION SEQUENCE

1. Using temperature dependent characteristics of diode on IMS substrate, the case temperature ( $T_c$ ) is detected. Upon occasion of over temperature condition,  $V_{GE}$  of the lower arm IGBT is interrupted. (This condition continues between OT Trip Level and OT Reset Level as shown in the chart)
2. An error signal output ( $V_{FO}$ ) stays in 'H' level until the case temperature goes below the reset level after the temperature reaches to the trip level.
3. The reset operation is provided on condition that case temperature goes below the OT reset level and input signal turns from operation "off" to "on".





APPLICATION

