TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

T C 7 M A 5 7 3 F K

Low-Voltage Octal D-Type Latch with 3.6 V Tolerant Inputs and Outputs

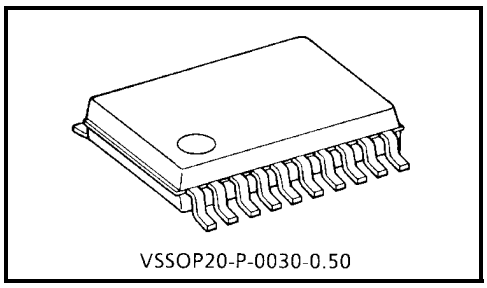
The TC7MA573FK is a high performance CMOS octal D-type latch. Designed for use in 1.8 V, 2.5 V or 3.3 V systems, it achieves high speed operation while maintaining the CMOS low power dissipation.

It is also designed with over voltage tolerant inputs and outputs up to 3.6 V.

This 8 bit D-type latch is controlled by a latch enable input (LE) and an output enable input ($\overline{OE}$).

When the $\overline{OE}$ input is high, the eight outputs are in a high impedance state.

All inputs are equipped with protection circuits against static discharge.



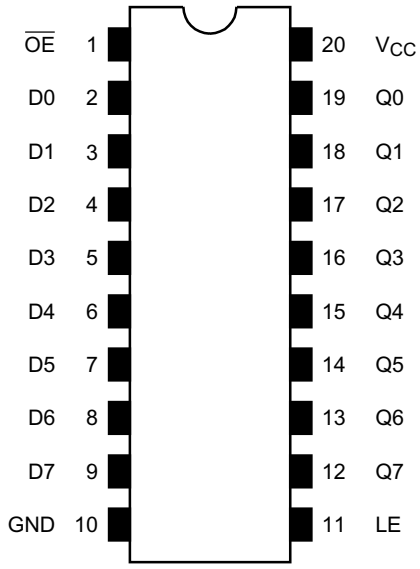
Weight: 0.03 g (typ.)

Features

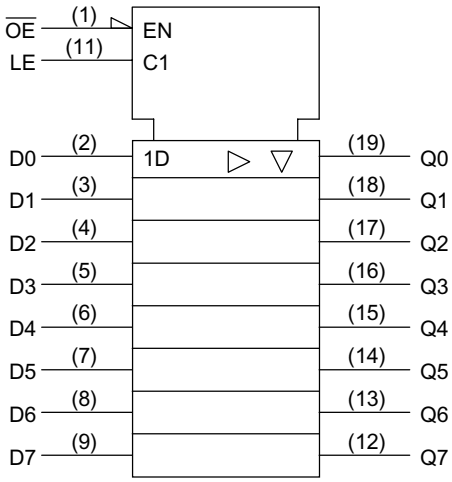
- Low voltage operation: V_{CC} = 1.8~3.6 V
- High speed operation: t_{pd} = 4.2 ns (max) (V_{CC} = 3.0~3.6 V)
  t_{pd} = 4.7 ns (max) (V_{CC} = 2.3~2.7 V)
  t_{pd} = 9.4 ns (max) (V_{CC} = 1.8 V)
- 3.6 V tolerant inputs and outputs.
- Output current: I_{OH}/I_{OL} = ±24 mA (min) (V_{CC} = 3.0 V)
  I_{OH}/I_{OL} = ±18 mA (min) (V_{CC} = 2.3 V)
  I_{OH}/I_{OL} = ±6 mA (min) (V_{CC} = 1.8 V)
- Latch-up performance: ±300 mA
- ESD performance: Machine model > ±200
  Human body model > ±2000 V
- Package: VSSOP (US20)
- Power down protection is provided on all inputs and outputs.
- Supports live insertion/withdrawal (*)

*: To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

Pin Assignment (top view)



IEC Logic Level



Truth Table

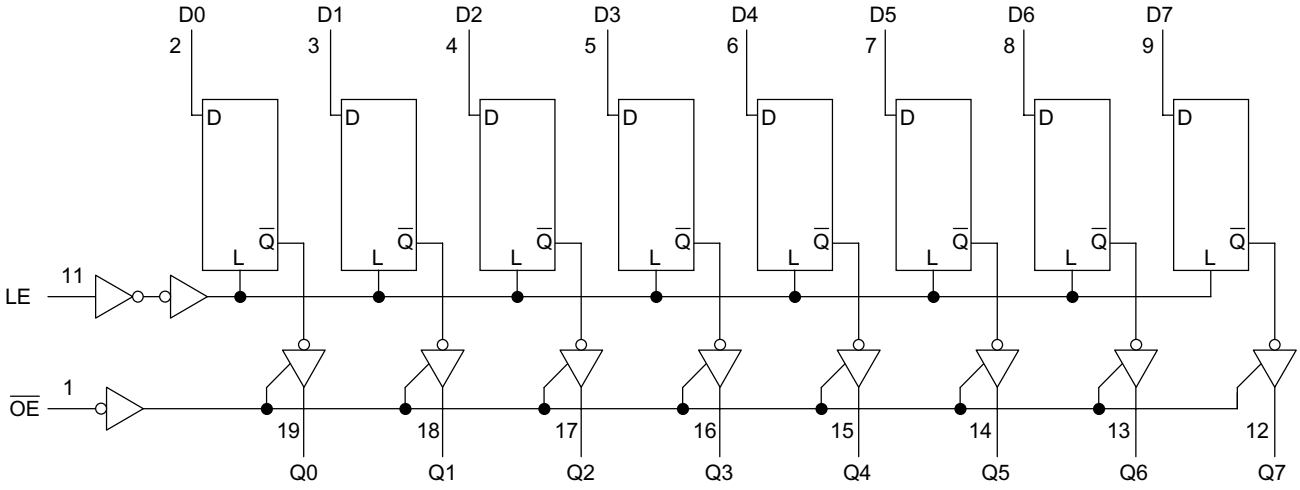
Inputs			Outputs
$\overline{OE}$	LE	D	
H	X	X	Z
L	L	X	Q_n
L	H	L	L
L	H	H	H

X: Don't care

Z: High impedance

Q_n: Q outputs are latched at the time when the LE inputs is taken to a low logic level.

System Diagram



Maximum Ratings

Characteristics	Symbol	Rating	Unit
Power supply voltage	V_{CC}	−0.5~4.6	V
DC input voltage	V_{IN}	−0.5~4.6	V
DC output voltage	V_{OUT}	−0.5~4.6 (Note1)	V
		−0.5~V_{CC} + 0.5 (Note2)	
Input diode current	I_{IK}	−50	mA
Output diode current	I_{OK}	±50 (Note3)	mA
DC output current	I_{OUT}	±50	mA
Power dissipation	P_D	180	mW
DC V_{CC}/ground current	I_{CC}/I_{GND}	±100	mA
Storage temperature	T_{stg}	−65~150	°C

Note1: Off-state

Note2: High or low state. I_{OUT} absolute maximum rating must be observed.

Note3: $V_{OUT} < GND$, $V_{OUT} > V_{CC}$

Recommended Operating Range

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	1.8~3.6	V
		1.2~3.6 (Note4)	
Input voltage	V_{IN}	−0.3~3.6	V
Output voltage	V_{OUT}	0~3.6 (Note5)	V
		0~V_{CC} (Note6)	
Output current	I_{OH}/I_{OL}	±24 (Note7)	mA
		±18 (Note8)	
		±6 (Note9)	
Operating temperature	T_{opr}	−40~85	°C
Input rise and fall time	dt/dv	0~10 (Note10)	ns/V

Note4: Data retention only

Note5: Off-state

Note6: High or low state

Note7: V_{CC} = 3.0~3.6 V

Note8: V_{CC} = 2.3~2.7 V

Note9: V_{CC} = 1.8 V

Note10: V_{IN} = 0.8~2.0 V, V_{CC} = 3.0 V

Electrical Characteristics

DC Characteristics (Ta = –40~85°C, 2.7 V < V_{CC} ≦ 3.6 V)

Characteristics		Symbol	Test Condition		V_{CC} (V)	Min	Max	Unit
Input voltage	High level	V_{IH}	—		2.7~3.6	2.0	—	V
	Low level	V_{IL}	—		2.7~3.6	—	0.8	
Output voltage	High level	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = –100 μA	2.7~3.6	V_{CC} – 0.2	—	V
				I_{OH} = –12 mA	2.7	2.2	—	
				I_{OH} = –18 mA	3.0	2.4	—	
				I_{OH} = –24 mA	3.0	2.2	—	
	Low level	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 100 μA	2.7~3.6	—	0.2	
				I_{OL} = 12 mA	2.7	—	0.4	
				I_{OL} = 18 mA	3.0	—	0.4	
				I_{OL} = 24 mA	3.0	—	0.55	
Input leakage current		I_{IN}	V_{IN} = 0~3.6 V		2.7~3.6	—	±5.0	μA
3-state output off-state current		I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = 0~3.6 V		2.7~3.6	—	±10.0	μA
Power off leakage current		I_{OFF}	V_{IN}, V_{OUT} = 0~3.6 V		0	—	10.0	μA
Quiescent supply current		I_{CC}	V_{IN} = V_{CC} or GND		2.7~3.6	—	20.0	μA
			V_{CC} ≦ (V_{IN}, V_{OUT}) ≦ 3.6 V		2.7~3.6	—	±20.0	
		ΔI_{CC}	V_{IH} = V_{CC} – 0.6 V (per input)		2.7~3.6	—	750	

DC Characteristics (Ta = –40~85°C, 2.3 V ≦ V_{CC} ≦ 2.7 V)

Characteristics		Symbol	Test Condition		V_{CC} (V)	Min	Max	Unit
Input voltage	High level	V_{IH}	—		2.3~2.7	1.6	—	V
	Low level	V_{IL}	—		2.3~2.7	—	0.7	
Output voltage	High level	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = –100 μA	2.3~2.7	V_{CC} – 0.2	—	V
				I_{OH} = –6 mA	2.3	2.0	—	
				I_{OH} = –12 mA	2.3	1.8	—	
				I_{OH} = –18 mA	2.3	1.7	—	
	Low level	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 100 μA	2.3~2.7	—	0.2	
				I_{OL} = 12 mA	2.3	—	0.4	
				I_{OL} = 18 mA	2.3	—	0.6	
Input leakage current		I_{IN}	V_{IN} = 0~3.6 V		2.3~2.7	—	±5.0	μA
3-state output off-state current		I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = 0~3.6 V		2.3~2.7	—	±10.0	μA
Power off leakage current		I_{OFF}	V_{IN}, V_{OUT} = 0~3.6 V		0	—	10.0	μA
Quiescent supply current		I_{CC}	V_{IN} = V_{CC} or GND		2.3~2.7	—	20.0	μA
			V_{CC} ≦ (V_{IN}, V_{OUT}) ≦ 3.6 V		2.3~2.7	—	±20.0	

DC Characteristics (Ta = –40~85°C, 1.8 V ≦ V_{CC} < 2.3 V)

Characteristics		Symbol	Test Condition		V_{CC} (V)	Min	Max	Unit
Input voltage	High level	V_{IH}	—		1.8~2.3	0.7 × V_{CC}	—	V
	Low level	V_{IL}	—		1.8~2.3	—	0.2 × V_{CC}	
Output voltage	High level	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = –100 μA	1.8	V_{CC} – 0.2	—	V
				I_{OH} = –6 mA	1.8	1.4	—	
	Low level	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 100 μA	1.8	—	0.2	
				I_{OL} = 6 mA	1.8	—	0.3	
Input leakage current		I_{IN}	V_{IN} = 0~3.6 V		1.8	—	±5.0	μA
3-state output off-state current		I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = 0~3.6 V		1.8	—	±10.0	μA
Power off leakage current		I_{OFF}	V_{IN}, V_{OUT} = 0~3.6 V		0	—	10.0	μA
Quiescent supply current		I_{CC}	V_{IN} = V_{CC} or GND		1.8	—	20.0	μA
			V_{CC} ≦ (V_{IN}, V_{OUT}) ≦ 3.6 V		1.8	—	±20.0	

AC Characteristics (Ta = –40~85°C, Input: $t_r = t_f = 2.0$ ns, $C_L = 30$ pF, $R_L = 500\ \Omega$)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Min	Max	Unit
Propagation delay time (D-Q)	t_{pLH} t_{pHL}	Figure 1, Figure 2	1.8	1.5	9.4	ns
			2.5 ± 0.2	0.8	4.7	
			3.3 ± 0.3	0.6	4.2	
Propagation delay time (LE-Q)	t_{pLH} t_{pHL}	Figure 1, Figure 2	1.8	1.5	9.8	ns
			2.5 ± 0.2	0.8	4.9	
			3.3 ± 0.3	0.6	4.2	
3-state output enable time	t_{pZL} t_{pZH}	Figure 1, Figure 3	1.8	1.5	9.8	ns
			2.5 ± 0.2	0.8	5.5	
			3.3 ± 0.3	0.6	4.5	
3-state output disable time	t_{pLZ} t_{pHZ}	Figure 1, Figure 3	1.8	1.5	6.5	ns
			2.5 ± 0.2	0.8	3.6	
			3.3 ± 0.3	0.6	3.3	
Minimum pulse width	$t_{w\ (H)}$	Figure 1, Figure 2	1.8	4.0	—	ns
			2.5 ± 0.2	1.5	—	
			3.3 ± 0.3	1.5	—	
Minimum set-up time	t_s	Figure 1, Figure 2	1.8	2.5	—	ns
			2.5 ± 0.2	1.5	—	
			3.3 ± 0.3	1.5	—	
Minimum hold time	t_h	Figure 1, Figure 2	1.8	1.0	—	ns
			2.5 ± 0.2	1.0	—	
			3.3 ± 0.3	1.0	—	
Output to output skew	t_{osLH} t_{osHL}	(Note11)	1.8	—	0.5	ns
			2.5 ± 0.2	—	0.5	
			3.3 ± 0.3	—	0.5	

For $C_L = 50$ pF, add approximately 300 ps to the AC maximum specification.

Note11: This parameter is guaranteed by design.
($t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$)

Dynamic Switching Characteristics (Ta = 25°C, Input: $t_r = t_f = 2.0$ ns, $C_L = 30$ pF)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Typ.	Unit
Quiet output maximum dynamic V_{OL}	V_{OLP}	V_{IH} = 1.8 V, V_{IL} = 0 V (Note12)	1.8	0.25	V
		V_{IH} = 2.5 V, V_{IL} = 0 V (Note12)	2.5	0.6	
		V_{IH} = 3.3 V, V_{IL} = 0 V (Note12)	3.3	0.8	
Quiet output minimum dynamic V_{OL}	V_{OLV}	V_{IH} = 1.8 V, V_{IL} = 0 V (Note12)	1.8	−0.25	V
		V_{IH} = 2.5 V, V_{IL} = 0 V (Note12)	2.5	−0.6	
		V_{IH} = 3.3 V, V_{IL} = 0 V (Note12)	3.3	−0.8	
Quiet output minimum dynamic V_{OH}	V_{OHV}	V_{IH} = 1.8 V, V_{IL} = 0 V (Note12)	1.8	1.5	V
		V_{IH} = 2.5 V, V_{IL} = 0 V (Note12)	2.5	1.9	
		V_{IH} = 3.3 V, V_{IL} = 0 V (Note12)	3.3	2.2	

Note12: This parameter is guaranteed by design.

Capacitive Characteristics (Ta = 25°C)

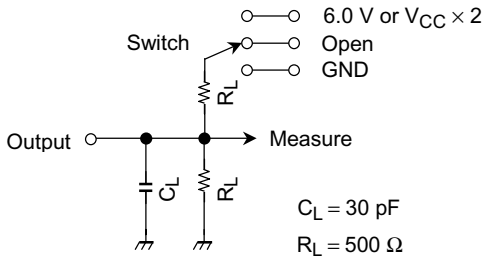
Characteristics	Symbol	Test Condition	V_{CC} (V)	Typ.	Unit
Input capacitance	C_{IN}	—	1.8, 2.5, 3.3	6	pF
Output capacitance	C_O	—	1.8, 2.5, 3.3	7	pF
Power dissipation capacitance	C_{PD}	f_{IN} = 10 MHz (Note13)	1.8, 2.5, 3.3	20	pF

Note13: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$I_{CC\ (opr)} = C_{PD}KV_{CC}Kf_{IN} + I_{CC}/8$ (per bit)

AC Test Circuit



Parameter	Switch	
t_{pLH}, t_{pHL}	Open	
t_{pLZ}, t_{pZL}	6.0 V $V_{CC} \times 2$	V_{CC} = 3.3 ± 0.3 V V_{CC} = 2.5 ± 0.2 V V_{CC} = 1.8 V
t_{pHZ}, t_{pZH}	GND	

Figure 1

AC Waveform

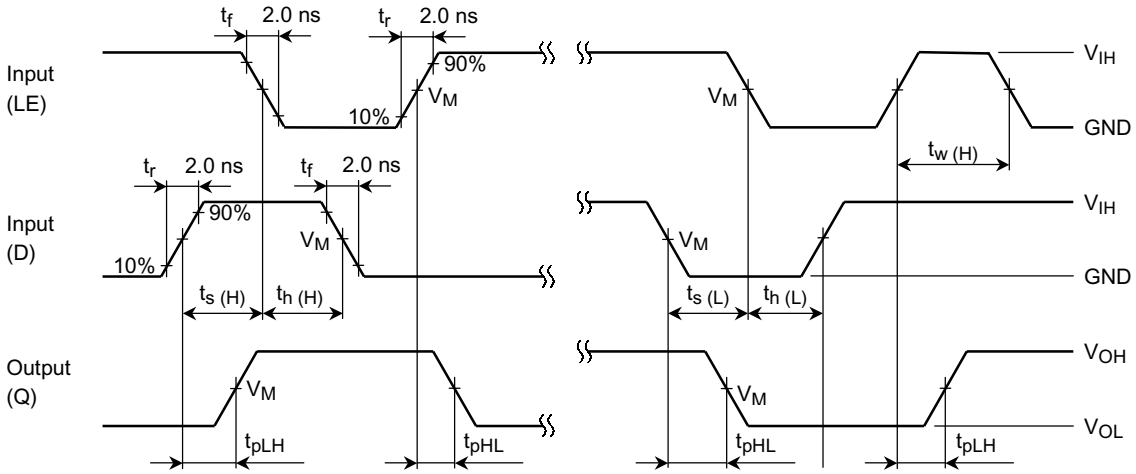
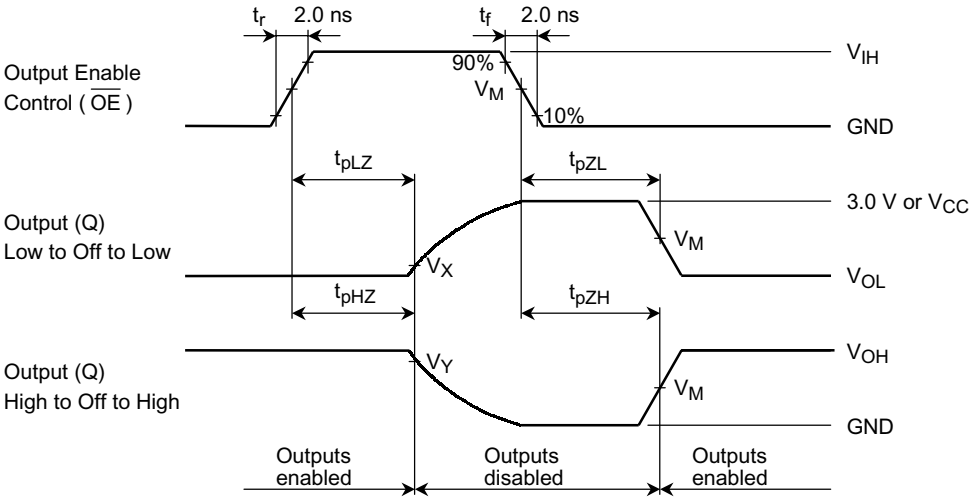


Figure 2 t_{pLH}, t_{pHL}, t_w, t_s, t_h

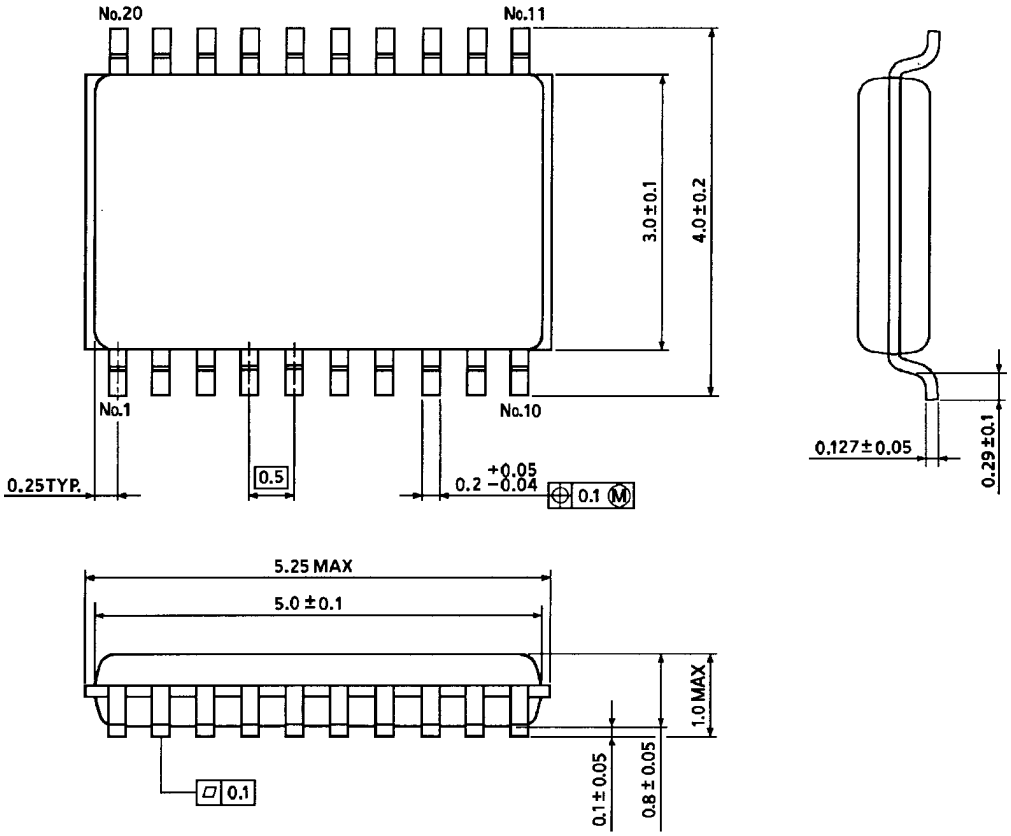


Symbol	V_{CC}		
	3.3 ± 0.3 V	2.5 ± 0.2 V	1.8 V
V_{IH}	2.7 V	V_{CC}	V_{CC}
V_M	1.5 V	$V_{CC}/2$	$V_{CC}/2$
V_X	V_{OL} + 0.3 V	V_{OL} + 0.15 V	V_{OL} + 0.15 V
V_Y	V_{OH} − 0.3 V	V_{OH} − 0.15 V	V_{OH} − 0.15 V

Figure 3 t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}

Package Dimensions

VSSOP20-P-0030-0.50 Unit : mm



Weight: 0.03 g (typ.)