

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

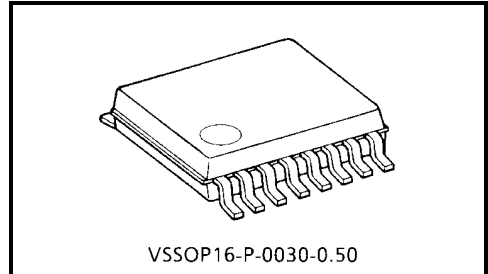
# TC7MB3253FK

Dual 1-of-4 FET Multiplexer/Demultiplexer

The TC7MB3253FK is high-speed CMOS dual 1-4 Multiplexer/Demultiplexer. The low on resistance of the switch allows connections to be made with minimal propagation delay time.

This device consists of two individual two-inputs multiplexer/demultiplexer with common select inputs (S1, S0). The A inputs is connected to the corresponded B1~B4 outputs determined by the combination both the select inputs (S1, S0) and output enable ( $\overline{OE}$ ). When the output enable ( $\overline{OE}$ ) input is held "H" level, the switches are open with regardless the state of select inputs and a high-impedance state exists between the switches.

All inputs are equipped with protection circuits against static discharge.



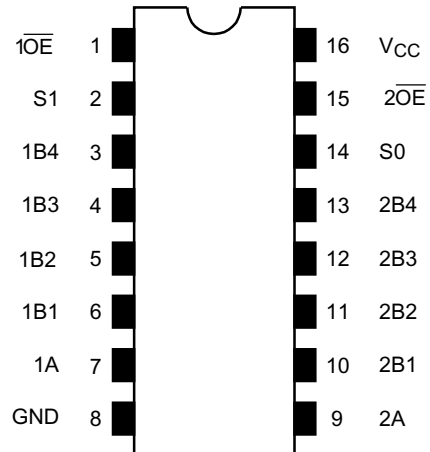
VSSOP16-P-0030-0.50

Weight: 0.02 g (typ.)

## Features

- Operating voltage:  $V_{CC} = 4.5 \sim 5.5 \text{ V}$
- High speed:  $t_{pd} = 0.25 \text{ ns (max)}$
- Low on resistance:  $R_{ON} = 5 \Omega \text{ (typ.)}$
- ESD performance: Machine model  $> \pm 200 \text{ V}$   
Human body model  $> \pm 2000 \text{ V}$
- Compatible with TTL outputs (control inputs)
- Package: VSSOP (US16)
- Pin compatible with the 74xx253 type.  
Functionally equivalent to (FST/CBT) 3253.

## Pin Assignment (top view)



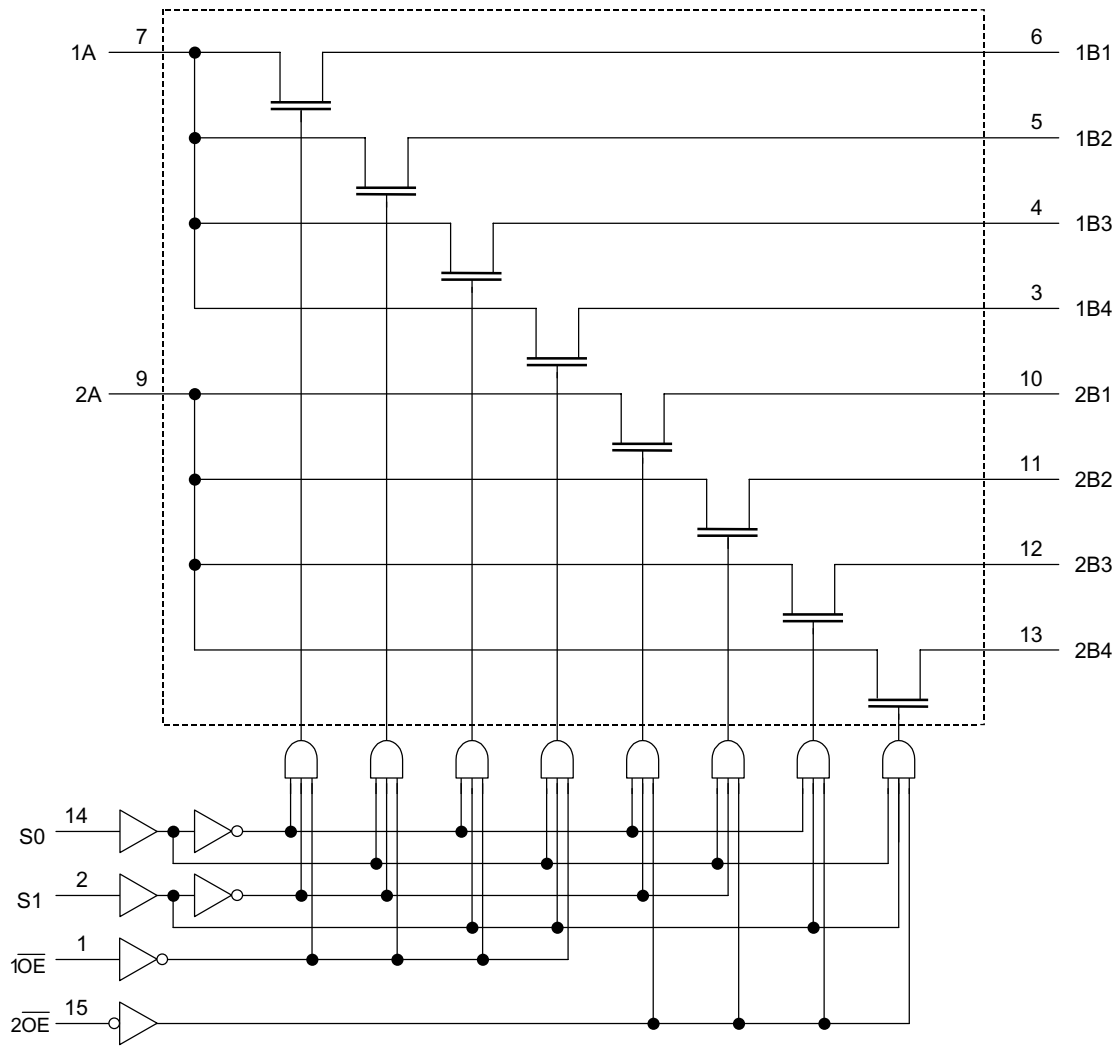
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Truth Table

Inputs			Function
$\overline{OE}$	S1	S0	
L	L	L	A port = B1 port
L	L	H	A port = B2 port
L	H	L	A port = B3 port
L	H	H	A port = B4 port
H	X	X	Disconnect

System Diagram



## Maximum Ratings

Characteristics	Symbol	Rating	Unit
Power supply range	$V_{CC}$	-0.5~7.0	V
DC input voltage	$V_{IN}$	-0.5~7.0	V
DC switch voltage	$V_S$	-0.5~7.0	V
Input diode current	$I_{IK}$	-50	mA
Continuous channel current	$I_S$	128	mA
Power dissipation	$P_D$	180	mW
DC $V_{CC}$ /GND current	$I_{CC}/I_{GND}$	$\pm 100$	mA
Storage temperature	$T_{stg}$	-65~150	°C

## Recommended Operating Conditions

Characteristics	Symbol	Rating	Unit
Supply voltage	$V_{CC}$	4.5~5.5	V
Input voltage	$V_{IN}$	0~5.5	V
Switch voltage	$V_S$	0~5.5	V
Operating temperature	$T_{opr}$	-40~85	°C
Input rise and fall time	dt/dv	0~10	ns/V

## Electrical Characteristics

DC Characteristics ( $T_a = -40\sim 85^\circ\text{C}$ )

Characteristics		Symbol	Test Condition		Min	Typ. (Note1)	Max	Unit
				$V_{CC}$ (V)				
Input voltage	"H" level	$V_{IH}$	—	4.5~5.5	2.0	—	—	V
	"L" level	$V_{IL}$	—	4.5~5.5	—	—	0.8	
Input leakage current		$I_{IN}$	$V_{IN} = 0\sim 5.5\text{ V}$	5.5	—	—	$\pm 1.0$	$\mu\text{A}$
Off-state leakage current (switch off)		$I_{SZ}$	$A, B = 0\sim 5.5\text{ V}, \overline{OE} = V_{CC}$	5.5	—	—	$\pm 1.0$	$\mu\text{A}$
On resistance (Note2)		$R_{ON}$	$V_{IS} = 0\text{ V}$	$I_{IS} = 64\text{ mA}$	4.5	—	5	$\Omega$
				$I_{IS} = 30\text{ mA}$	4.5	—	5	
			$V_{IS} = 2.4\text{ V}, I_{IS} = 15\text{ mA}$		4.5	—	10	
Increase in $I_{CC}$ per input		$I_{CC}$	$V_{IN} = V_{CC}\text{ or GND}, I_{OUT} = 0$		5.5	—	10	$\mu\text{A}$
		$\Delta I_{CC}$	$V_{IN} = 3.4\text{ V (one input)}$		5.5	—	2.5	mA

Note1: Typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_a = 25^\circ\text{C}$ .

Note2: Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

## AC Characteristics (Ta = -40~85°C)

Characteristics	Symbol	Test Condition	V <sub>CC</sub> (V)	Min	Max	Unit
Propagation delay time (bus to bus)	t <sub>pLH</sub> t <sub>pHL</sub>	Figure 1, Figure 2 (Note3)	4.5	—	0.25	ns
Propagation delay time (S to bus)	t <sub>pLH</sub> t <sub>pHL</sub>	Figure 1, Figure 2	4.5	—	5.3	ns
Output enable time ( $\overline{\text{OE}}$ to bus)	t <sub>pZL</sub> t <sub>pZH</sub>	Figure 1, Figure 3	4.5	—	5.3	ns
Output enable time (S to bus)	t <sub>pZL</sub> t <sub>pZH</sub>	Figure 1, Figure 3	4.5	—	5.3	ns
Output disable time ( $\overline{\text{OE}}$ to bus)	t <sub>pLZ</sub> t <sub>pHZ</sub>	Figure 1, Figure 3	4.5	—	5.3	ns
Output disable time (S to bus)	t <sub>pLZ</sub> t <sub>pHZ</sub>	Figure 1, Figure 3	4.5	—	5.3	ns

Note3: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical on resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage the source (zero output impedance).

## Capacitive Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	V <sub>CC</sub> (V)	Typ.	Unit
Control pin input capacitance ( $\overline{\text{OE}}$ , S)	C <sub>IN</sub>	(Note4)	5.0	3	pF
Switch terminal capacitance (B1~4)	C <sub>I/O</sub>	$\overline{\text{OE}} = V_{CC}$ (Note4)	5.0	10	pF
Switch terminal capacitance (A)	C <sub>I/O</sub>	$\overline{\text{OE}} = V_{CC}$ (Note4)	5.0	31	pF

Note4: This parameter is guaranteed by design.

AC Test Circuit

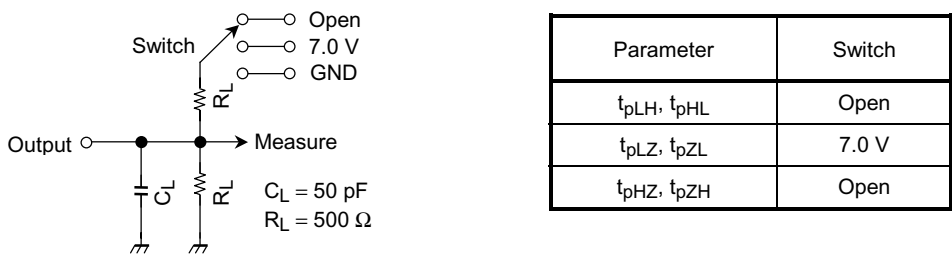


Figure 1

AC Waveform

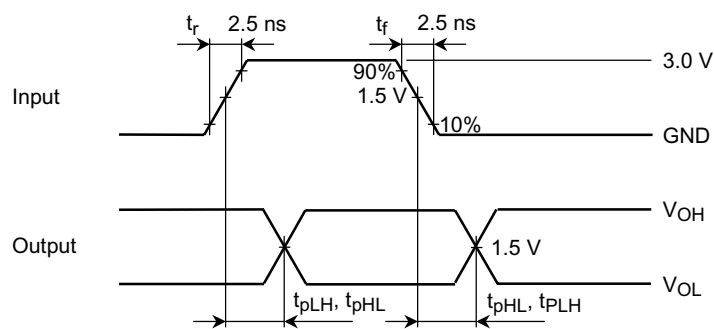


Figure 2  $t_{pLH}$ ,  $t_{pHL}$

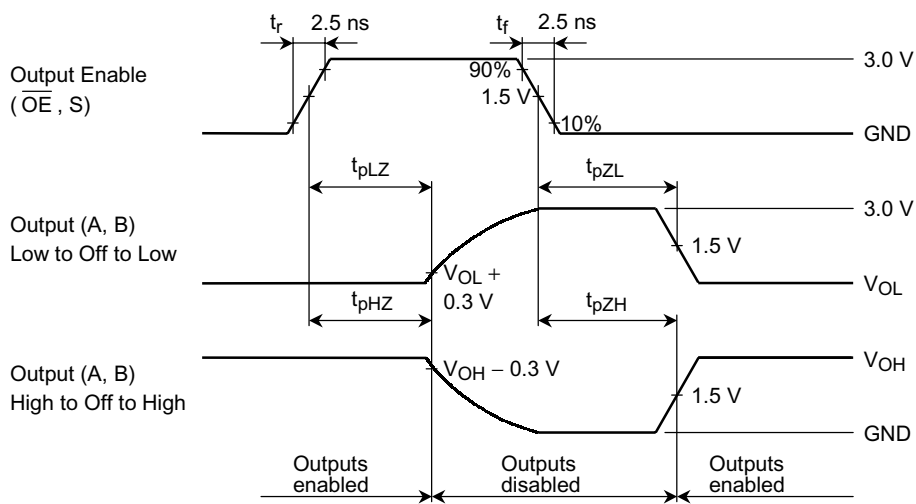
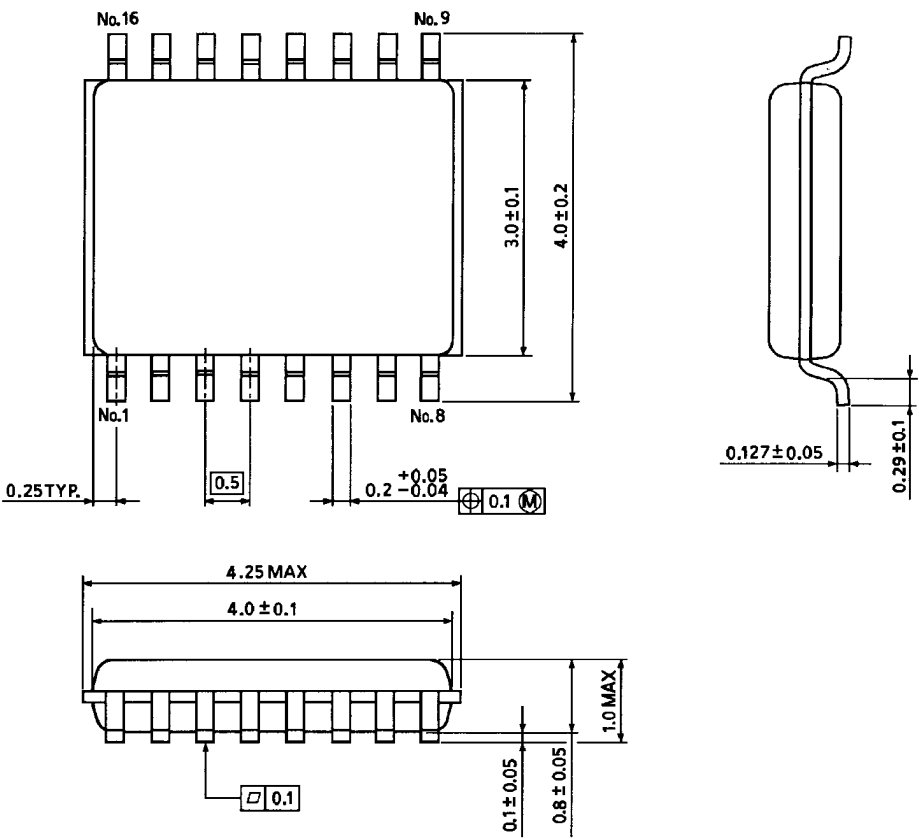


Figure 3  $t_{pLZ}$ ,  $t_{pHZ}$ ,  $t_{pZL}$ ,  $t_{pZH}$

Package Dimensions

VSSOP16-P-0030-0.50

Unit : mm



Weight: 0.02 g (typ.)