W40C06A

Six Outputs

Features

- **Six skew-controlled CMOS outputs with enables**
- **Low output impedance, high current output buffers**
- **Each output can drive two 50Ω (or higher) clock lines**
- **3.3V operation**
- **DC to 100-MHz operation**
- **Controlled output rate slew reduces EMI and output ringing**
- **Ideal for PCI or CPU clock distribution**
- **Low power CMOS design available in:**
  - **16-pin SSOP (Shrink Small Outline Package)**

Key Specifications

Supply Voltages: ..... V_{CC} = 3.3V ±10% or 5.0V±10%

Operating Temperature: ..... 0°C to +70°C

Output Frequency: ..... DC to 100 MHz

Skew Output: ..... <400 ps rising edges <500 ps falling edges

Output Drive Current: ..... 48 mA max

Output Impedance: 5Ω

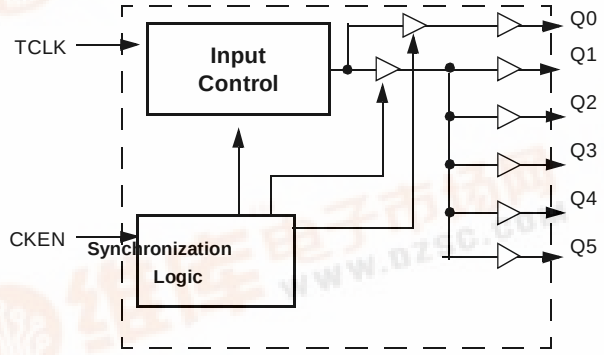
Output Rise/Fall Edge Rate: .....1 to 4 volts/ns

Output Duty Cycle: ..... 40/65% worst case

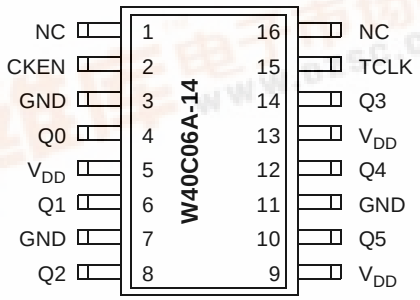
Table 1. Output Enable Selection (-14)

W40C06A-14		
CKEN	**Q0**	**Q1:5**
0	Active	Low
1	Active	Active

Block Diagram



Pin Configuration



Pin Definitions

Pin Name	Pin No.	Pin Type	Pin Description
Q0:5	4, 6, 8, 10, 12, 14	O	***Buffered Clock Outputs:*** Six skew controlled CMOS clock outputs.
VDD	5, 9, 13	P	***Power Connection:*** Power supply for core logic and output buffers. Connected to a 3.3V supply.
GND	3, 7, 11	G	***Ground Connection:*** Connect all ground pins to the common system ground plane.
CKEN	2	I	***Clock Enable:*** Provide Start/Stop control of buffer outputs refer to *Table 1*.
TCLK	15	I	***Clock Input:*** External reference frequency input.
NC	1, 16	NC	***No Connection:*** These pins should remain unconnected.

General Overview

The W40C06A is a six-output, low-skew clock buffer ideally suited for PCI, CPU, and other system clock applications. Each high-current, low-impedance output is specifically designed to drive up to two impedance-controlled signal lines. Controlled output rise/fall times further help to provide good signal characteristics.

The W40C06A is ideal for clock signal distribution in skew sensitive applications such as Pentium® processor or PCI applications. W40C06A-14 has an enable input pin (see *Table 1*) that starts and stops the clock outputs without producing short cycles.

Functional Description

The W40C06A enable pin provides start/stop control of buffer outputs Q0 through Q5. Refer to *Table 1*, “Output Enable Selection,” for decoding. Active (enabled) outputs are in phase with TCLK but are phase delayed by several nanoseconds. Low (disabled) outputs are held at logic LOW.

Synchronization Logic

Output Control

To prevent output “short cycling,” internal synchronization logic is used to ensure complete clocks cycles. This is true for both output enable or disable. Upon enabling an output, there is a maximum latency of four clock cycles, assuming the crystal oscillator is active.

Clock Transmission Lines in System Applications

With the increase in system clock frequencies, transmission line theory is commonly being applied to the design of clock distribution lines. High-speed logic systems typically require tight skew control between clock lines, which means that the clock signal must have short rise/fall times to overcome the effect of noise. Short rise/fall times may create other problems such as signal overshoot/undershoot and signal reflections which may result in distorting the signal at the load end. These problems must be avoided since they create unwanted clock skew.

Reflections and signal overshoot/undershoot can be controlled by designing clock distribution traces as transmission lines. A transmission line accepts and delivers a clock signal without distortion or reflections if its impedance is matched to the line source and load. In system clock line implementation, source impedance is typically controlled but is not practical to control load impedance.

Clock source impedance is matched to the transmission line by using series termination; this involves the addition of a series termination resistor between the output pin and transmission line to, in effect, raise the output buffer impedance to match the line. For example, if the clock output buffer impedance is 30Ω and the transmission line impedance is 50Ω, a 20Ω termination resistor connected between the clock output and transmission line will match the two (the clock buffer impedance becomes 50Ω).

The end of the transmission line is usually “open” with the only load being the typically high-resistance capacitive load of the logic input on the device being clocked. This condition causes a reflection to be sent back to the source. If the source is properly matched to line (through series termination), this reflection will be absorbed (a poorly matched source will re-reflect the pulse edge which can cause waveform distortion by mixing a reflected edge with a new clock pulse edge).

It is interesting to note that when a new clock edge is first driven into the transmission line, the voltage level at the input of the line is only one-half the final signal amplitude, assuming a properly matched line. This edge remains at half amplitude for the time it takes for the edge to reach the end of the line and back. The edge travels down the line at a speed of about 0.2 ns per inch of transmission, so for a five-inch line this round-trip takes about 2.0 ns. During that time, the clock source dissipates power at the rate of $(V_{DD}/2)^2/R$, where R is the sum resistance of the output buffer and series termination resistor (this assumes the case of a CMOS output driver, as used in the W40C06A, where the clock signal amplitude is equal to V_{DD}).

W40C06A Clock Driver Advantages

Low Output Impedance

The typical CMOS clock buffer device has an output impedance of around 50Ω. This means that a typical 60Ω transmission line can be properly series terminated with a 10Ω matching resistor. However, two 60Ω transmission lines could not be driven with series termination (to maintain good waveform integrity) since this presents a 30Ω load to the buffer.

The W40C06A exhibits a 5Ω typical buffer output impedance. The main advantage of the low W40C06A output impedance is that one output can drive more than one transmission line while maintaining proper series termination. For example, if

driving two 50Ω lines, the W40C06A buffer output resistance (as seen by each line) will be about 10Ω, therefore each line can be series terminated with a 40Ω resistor.

Other advantages are also gained by the W40C06A buffer output impedance being much less than the series termination resistor value. First, output buffer impedance variation will have less effect on total source impedance. A CMOS output buffer can vary as much as ±20% with changes in process and operating conditions, while variation of the termination resistor is typically less than 5%. Source impedance (with less variation) results in better signal integrity. Second, more power will be dissipated by the series termination resistor than by the output buffer. This can be important when driving many long transmission lines; the termination resistors are less affected by heating than are CMOS buffer devices.

Controlled Output Rise and Fall Time

The W40C06A incorporates internal clock edge rise/fall time control to further improve clock integrity. Rise/fall times that are too fast cause excessive signal overshoot/undershoot due to interactions between the high device impulse current and power supply inductance caused by the device packaging. Rise/fall times that are too slow make it difficult to meet the system clock skew requirement, especially in the presence of system noise.

Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability

Parameter	Description	Rating	Unit
V_{DD}, V_{IN}	Voltage on any pin with respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Operating Temperature	0 to +70	°C
T_B	Ambient Temperature under Bias	–55 to +125	°C

3.3V DC Electrical Characteristics: T_A = 0°C to +70°C, V_{DD} = 3.3V±10%

Parameter	Description	Test Condition	Min	Typ	Max	Unit
I_{DD}	Supply Current	Note 1		50	60	mA
I_{DD}	Standby Current	CKEN = 0		7	12	µA
V_{IL}	Input Low Voltage	V_{DD} = 3.3V			0.8	V
V_{IH}	Input High Voltage	V_{DD} = 3.3V	2.0			V
V_{OL}	Output Low Voltage	I_{OL} = 48 mA, V_{DD} = 3.3V			0.4	V
V_{OH}	Output High Voltage	I_{OH} = –48 mA, V_{DD} = 3.3V	2.4			V
I_{IL}	Input Low Current	V_{IN} = 0V	–2.5		2.5	µA
I_{IH}	Input High Current	V_{IN} = V_{DD}	–2.5		2.5	µA
C_{IN}	Input Capacitance	Except pin TCLK		5	9	pF
C_L	Load Capacitance	Pin TCLK		6		pF

3.3V AC Electrical Characteristics: T_A = 0°C to +70°C, V_{DD} = 3.3V±10%[2]

Parameter	Description	Test Condition	Min	Typ	Max	Unit[3]
f_{IN}	Input Frequency	TTL clock into TCLK	0		100	MHz
Z_{OUT}	Active Output Source Impedance			5.0		Ω
t_{ON}	Start-up Time to First Clock Cycle	Oscillator initially off			5	ms
t_{OFF}	Turnoff Time to Standby State	Oscillator initially running			4	cycles
t_{EN}	Output Enable Time	Oscillator already running			4	cycles
t_{DIS}	Output Disable Time	Oscillator stays running			4	cycles
t_R	Output Rise Edge Rate	Outputs loaded	1		4	V/ns
t_F	Output Fall Edge Rate	Outputs loaded	1		4	V/ns
t_{SR}	Output Skew Rising Edges	Same package		200	400	ps
t_{SF}	Output Skew Falling Edges	Same package		200	500	ps
t_D	Duty Cycle		45	50	55	%
t_{JA}	Jitter, Absolute	Outputs loaded			300	ps

Notes:

1. W40C06A with no output loading.
2. All AC tests are performed with 20-pF load on each clock output unless otherwise specified. Threshold voltage for timing measurements is 1.5V.
3. Unit “cycles” implies input clock cycles.

Applications Information

Series Termination

Resistors R_{S1}, R_{S2}, and R_{S3} in *Figure 3* are series termination resistors used for matching the impedance of the output buffer to the impedance of the transmission line. This is accomplished by sizing the series termination resistor value so that when added to the output buffer impedance this value matches the transmission line impedance. The resistors should be placed as close to the output pins as possible.

In *Figure 3*, output Q5 drives one line and Q3 drives two lines (for diagrammatic simplicity not all device pins are connected). As stated previously, the W40C06A exhibits a 5Ω buffer impedance when driving one 50Ω transmission line and appears to have an 8Ω–12Ω impedance when driving two transmission lines as viewed from each line). Assuming this transmission line impedance, this means that R_{S1} needs to be 45Ω and R_{S2}, R_{S3} need to be 40Ω each.

In order to drive the typical capacitive load of a CMOS input, typical transmission line impedance is 50Ω–100Ω.

Power Supply Connections

GND pins should be connected directly to the ground plane. Each V_{DD} pin should be connected to the power plane and should include a decoupling capacitor.

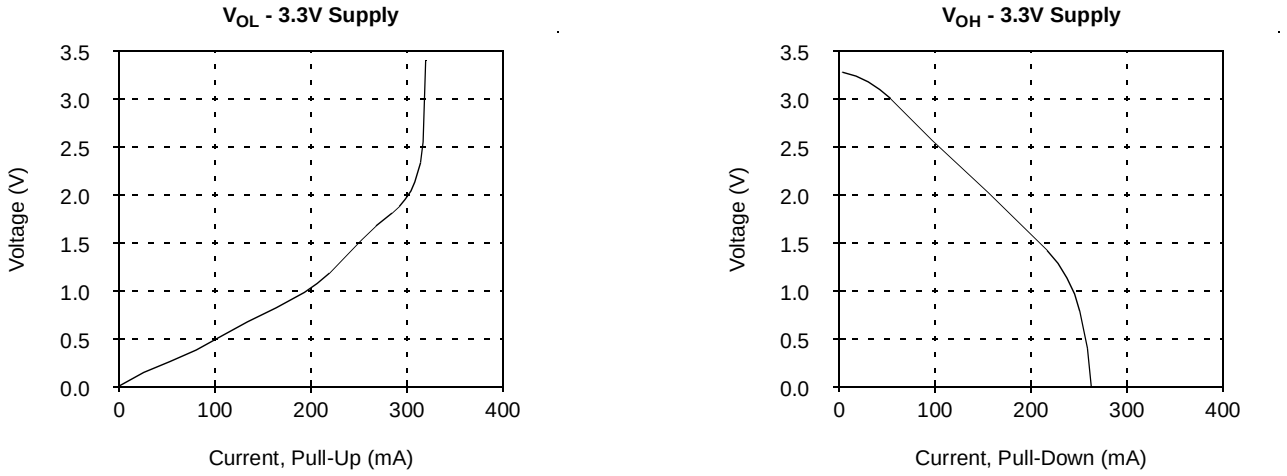


Figure 1. Typical DC Output V/I Characteristics

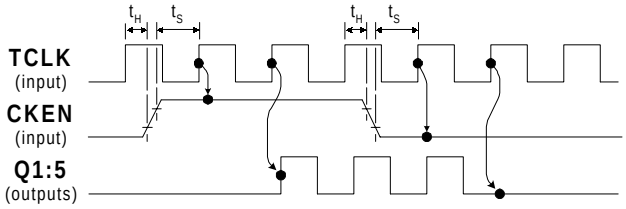


Figure 2. CKEN Timing Requirements

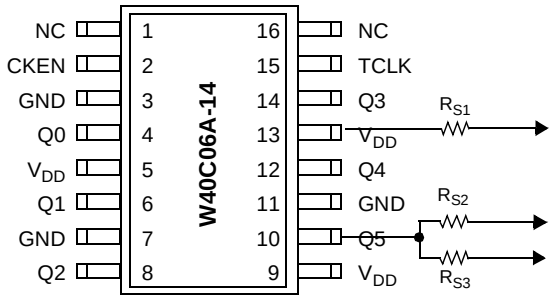


Figure 3. Application Diagram

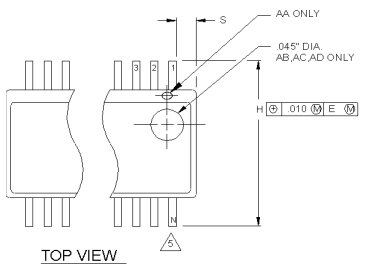
Ordering Information

Ordering Code	Freq. Mask Code	Package Name	Package Type
W40C06A	-14	H	16-pin Plastic SSOP (150-mil)

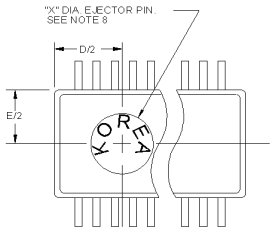
Pentium is a registered trademark of Intel Corporation.

Package Diagram

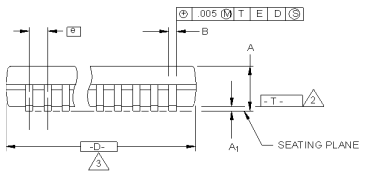
16-Pin Shrink Small Outline Package (TSSOP, 0.150 inch)



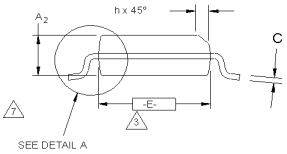
TOP VIEW



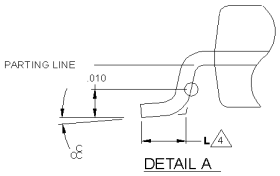
BOTTOM VIEW



SIDE VIEW



END VIEW



DETAIL A

NOTES:

1. DIMENSIONING & TOLERANCES PER ANSI Y14.5M - 1982.
2. "T" IS A REFERENCE DATUM.
3. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DOES INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE MOLD PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006 INCHES PER SIDE.
4. "L" IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
5. "N" IS THE NUMBER OF TERMINAL POSITIONS.
6. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
7. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .003 INCHES AT SEATING PLANE.
8. COUNTRY OF ORIGIN LOCATION AND EJECTOR PIN ON PACKAGE BOTTOM IS OPTIONAL AND DEPENDS ON ASSEMBLY LOCATION.
9. CONTROLLING DIMENSION: INCHES.
10. MAXIMUM DIE THICKNESS ALLOWABLE WITHOUT DIE COAT IS .016.

THIS TABLE IN INCHES

SYMBOL	COMMON DIMENSIONS			NOTE	NOTE	3						5
					VARI-	D			S			N
	MIN.	NOM.	MAX.		ATIONS	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
A	.061	.064	.068		AA	.189	.194	.196	.0020	.0045	.0070	16
A_1	.004	.006	.0098		AB	.337	.342	.344	.0500	.0525	.0550	20
A_2	.055	.058	.061		AC	.337	.342	.344	.0250	.0275	.0300	24
B	.008	.010	.012		AD	.386	.391	.393	.0250	.0280	.0300	28
C	.0075	.008	.0098									
D	SEE VARIATIONS			3								
E	.150	.155	.157									
e	.025 BSC											
H	.230	.236	.244									
h	.010	.013	.016									
L	.016	.025	.035									
N	SEE VARIATIONS			5								
S	SEE VARIATIONS											
∝	0°	5°	8°									
X	.085	.093	.100									

THIS TABLE IN MILLIMETERS

SYMBOL	COMMON DIMENSIONS			NOTE	NOTE	3						5
					VARI-	D			S			N
	MIN.	NOM.	MAX.		ATIONS	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
A	1.55	1.63	1.73		AA	4.80	4.93	4.98	0.05	0.11	0.18	16
A_1	0.127	0.15	0.25		AB	8.56	8.69	8.74	1.27	1.33	1.40	20
A_2	1.40	1.47	1.55		AC	8.56	8.69	8.74	0.64	0.70	0.76	24
B	0.20	0.25	0.31		AD	9.80	9.93	9.98	0.64	0.71	0.76	28
C	0.19	0.20	0.25									
D	SEE VARIATIONS			3								
E	3.81	3.94	3.99									
e	0.635 BSC											
H	5.84	5.99	6.20									
h	0.25	0.33	0.41									
L	0.41	0.64	0.89									
N	SEE VARIATIONS			5								
S	SEE VARIATIONS											
∝	0°	5°	8°									
X	2.16	2.36	2.54									