W42C27

Specialty Clock Generator

Features

- Supports 3.3V and 5V operation
- W42C27-36 provides the same functionality but stronger output drive than the W42C27-13 (obsolete)
- Proprietary crystal oscillator circuitry provides low REF jitter, excellent duty cycle
- Integral PLL loop filter components ensure stable PLL operation in noisy system environments
- Output clocks are TTL or CMOS-level compatible
- Custom options available with metal layer changes
- Low power CMOS design available in:
  — 8-pin SOIC (Small Outline Integrated Circuit)

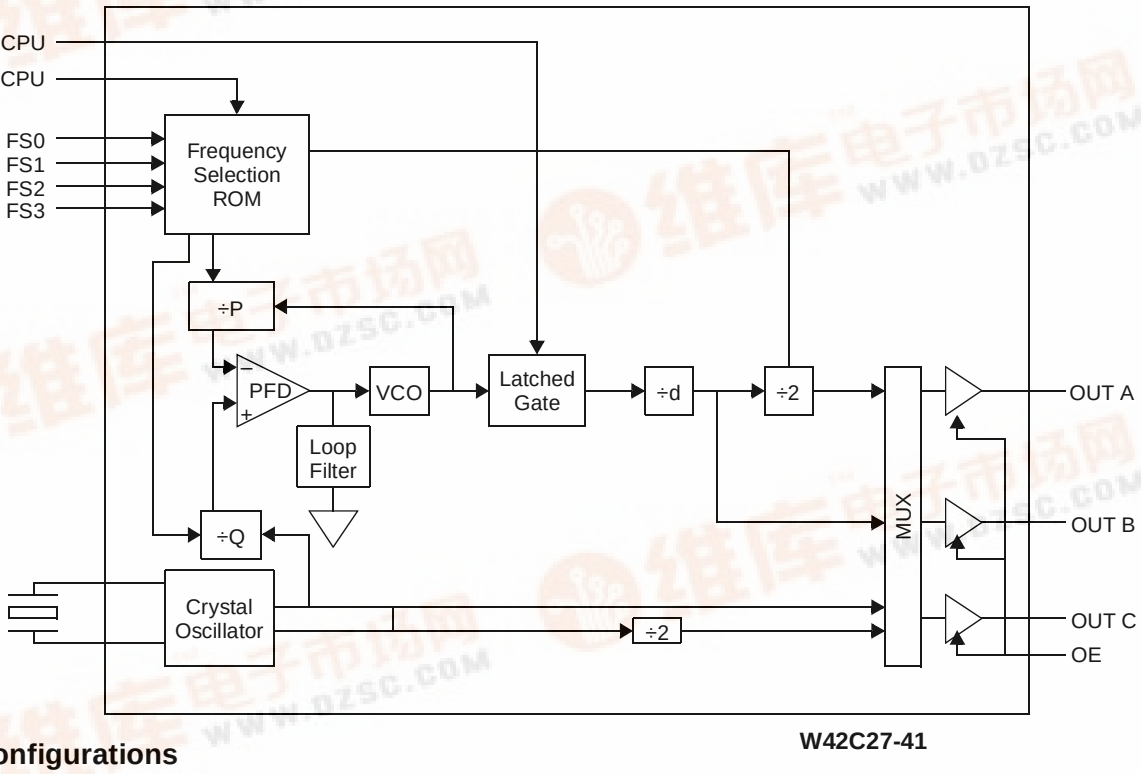
Table 1. Input/Output Frequency Selection

W42C27-41				
FS1	FS0	Reference (input)	CLK	Ratio (P/Q)
0	0	17.734	48.625	85/31
0	1	17.734	96.059	65/12
1	0	14.318	48.682	17/5
1	1	14.318	96.016	114/17

Table 2. Product Selection Guide

Part	Input (MHz)	Output (MHz)	Application
-36	17	106.25	Fibre Channel
-41	14.318	Selectable	Digital Cameras

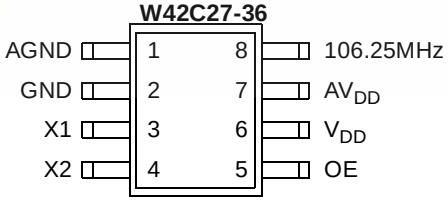
Functional Block Diagram: W42C27 Base Feature Set

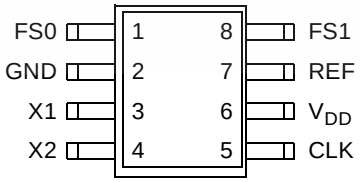


W42C27-41

Pin Configurations

W42C27-36





Pin Definitions

Pin Name	Pin Type	Pin Description
106.25MHz	O	106.25-MHz reference clock for FC-AL chipsets
AGND	G	Analog ground connection
AV_{DD}	P	Analog Power Connection
CLK	O	Clock output (refer to *Table 1* on page 1)
FS0:1	I	Frequency Selection inputs[1]
GND	G	Ground connection
OE	I	Output Enable, puts clock outputs in high-impedance state when LOW[1]
REF	O	Reference Clock output, outputs crystal or input clock frequency
V_{DD}	P	Power supply connection
X1	I	Crystal connection or external clock frequency input[1]
X2	I	Crystal connection, leave this pin unconnected when using external clock

Note:
1. All inputs, except X1/X2 have an internal pull-up resistor. Unconnected inputs will assume a logic HIGH condition.

Overview

The W42C27 is a general-purpose device that features a single phase-locked loop. Through the use of metal masks, the chip can be tailored to a wide variety of applications.

The W42C27 can have up to three output frequencies. A wide variety of input functions are available through mask options.

W42C27-36 Option Description

The standard W42C27-36 option provides a fixed 106.25-MHz clock output that is useful in FC-AL (Fiber Channel Arbitrated Loop) applications. FC-AL chip sets, such as the Vitesse VSC7105/7106, require a 106.25-MHz input reference clock.

Unlike other Cypress clock products, the W42C27-36 requires a 17.0-MHz crystal or reference clock source. To maintain the 106.25-MHz ±50 ppm accuracy required by FC-AL applications, the 17.0-MHz crystal needs to be controlled to within ±50 ppm (the 106.25-MHz output is derived by the PLL ratio of 25/4 x 17.0 MHz). To facilitate precise frequency control of the crystal oscillator, external crystal load capacitors are used and required with the W42C27-36 option; no internal load capacitors are implemented at device pin X1 and X2 (again unlike other Cypress clock devices). The required load capacitance value for accurate crystal oscillation frequency is specified by the crystal manufacturer. Stray capacitance of X1 and X2 is about 5 pF.

Improved Crystal Oscillator Circuit

The W42C27 incorporates a new crystal oscillator circuit designed to provide 50% duty cycle over a range of operating conditions including the addition of external crystal load capacitors to pins X1 and X2. (Crystal load capacitance is sometimes increased to match a particular crystal load requirement when absolute frequency accuracy is important.) Duty cycle is also maintained when using an external clock source (connected to pin X1, pin X2 is left open), as long as the external clock has good duty cycle.

Crystal load capacitance of the W42C27 is about 10 pF (excluding the W42C27-36 option), which is becoming an industry standard. This helps to control frequency accuracy, assuming that a crystal which specifies a 10-pF load condition is used. The circuit exhibits about 50% less clock jitter from the REF output when compared to similar devices.

Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability

Parameter	Description	Rating	Unit
V_{DD}, V_{IN}	Voltage on any pin with respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Operating Temperature	0 to +70	°C
T_B	Ambient Temperature under Bias	–55 to +125	°C

Electrical Characteristics at 5.0V

DC Electrical Characteristics: T_A = 0°C to +70°C; V_{DD} = 5V ± 10%

Parameter	Description	Conditions	Min	Typ	Max	Unit
I_{DD}	Operating Supply Current	Note 2			25	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage		2.0			V
V_{OL}	Output Low Voltage	I_{OL} = 8 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = –0.1 mA	V_{DD} – 0.4V			V
V_{OH}	Output High Voltage	I_{OH} = –4 mA	2.4			V
C_I	Input Capacitance	Except X1, X2			10	pF
C_L	Load Capacitance	Pins X1, X2 (except for -36)		10		pF
I_{IL}	Input Low Current	V_{IN} = 0V (includes pull-up resistor)			–100	µA
I_{IH}	Input High Current	V_{IN} = V_{DD}			10	µA
R_P	Input Pull-Up Resistor	V_{IN} = 0V		250		kΩ

AC Characteristics: T_A = 0°C to +70°C; V_{DD} = 5V ± 10%

Parameter	Description	Min	Typ	Max	Unit
F_O	Output Frequency	2		120	MHz
F_I	Input Frequency	2	14.318	32	MHz
T_R	Output Rise Time, 0.8 to 2.0V, 25-pF Load		1	2	ns
T_R	Output Rise Time, 20 to 80% V_{CC}, 25-pF Load		2	4	ns
T_F	Output Fall Time, 2.0 to 0.8V, 25-pF Load		1	2	ns
T_F	Output Fall Time, 80 to 20% V_{CC}, 25-pF Load		2	4	ns
D_T	Duty Cycle, 15-pF Load	40	50	60	%
T_{J1S}	Jitter, 1 Sigma, All Frequencies			±150	ps
T_{JABS}	Jitter, Absolute, All Frequencies			±250	ps
T_{PU}	Powerup Time, Off to stated output frequency		15	30	ms

Note:

2. W42C27 with no load. Power supply current varies with frequency.

Electrical Characteristics at 3.3V

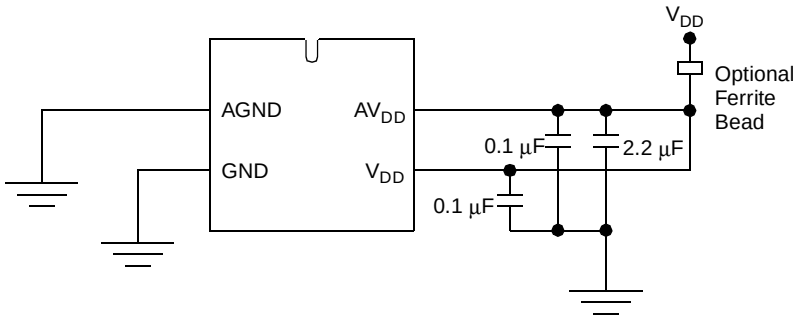
DC Electrical Characteristics: T_A = 0°C to +70°C; V_{DD} = 3.3V ± 5%

Parameter	Description	Conditions	Min	Typ	Max	Unit
I_{DD}	Operating Supply Current	Note 2			20	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage		2.0			V
V_{OL}	Output Low Voltage	I_{OL} = 8 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4 mA	2.4			V
C_I	Input Capacitance	Except X1, X2			10	pF
C_L	Load Capacitance	Pins X1, X2		10		pF
I_{IL}	Input Low Current	V_{IN} = 0V (includes pull-up resistor)			–100	µA
I_{IH}	Input High Current	V_{IN} = V_{DD}			10	µA
R_P	Input Pull-Up Resistor	V_{IN} = 0V		250		kΩ

AC Characteristics: T_A = 0°C to +70°C; V_{DD} = 3.3V ± 5%

Parameter	Description	Min	Typ	Max	Unit
F_O	Output Frequency	2		110	MHz
F_I	Input Frequency	2	14.318	32	MHz
$ICLK_R$	Input Clock Rise Time			20	ns
$ICLK_F$	Input Clock Fall Time			20	ns
T_R	Output Rise Time, 20 to 80% V_{CC}, 25-pF Load		2	4	ns
T_F	Output Fall Time, 80 to 20% V_{CC}, 25-pF Load		2	4	ns
D_T	Duty Cycle, 15-pF Load	40	50	60	%
T_{J1S}	Jitter, 1 Sigma, All Frequencies			±150	ps
T_{JABS}	Jitter, Absolute, All Frequencies			±250	ps
T_{PU}	Powerup Time, Off to stated output frequency		15	30	ms

Recommended Circuit Configuration



Recommended Circuit Configuration

For optimum performance in system applications, the above power supply decoupling scheme should be used. GND pins are connected directly to the ground plane.

V_{DD} decoupling is important to reduce phase jitter and EMI radiation. The 0.1-µF decoupling capacitor should be placed as close to the V_{DD} pins as possible, otherwise the increased trace inductance will negate its decoupling capability. The 2.2-µF decoupling capacitor shown is optional but will improve power supply rejection. For further EMI protection, the V_{DD} connection can be made via a ferrite bead, as shown.

When using the W42C27, unused input select pins may be tied to either ground or V_{DD}, or may be left unconnected. Since internal pull-up resistors are incorporated on all logic input pins, an unconnected input will assume a logic 1 condition. Output clocks should use a series termination resistor (about 33Ω) placed as close to the clock outputs as possible; this will also help to decrease jitter, EMI and clock signal ringing.

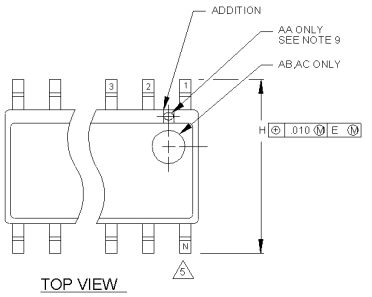
Ordering Information

Ordering Code	Freq. Mask Code	Package Name	Package Type
W42C27	36, 41	G	8-pin SOIC (150-mil)

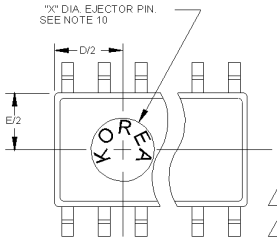
Document #: 38-00804

Package Diagrams

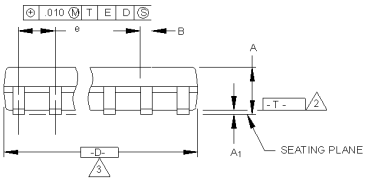
8-Pin Small Outline Integrated Circuit, Narrow (SOIC, 0.150 inch)



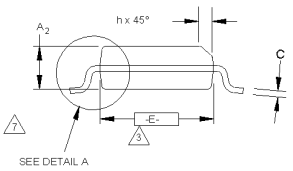
TOP VIEW



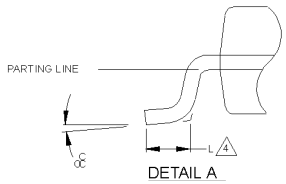
BOTTOM VIEW



SIDE VIEW



END VIEW



DETAIL A

NOTES:

1. MAXIMUM DIE THICKNESS ALLOWABLE IS .015.
2. DIMENSIONING & TOLERANCES PER ANSI.Y14.5M - 1982.
3. "T" IS A REFERENCE DATUM.
4. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DOES INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE MOLD PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. "L" IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. "N" IS THE NUMBER OF TERMINAL POSITIONS.
7. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
8. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .003 INCHES AT SEATING PLANE.
9. THE APPEARANCE OF PIN #1 I.D ON THE 8 LD IS OPTIONAL, ROUND TYPE ON SINGLE LEADFRAME AND RECTANGULAR TYPE ON MATRIX LEADFRAME.
10. COUNTRY OF ORIGIN LOCATION AND EJECTOR PIN ON PACKAGE BOTTOM IS OPTIONAL AND DEPEND ON ASSEMBLY LOCATION.
11. CONTROLLING DIMENSION: INCHES.

THIS TABLE IN INCHES

SYMBOL	COMMON DIMENSIONS			NOTE	NOTE VARI-ATIONS	3 D			5 N
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
A	.061	.064	.068		AA	.189	.194	.196	8
A_1	.004	.006	.0098		AB	.337	.342	.344	14
A_2	.055	.058	.061		AC	.386	.391	.393	16
B	.0138	.016	.0192						
C	.0075	.008	.0098						
D	SEE VARIATIONS			3					
E	.150	.155	.157						
e	.050 BSC								
H	.230	.236	.244						
h	.010	.013	.016						
L	.016	.025	.035						
N	SEE VARIATIONS			5					
α	0°	5°	8°						
X	.085	.093	.100						

THIS TABLE IN MILLIMETERS

SYMBOL	COMMON DIMENSIONS			NOTE	NOTE VARI-ATIONS	3 D			5 N
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
A	1.55	1.63	1.73		AA	4.80	4.93	4.98	8
A_1	0.127	0.15	0.25		AB	8.58	8.69	8.74	14
A_2	1.40	1.47	1.55		AC	9.80	9.93	9.98	16
B	0.35	0.41	0.49						
C	0.19	0.20	0.25						
D	SEE VARIATIONS			3					
E	3.81	3.94	3.99						
e	1.27 BSC								
H	5.84	5.99	6.20						
h	0.25	0.33	0.41						
L	0.41	0.64	0.89						
N	SEE VARIATIONS			5					
α	0°	5°	8°						
X	2.16	2.36	2.54						