



PRELIMINARY

CY7C09349
CY7C09359

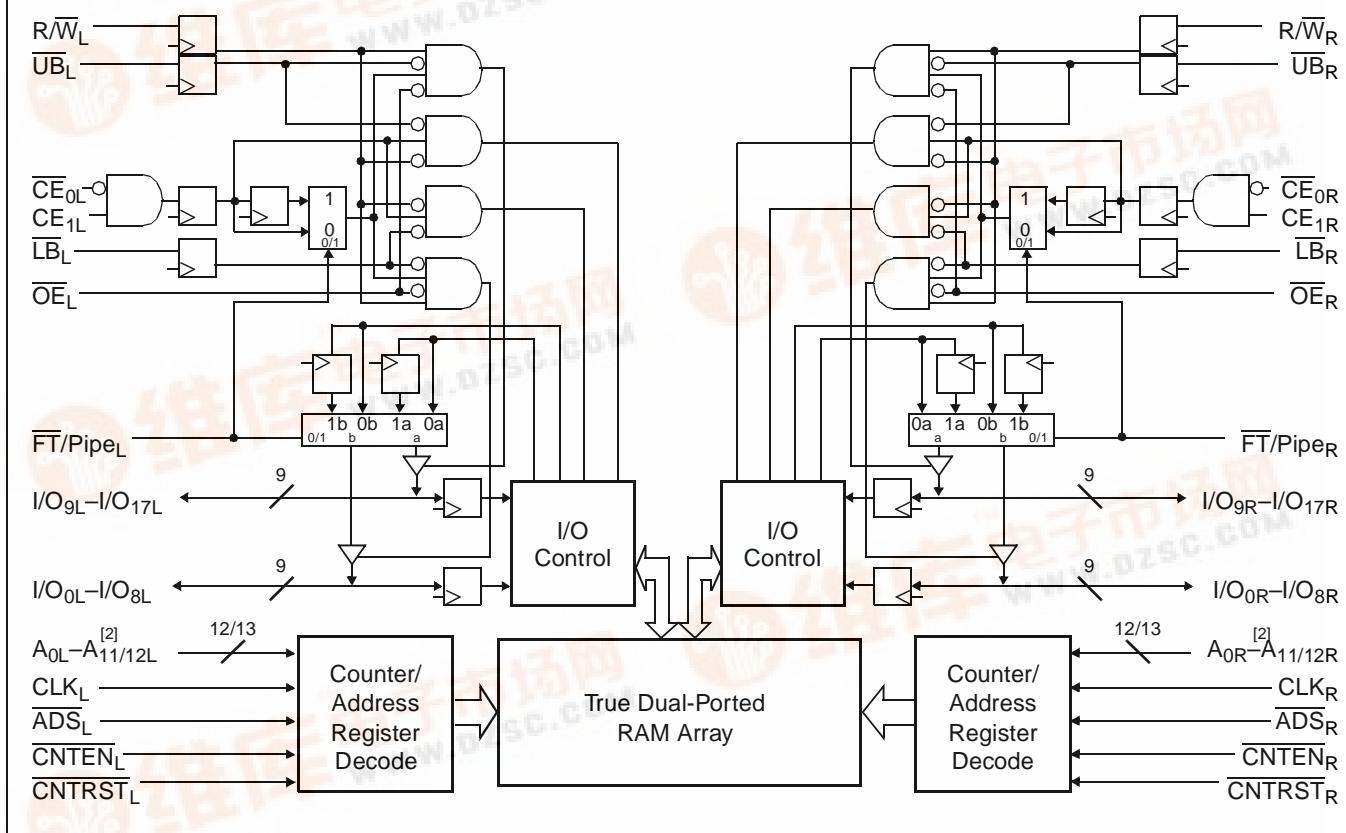
4K/8K x 18 Synchronous Dual-Port Static RAM

Features

- True dual-ported memory cells which allow simultaneous access of the same memory location
- Two Flow-Through/Pipelined devices
 - 4K x 18 organization (CY7C09349)
 - 8K x 18 organization (CY7C09359)
- Three Modes
 - Flow-Through
 - Pipelined
 - Burst
- Pipelined output mode on both ports allows fast 100-MHz cycle time
- 0.35-micron CMOS for optimum speed/power

- High-speed clock to data access 6.5^[1]/7.5/9/12 ns (max.)
- Low operating power
 - Active = 200 mA (typical)
 - Standby = 0.05 mA (typical)
- Fully synchronous interface for easier operation
- Burst counters increment addresses internally
 - Shorten cycle times
 - Minimize bus noise
 - Supported in Flow-Through and Pipelined modes
- Dual Chip enables for easy depth expansion
- Upper and lower byte controls for bus matching
- Automatic power-down
- Commercial and Industrial temperature ranges
- Available in 100-pin TQFP

Logic Block Diagram



Notes:

- See page 6 for Load Conditions.
- $A_0 - A_{11}$ for 4K; $A_0 - A_{12}$ for 8K devices.



Functional Description

The CY7C09349 and CY7C09359 are high-speed synchronous CMOS 4K and 8K x 18 dual-port static RAMs. Two ports are provided, permitting independent, simultaneous access for reads and writes to any location in memory.^[3] Registers on control, address, and data lines allow for minimal set-up and hold times. In pipelined output mode, data is registered for decreased cycle time. Clock to data valid $t_{CD2} = 6.5$ ns^[1] (pipelined). Flow-through mode can also be used to bypass the pipelined output register to eliminate access latency. In flow-through mode data will be available $t_{CD1} = 15$ ns after the address is clocked into the device. Pipelined output or flow-through mode is selected via the $\overline{FT}/\overline{Pipe}$ pin.

Each port contains a burst counter on the input address register. The internal write pulse width is independent of the LOW-to-HIGH transition of the clock signal. The internal write pulse is self-timed to allow the shortest possible cycle times.

A HIGH on \overline{CE}_0 or LOW on CE_1 for one clock cycle will power down the internal circuitry to reduce the static power consumption. The use of multiple Chip Enables allows easier banking of multiple chips for depth expansion configurations. In the pipelined mode, one cycle is required with \overline{CE}_0 LOW and CE_1 HIGH to reactivate the outputs.

Counter enable inputs are provided to stall the operation of the address input and utilize the internal address generated by the internal counter for fast interleaved memory applications. A port's burst counter is loaded with the port's Address Strobe (\overline{ADS}). When the port's Count Enable (\overline{CNTEN}) is asserted, the address counter will increment on each LOW-to-HIGH transition of that port's clock signal. This will read/write one word from/into each successive address location until $CNTEN$ is deasserted. The counter can address the entire memory array and will loop back to the start. Counter Reset ($CNTRST$) is used to reset the burst counter.

All parts are available in 100-pin Thin Quad Plastic Flatpack (TQFP) packages.

Note:

3. When simultaneously writing to the same location, final value cannot be determined.

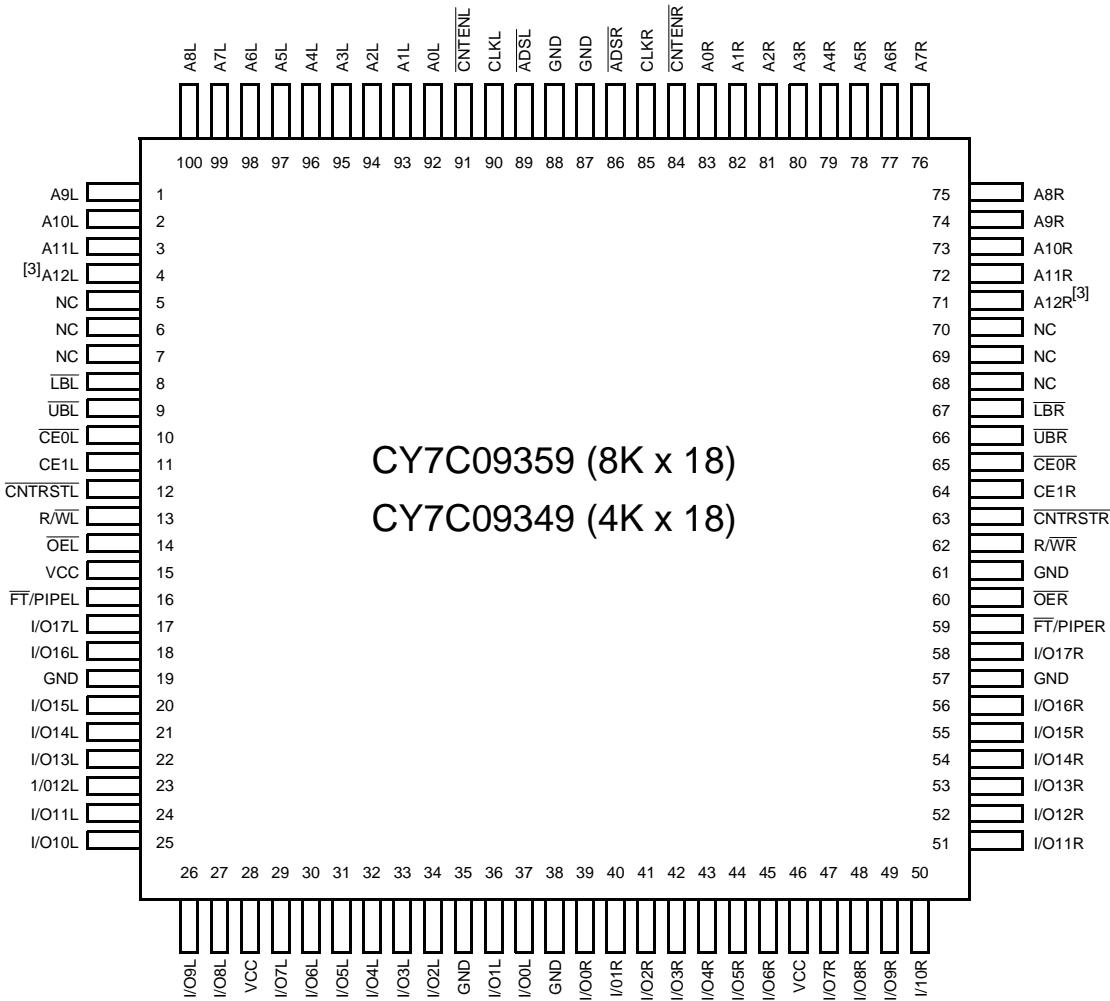


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Pin Configuration

100-Pin TQFP (Top View)



Selection Guide

	CY7C09349 CY7C09359 -6^[1]	CY7C09349 CY7C09359 -7	CY7C09349 CY7C09359 -9	CY7C09349 CY7C09359 -12
f _{MAX2} (MHz) (Pipelined)	100	83	67	50
Max. Access Time (ns) (Clock to Data, Pipelined)	6.5	7.5	9	12
Typical Operating Current I _{CC} (mA)	250	235	215	195
Typical Standby Current for I _{SB1} (mA) (Both Ports TTL Level)	45	40	35	30
Typical Standby Current for I _{SB3} (mA) (Both Ports CMOS Level)	0.05	0.05	0.05	0.05

Note:

4. This pin is NC for CY7C09349.

**Pin Definitions**

Left Port	Right Port	Description
A _{0L} –A _{12L}	A _{0R} –A _{12R}	Address Inputs (A ₀ –A ₁₁ for 4K, A ₀ –A ₁₂ for 8K devices).
ADS _L	ADS _R	Address Strobe Input. Used as an address qualifier. This signal should be asserted LOW during normal read or write transactions. Asserting this signal LOW also loads the burst address counter with data present on the I/O pins.
CE _{0L} ,CE _{1L}	CE _{0R} ,CE _{1R}	Chip Enable Input. To select either the left or right port, both CE ₀ AND CE ₁ must be asserted to their active states (CE ₀ ≤ V _{IL} and CE ₁ ≥ V _{IH}).
CLK _L	CLK _R	Clock Signal. This input can be free running or strobed. Maximum clock input rate is f _{MAX} .
CNTEN _L	CNTEN _R	Counter Enable Input. Asserting this signal <u>LOW</u> increments the burst address counter of its respective port on each rising edge of CLK. CNTEN is disabled if ADS or CNTRST are asserted LOW.
CNTRST _L	CNTRST _R	Counter Reset Input. Asserting this signal <u>LOW</u> resets the burst address counter of its respective port to zero. CNTRST is not disabled by asserting ADS or CNTEN.
I/O _{0L} –I/O _{17L}	I/O _{0R} –I/O _{17R}	Data Bus Input/Output (I/O ₀ –I/O ₁₅ for x16 devices).
LB _L	LB _R	Lower Byte Select Input. Asserting this signal <u>LOW</u> enables read and write operations to the lower byte (I/O ₀ –I/O ₈ for x18, I/O ₀ –I/O ₇ for x16) of the memory array. For read operations both the LB and OE signals must be asserted to drive output data on the lower byte of the data pins.
UB _L	UB _R	Upper Byte Select Input. Same function as LB, but to the upper byte (I/O _{8/9L} –I/O _{15/17L}).
OE _L	OE _R	Output Enable Input. This signal must be asserted <u>LOW</u> to enable the I/O data pins during read operations.
R/W _L	R/W _R	Read/Write Enable Input. This signal is asserted <u>LOW</u> to write to the dual port memory array. For read operations, assert this pin <u>HIGH</u> .
FT/PIPE _L	FT/PIPE _R	Flow-Through/Pipelined Select Input. For flow-through mode operation, assert this pin <u>LOW</u> . For pipelined mode operation, assert this pin <u>HIGH</u> .
GND		Ground Input.
NC		No Connect.
V _{CC}		Power Input.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature –65°C to +150°C

Ambient Temperature with Power Applied .. –55°C to +125°C

Supply Voltage to Ground Potential –0.3V to +7.0V

DC Voltage Applied to Outputs in High Z State –0.5V to +7.0V

DC Input Voltage..... –0.5V to +7.0V

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage >2001V

Latch-Up Current..... >200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	–40°C to +85°C	5V ± 10%

Shaded areas contain advance information.



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Electrical Characteristics Over the Operating Range

Parameter	Description	CY7C09349 CY7C09359												Unit	
		-6 ^[1]			-7			-9			-12				
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
V _{OH}	Output HIGH Voltage (V _{CC} = Min., I _{OH} = -4.0 mA)	2.4			2.4			2.4			2.4			V	
V _{OL}	Output LOW Voltage (V _{CC} = Min., I _{OH} = +4.0 mA)			0.4				0.4			0.4			0.4 V	
V _{IH}	Input HIGH Voltage	2.2			2.2			2.2			2.2			V	
V _{IL}	Input LOW Voltage			0.8				0.8			0.8			0.8 V	
I _{OZ}	Output Leakage Current	-10			10	-10					10	-10		10 μA	
I _{CC}	Operating Current (V _{CC} = Max, I _{OUT} = 0 mA) Outputs Disabled	Com'l. Ind.	250	450		235	420		215	360		195	300	mA	
I _{SB1}	Standby Current (Both Ports TTL Level) ^[5] CE _L & CE _R ≥ V _{IH} , f = f _{MAX}	Com'l. Ind.	45	115		40	105		35	95		30	85	mA	
I _{SB2}	Standby Current (One Port TTL Level) ^[5] CE _L CE _R ≥ V _{IH} , f = f _{MAX}	Com'l. Ind.	175	235		160	220		145	205		125	190	mA	
I _{SB3}	Standby Current (Both Ports CMOS Level) ^[5] CE _L & CE _R ≥ V _{CC} − 0.2V, f = 0	Com'l. Ind.	0.05	0.5		0.05	0.5		0.05	0.5		0.05	0.5	mA	
I _{SB4}	Standby Current (One Port CMOS Level) ^[5] CE _L CE _R ≥ V _{IH} , f = f _{MAX}	Com'l. Ind.	160	200		145	185		130	170		110	150	mA	
						160	200		145	185		125	165	mA	

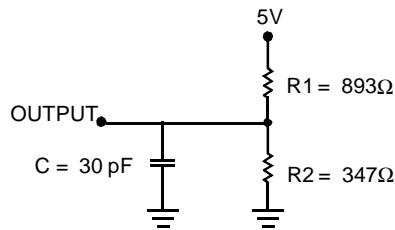
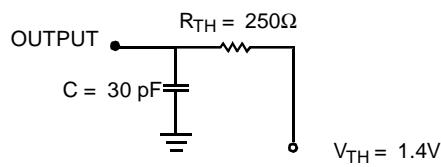
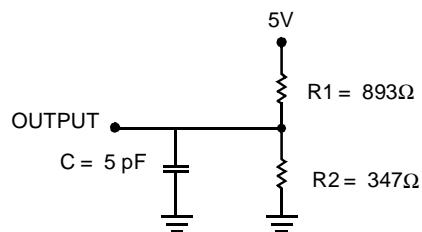
Shaded areas contain advance information.

Capacitance

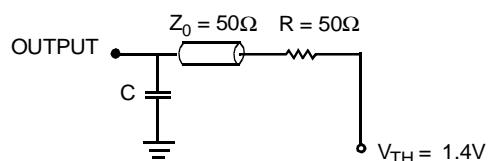
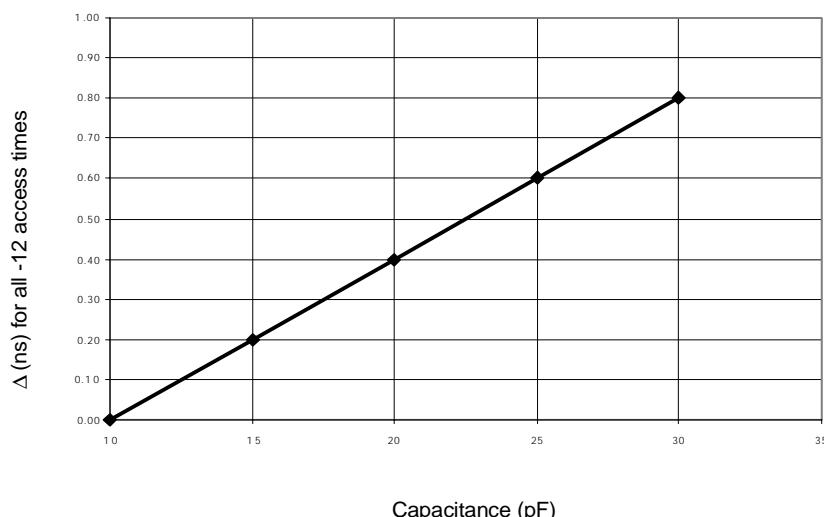
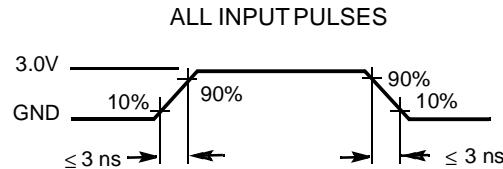
Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	10	pF
C _{OUT}	Output Capacitance		10	pF

Note:

5. CE_L and CE_R are internal signals. To select either the left or right port, both CE₀ AND CE₁ must be asserted to their active states (CE₀ ≤ V_{IL} and CE₁ ≥ V_{IH}).

AC Test Loads

(a) Normal Load (Load 1)

(b) Thévenin Equivalent (Load 1)

(c) Three-State Delay (Load 2)

(Used for t_{CKLZ} , t_{OLZ} , & t_{OHZ} including scope and jig)

AC Test Loads (Applicable to -6 only)^[6]

(a) Load 1 (-6 only)

(b) Load Derating Curve
Note:

6. Test Conditions: $C = 10 \text{ pF}$.



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Switching Characteristics Over the Operating Range

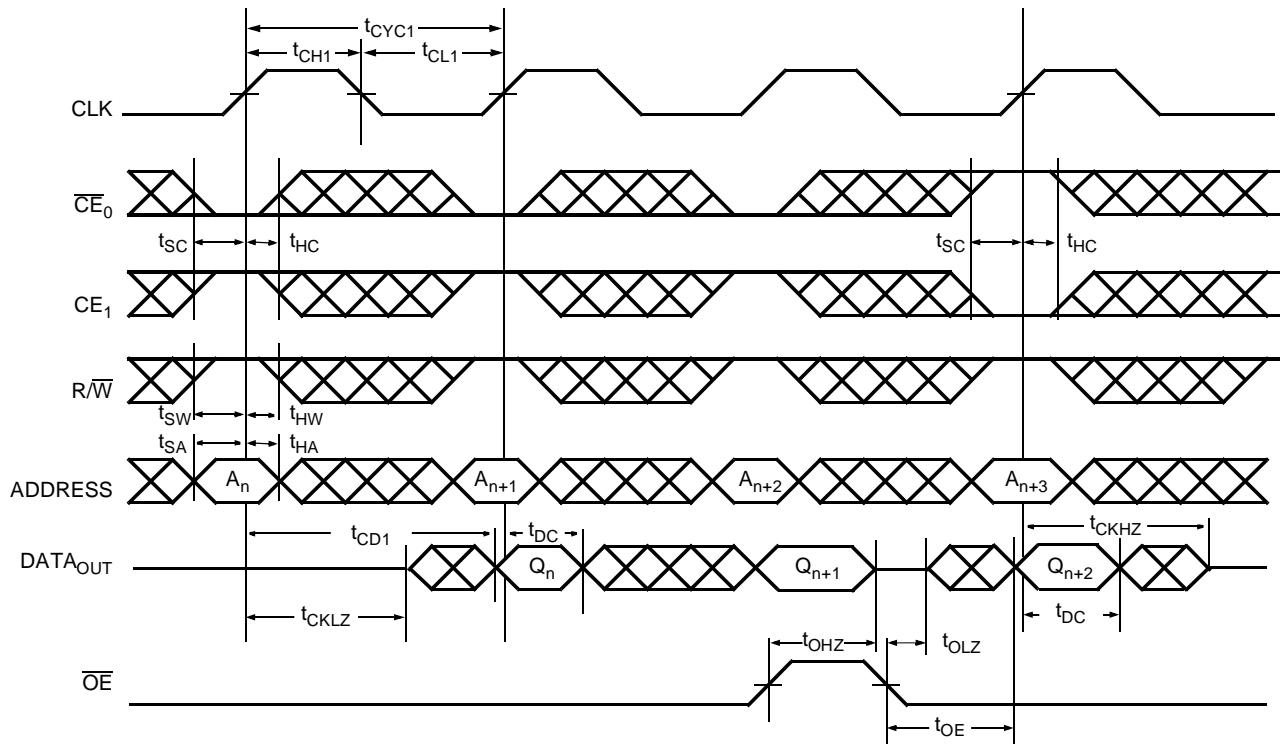
Parameter	Description	CY7C09349 CY7C09359								Unit	
		-6 ^[1]		-7		-9		-12			
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
f _{MAX1}	f _{Max} Flow-Through		53		45		40		33	MHz	
f _{MAX2}	f _{Max} Pipelined		100		83		67		50	MHz	
t _{CYC1}	Clock Cycle Time - Flow-Through	19		22		25		30		ns	
t _{CYC2}	Clock Cycle Time - Pipelined	10		12		15		20		ns	
t _{CH1}	Clock HIGH Time - Flow-Through	6.5		7.5		12		12		ns	
t _{CL1}	Clock LOW Time - Flow-Through	6.5		7.5		12		12		ns	
t _{CH2}	Clock HIGH Time - Pipelined	4		5		6		8		ns	
t _{CL2}	Clock LOW Time - Pipelined	4		5		6		8		ns	
t _R	Clock Rise Time		3		3		3		3	ns	
t _F	Clock Fall Time		3		3		3		3	ns	
t _{SA}	Address Set-up Time	3.5		4		4		4		ns	
t _{HA}	Address Hold Time	0		0		1		1		ns	
t _{SC}	Chip Enable Set-up Time	3.5		4		4		4		ns	
t _{HC}	Chip Enable Hold Time	0		0		1		1		ns	
t _{SW}	R/W Set-up Time	3.5		4		4		4		ns	
t _{HW}	R/W Hold Time	0		0		1		1		ns	
t _{SD}	Input Data Set-up Time	3.5		4		4		4		ns	
t _{HD}	Input Data Hold Time	0		0		1		1		ns	
t _{SAD}	ADS Set-up Time	3.5		4		4		4		ns	
t _{HAD}	ADS Hold Time	0		0		1		1		ns	
t _{SCN}	CNTEN Set-up Time	3.5		4		4		4		ns	
t _{HCN}	CNTEN Hold Time	0		0		1		1		ns	
t _{SRST}	CNTRST Set-up Time	3.5		4		4		4		ns	
t _{HRST}	CNTRST Hold Time	0		0		1		1		ns	
t _{OE}	Output Enable to Data Valid		8		9		10		12	ns	
t _{OLZ} ^[7]	OE to Low Z	2		2		2		2		ns	
t _{OHZ} ^[7]	OE to High Z	1	7	1	7	1	7	1	7	ns	
t _{CD1}	Clock to Data Valid - Flow-Through		15		18		20		25	ns	
t _{CD2}	Clock to Data Valid - Pipelined		6.5		7.5		9		12	ns	
t _{DC}	Data Output Hold After Clock HIGH	2		2		2		2		ns	
t _{CKHZ}	Clock HIGH to Output High Z	2	9	2	9	2	9	2	9	ns	
t _{CKLZ} ^[7]	Clock HIGH to Output Low Z	2		2		2		2		ns	
Port to Port Delays											
t _{CWDD}	Write Port Clock HIGH to Read Data Delay		30		35		40		40	ns	
t _{CCS}	Clock to Clock Set-up Time		9		10		15		15	ns	

Notes:

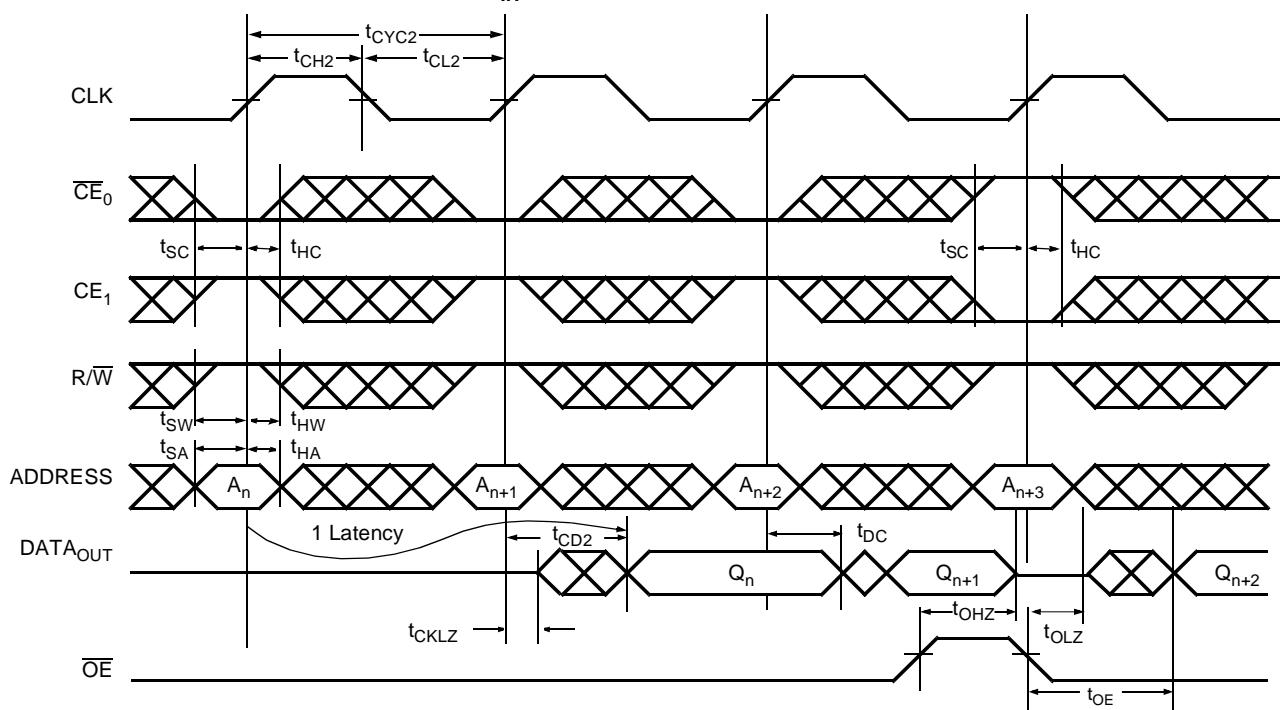
7. Test conditions used are Load 2.

Switching Waveforms

Read Cycle for Flow-Through Output ($\overline{FT}/PIPE = V_{IL}$)^[8, 9, 10, 11]

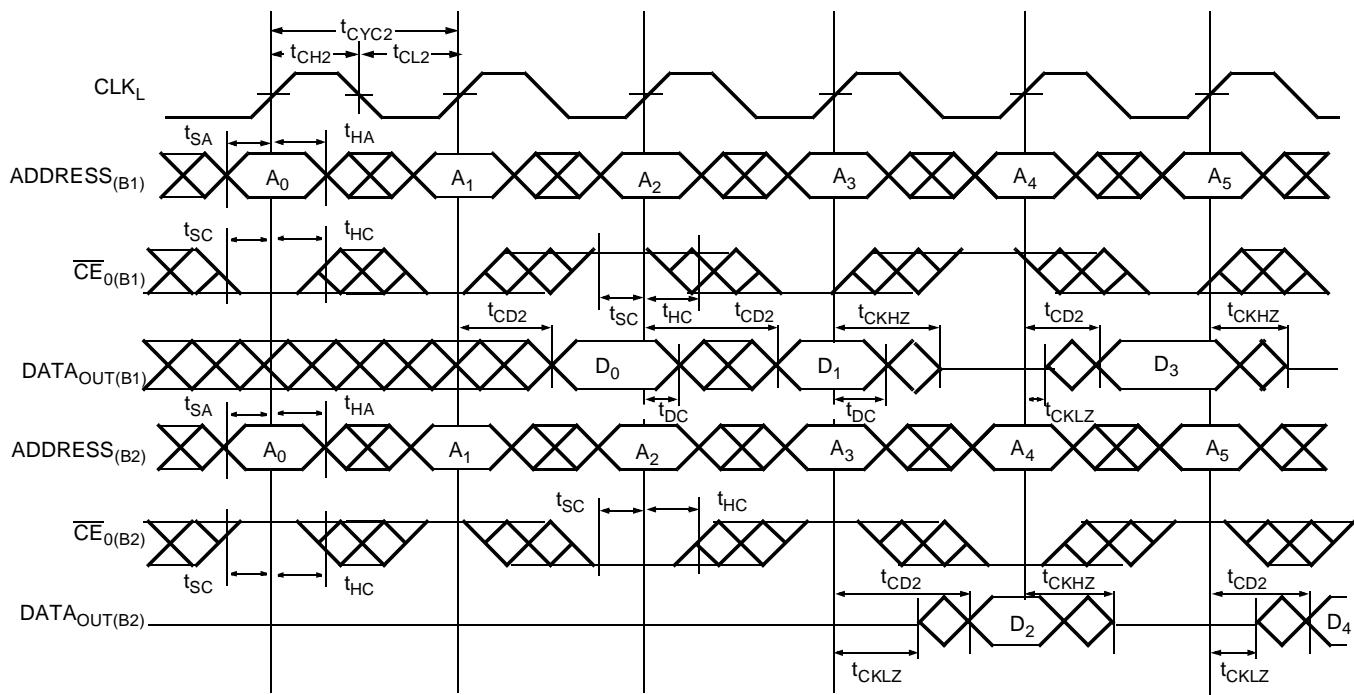
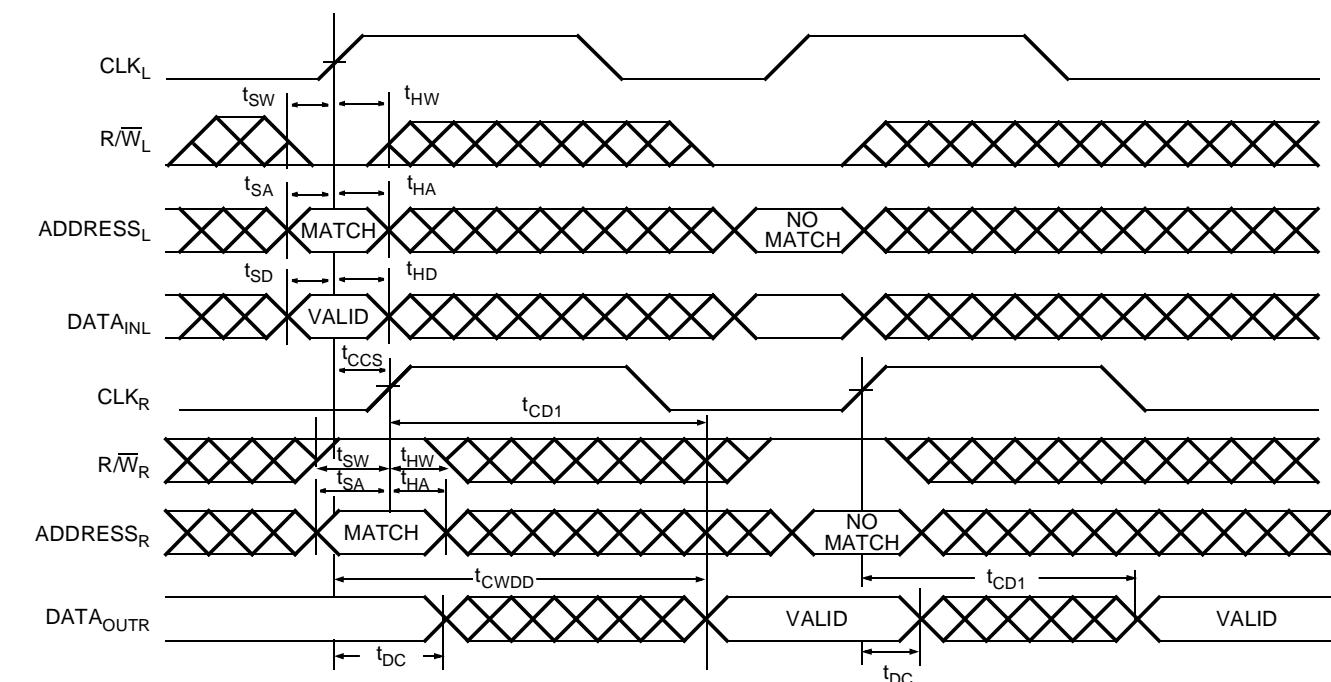


Read Cycle for Pipelined Operation ($\overline{FT}/PIPE = V_{IH}$)^[8, 9, 10, 11]

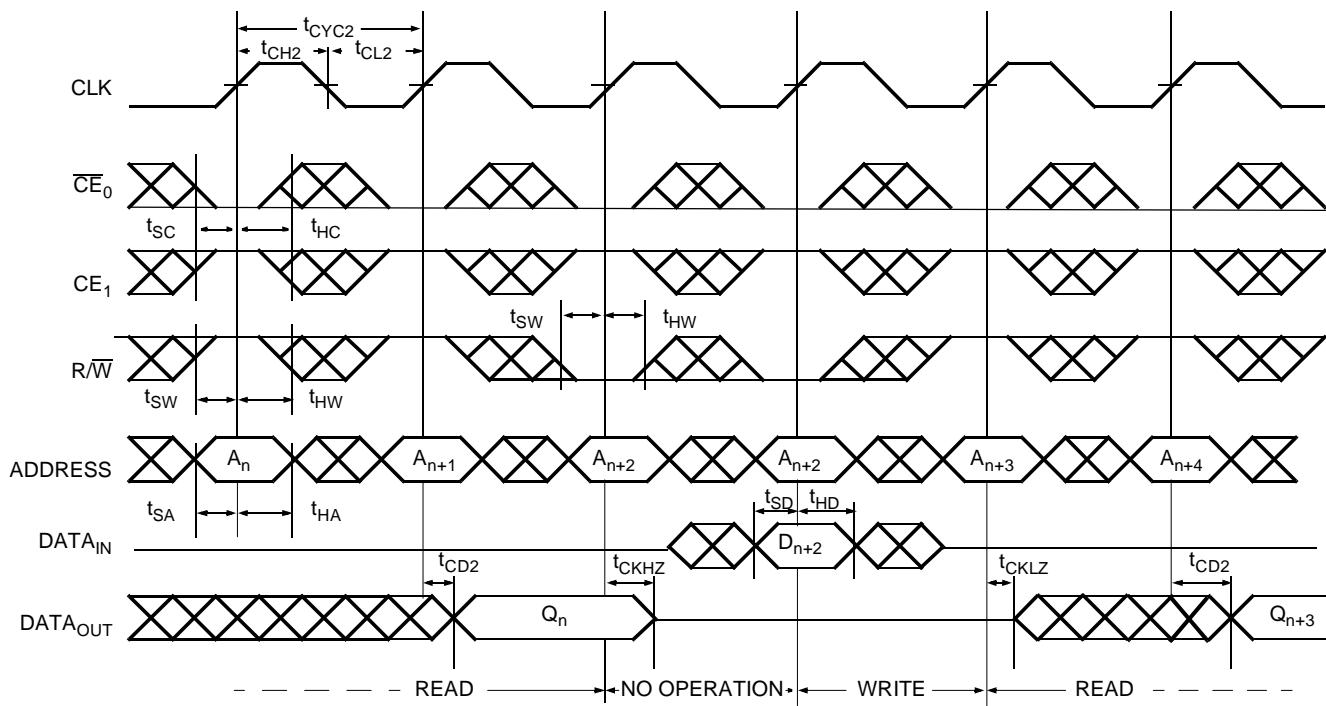
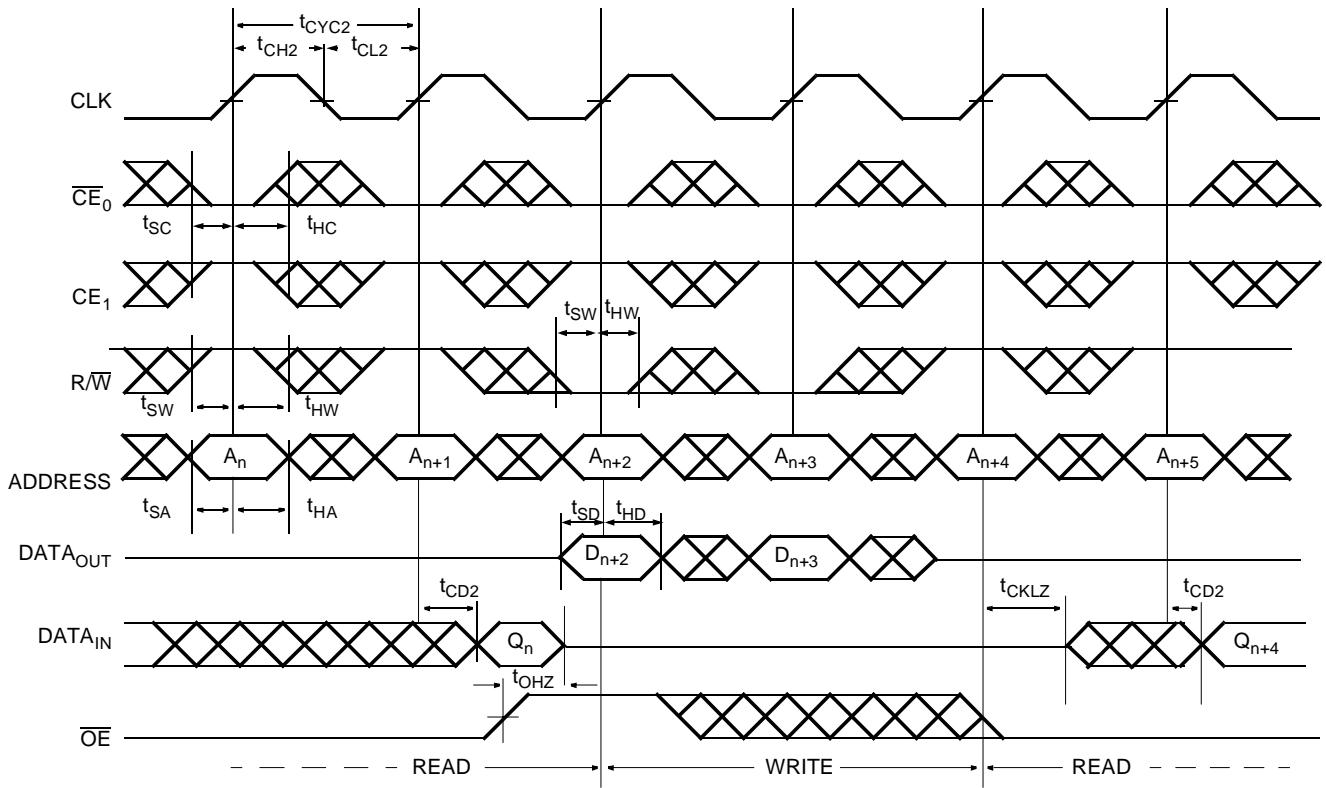


Notes:

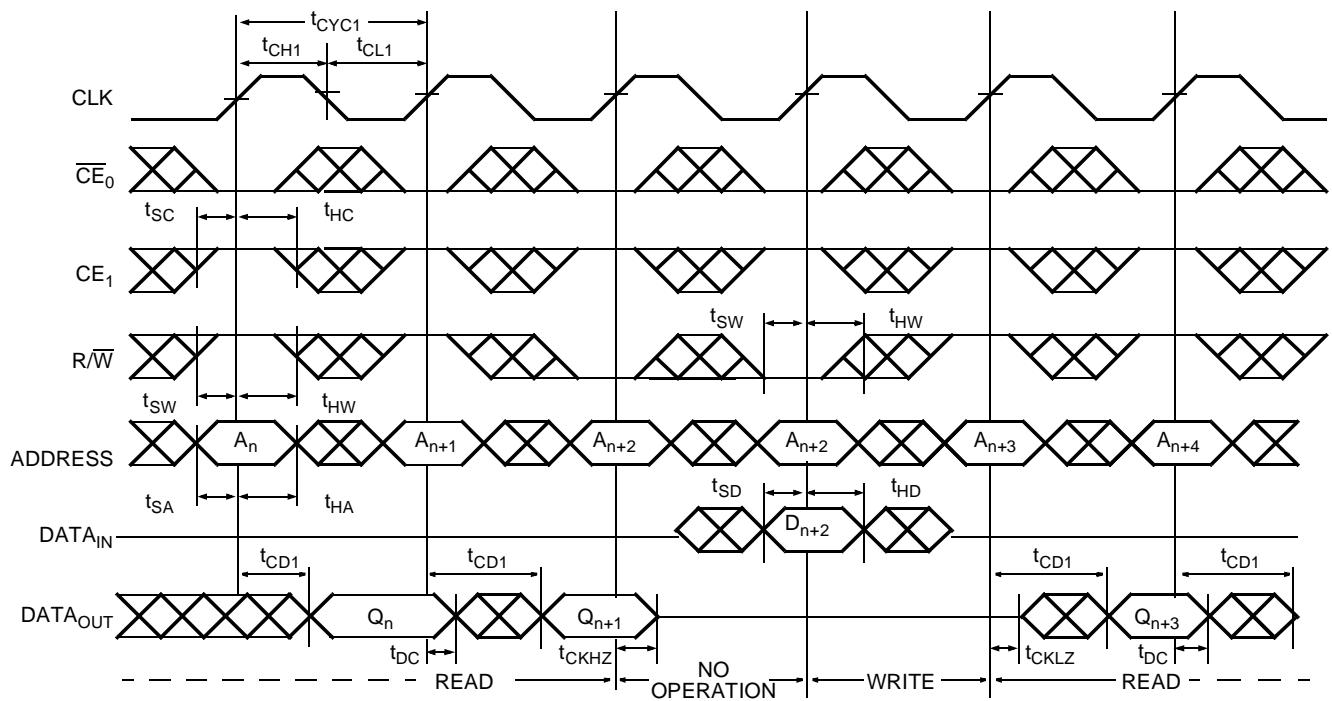
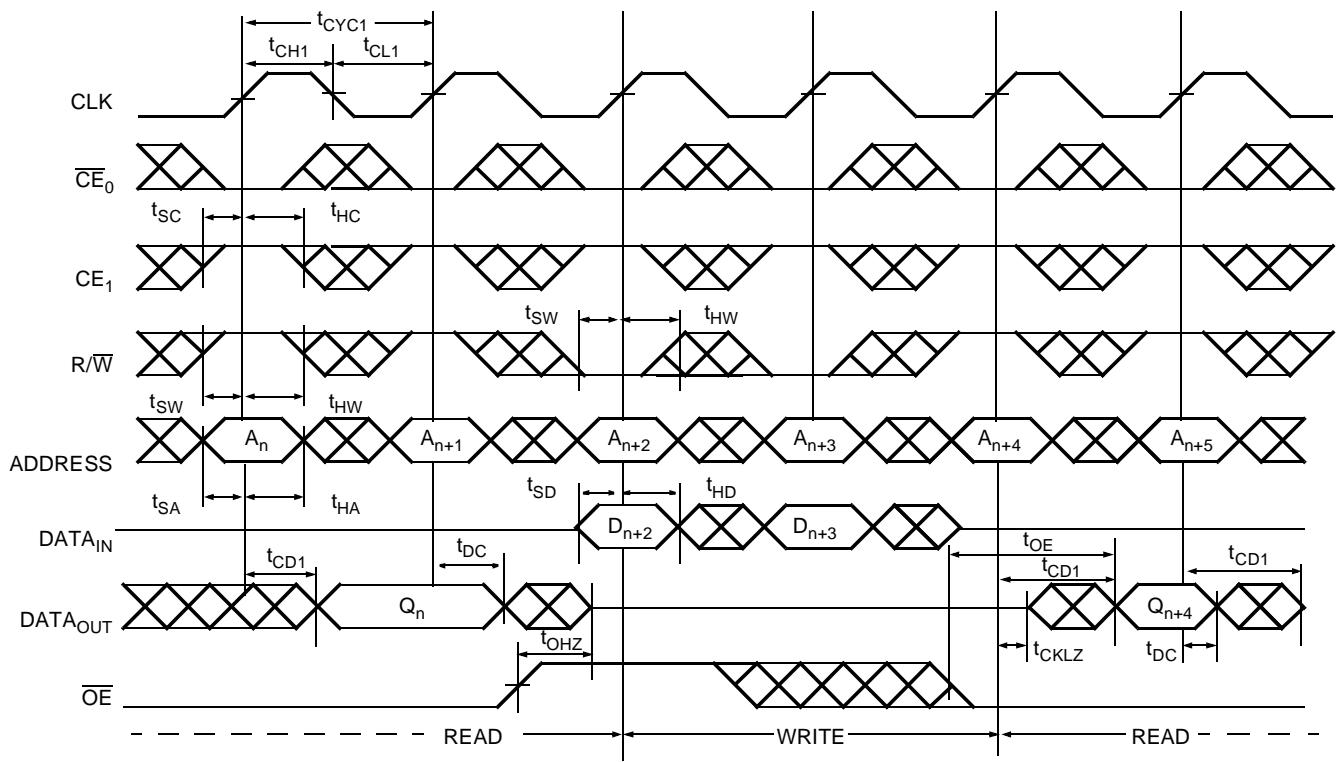
8. \overline{OE} is asynchronously controlled; all other inputs are synchronous to the rising clock edge.
9. $ADS = V_{IL}$, $CNTEN$ and $CNTRST = V_{IH}$.
10. The output is disabled (high-impedance state) by $\overline{CE}_0 = V_{IH}$ or $CE_1 = V_{IL}$ following the next rising edge of the clock.
11. Addresses do not have to be accessed sequentially since $ADS = V_{IL}$ constantly loads the address on the rising edge of the CLK. Numbers are for reference only.

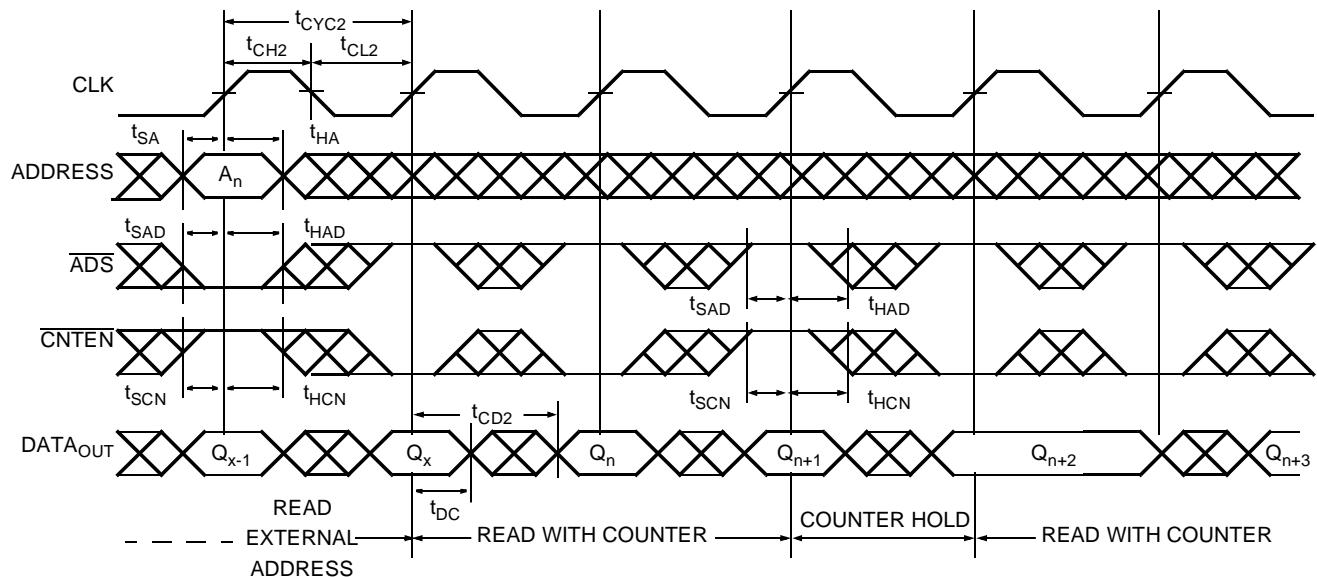
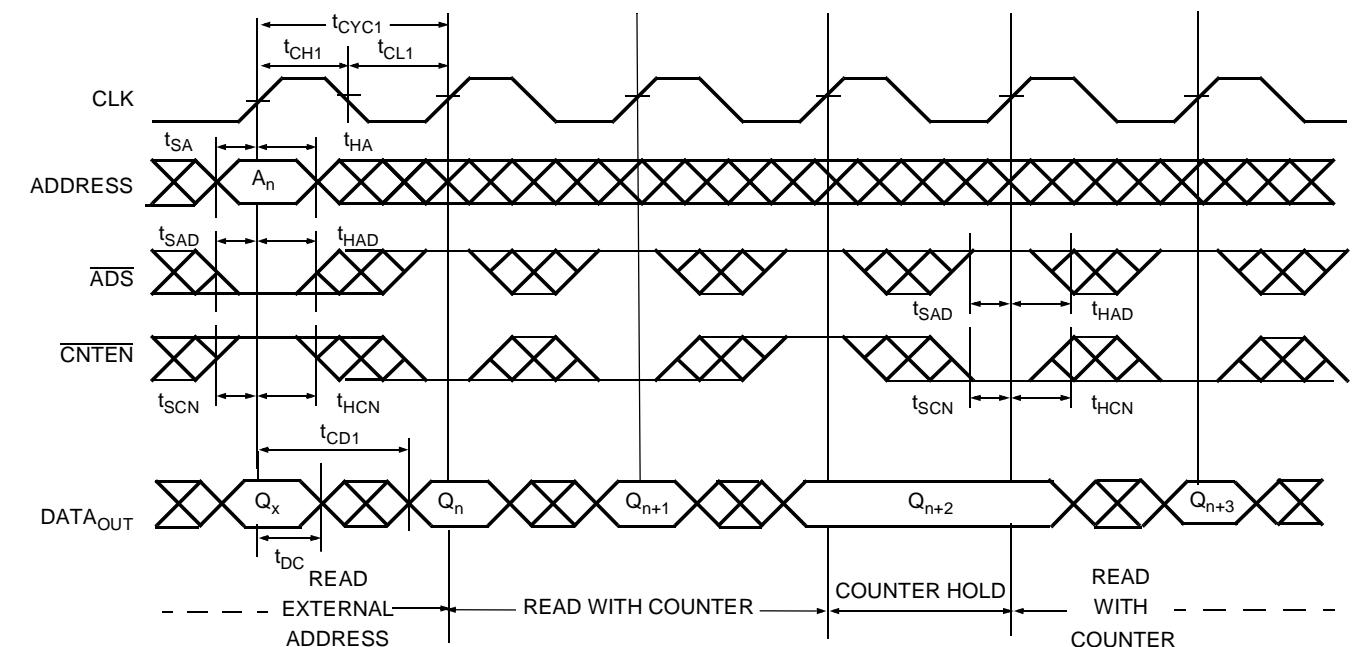
Switching Waveforms (continued)
Bank Select Pipelined Read^[12, 13]

Left Port Write to Flow-Through Right Port Read^[14, 15, 16, 17]

Notes:

12. In this depth expansion example, B1 represents Bank #1 and B2 is Bank #2; Each Bank consists of one Cypress dual-port device from this data sheet.
13. ADDRESS_(B1) = ADDRESS_(B2).
14. The same waveforms apply for a right port write to flow-through left port read.
15. CE₀, UB, LB, and ADS = V_{IL}; CE_{1(B1)}, CE_{1(B2)}, R/W, CNTEN, and CNTRST = V_{IH}.
16. OE = V_{IL} for the right port, which is being read from. OE = V_{IH} for the left port, which is being written to.
17. If t_{CCS} ≤ maximum specified, then data from right port READ is not valid until the maximum specified for t_{CWDD}. If t_{CCS}>maximum specified, then data is not valid until t_{CCS} + t_{CD1}. t_{CWDD} does not apply in this case.

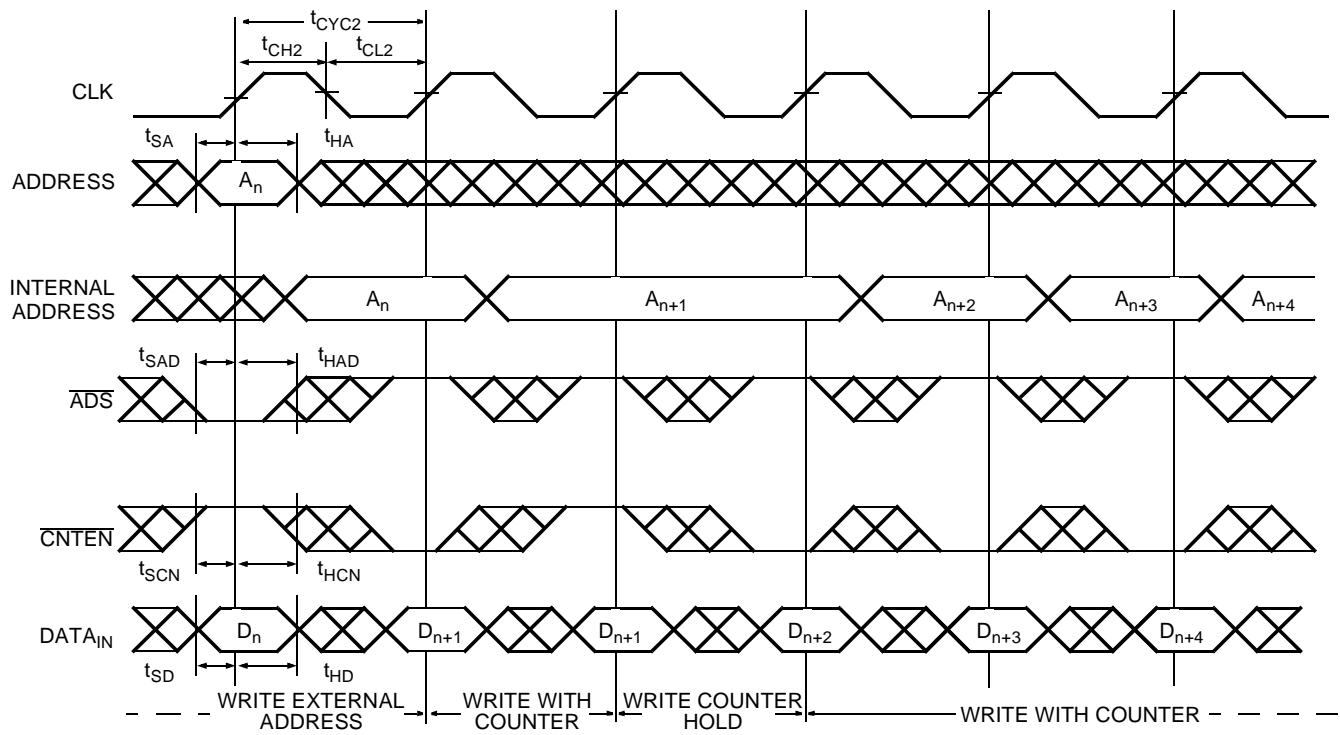
Switching Waveforms (continued)
Pipelined Read-to-Write-to-Read ($\overline{OE} = V_{IL}$)^[11, 18, 19, 20]

Pipelined Read-to-Write-to-Read (\overline{OE} Controlled)^[11, 18, 19, 20]

Notes:

18. Output state (HIGH, LOW, or High-Impedance) is determined by the previous cycle control signals.
19. \overline{CE}_0 and $\overline{ADS} = V_{IL}$; CE_1 , $CNTEN$, and $CNTRST = V_{IH}$.
20. During "No operation," data in memory at the selected address may be corrupted and should be rewritten to ensure data integrity.

Switching Waveforms (continued)
Flow-Through Read-to-Write-to-Read ($\overline{OE} = V_{IL}$)^[9, 11, 18, 19]

Flow-Through Read-to-Write-to-Read (\overline{OE} Controlled)^[9, 11, 18, 19]


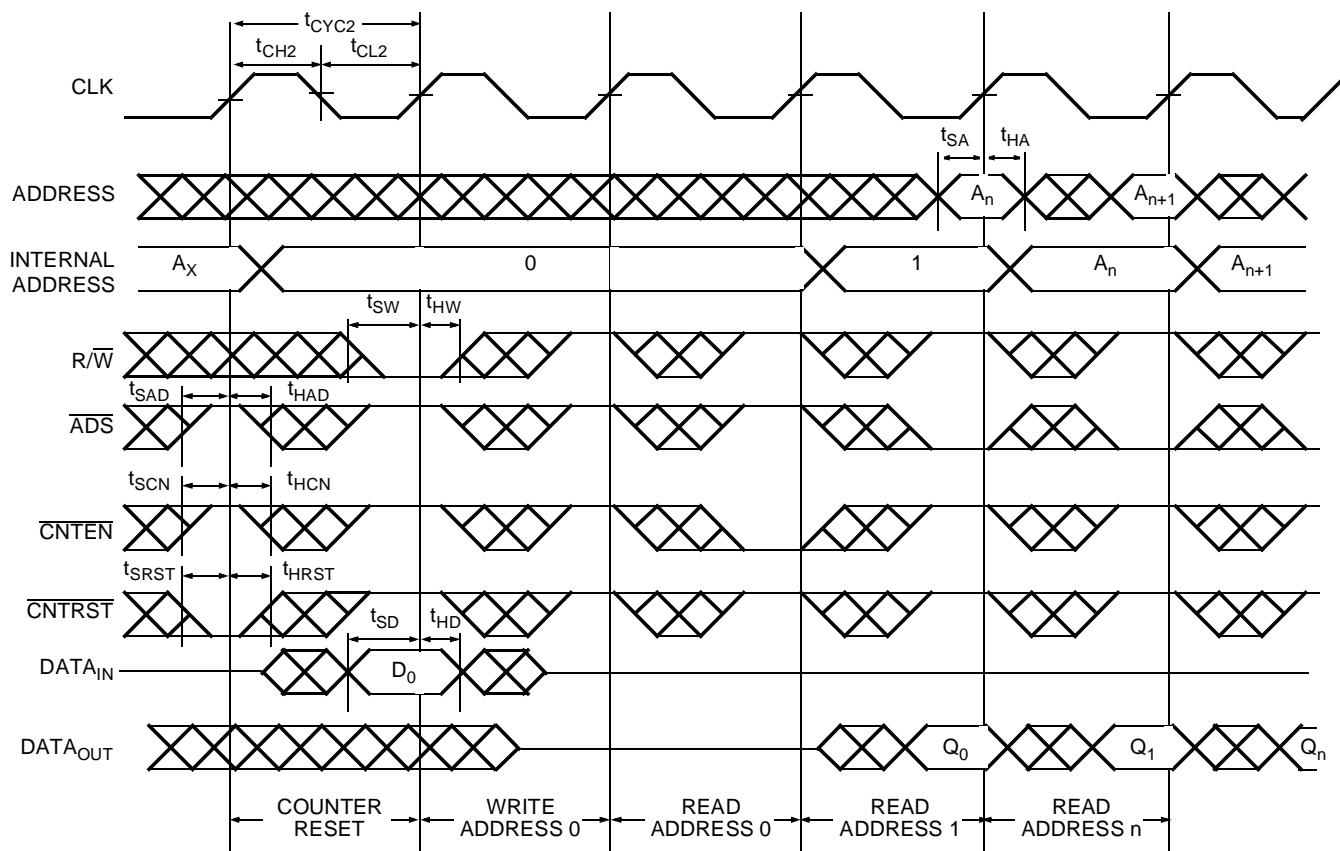
Switching Waveforms (continued)
Pipelined Read with Address Counter Advance^[21]

Flow-Through Read with Address Counter Advance^[21]

Note:

21. \overline{CE}_0 and $\overline{OE} = V_{IL}$; CE_1 , R/W and $\overline{CNTRST} = V_{IH}$.

Switching Waveforms (continued)
Write with Address Counter Advance (Flow-Through or Pipelined Outputs)^[22, 23]

Notes:

22. \overline{CE}_0 , \overline{UB} , \overline{LB} , and $R/\overline{W} = V_{IL}$; CE_1 and $\overline{CNTRST} = V_{IH}$.

23. The "Internal Address" is equal to the "External Address" when $\overline{ADS} = V_{IL}$ and equals the counter output when $\overline{ADS} = V_{IH}$.

Switching Waveforms (continued)
Counter Reset (Pipelined Outputs)^[11, 18, 24, 25]

Notes:

24. \overline{CE}_0 , \overline{UB} , and $\overline{LB} = V_{IL}$; $CE_1 = V_{IH}$.

25. No dead cycle exists during counter reset. A READ or WRITE cycle may be coincidental with the counter reset.

**PRELIMINARY****CY7C09349****CY7C09359****Read/Write and Enable Operation**^[26, 27, 28]

Inputs					Outputs	Operation
\overline{OE}	CLK	\overline{CE}_0	CE_1	R/W	$I/O_0-I/O_{17}$	
X	—	H	X	X	High-Z	Deselected ^[29]
X	—	X	L	X	High-Z	Deselected ^[29]
X	—	L	H	L	D_{IN}	Write
L	—	L	H	H	D_{OUT}	Read ^[29]
H	X	L	H	X	High-Z	Outputs Disabled

Address Counter Control Operation^[26,30,31,32]

Address	Previous Address	CLK	\overline{ADS}	$CNTEN$	$CNTRST$	I/O	Mode	Operation
X	X	—	X	X	L	$D_{out(0)}$	Reset	Counter Reset to Address 0
A_n	X	—	L	X	H	$D_{out(n)}$	Load	Address Load into Counter
X	A_n	—	H	H	H	$D_{out(n)}$	Hold	External Address Blocked—Counter Disabled
X	A_n	—	H	L	H	$D_{out(n+1)}$	Increment	Counter Enabled—Internal Address Generation

Notes:

26. "X" = "don't care," "H" = V_{IH} , "L" = V_{IL} .
27. \overline{ADS} , $CNTEN$, $CNTRST$ = "don't care."
28. \overline{OE} is an asynchronous input signal.
29. When CE changes state in the pipelined mode, deselection and read happen in the following clock cycle.
30. CE_0 and $OE = V_{IL}$; CE_1 and $R/W = V_{IH}$.
31. Data shown for flow-through mode; pipelined mode output will be delayed by one cycle.
32. Counter operation is independent of CE_0 and CE_1 .



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Ordering Information

4K x18 Synchronous Dual-Port SRAM

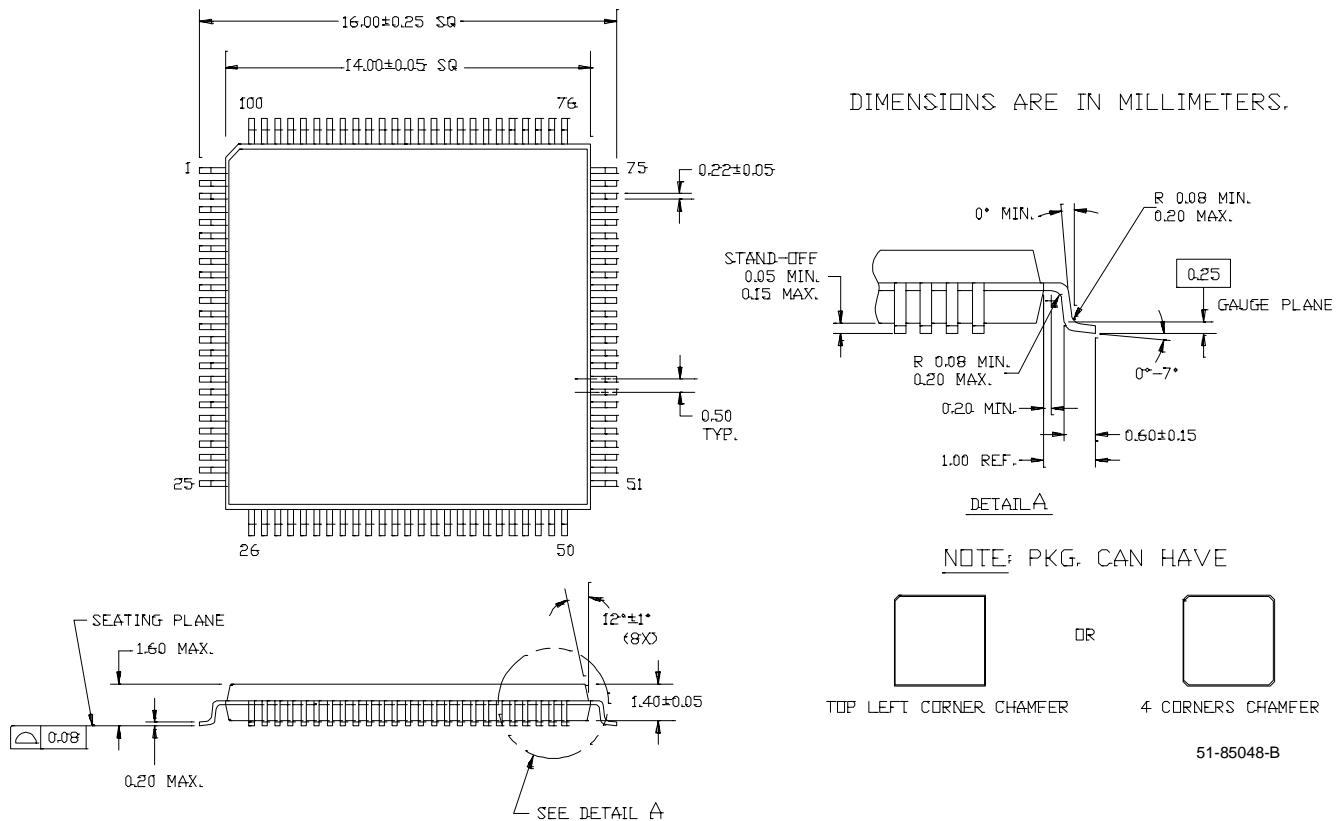
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
6.5 ^[1]	CY7C09349-6AC	A100	100-Pin Thin Quad Flat Pack	Commercial
7.5	CY7C09349-7AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C09349-7AI	A100	100-Pin Thin Quad Flat Pack	Industrial
9	CY7C09349-9AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C09349-9AI	A100	100-Pin Thin Quad Flat Pack	Industrial
12	CY7C09349-12AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C09349-12AI	A100	100-Pin Thin Quad Flat Pack	Industrial

8K x18 Synchronous Dual-Port SRAM

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
6.5 ^[1]	CY7C09359-6AC	A100	100-Pin Thin Quad Flat Pack	Commercial
7.5	CY7C09359-7AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C09359-7AI	A100	100-Pin Thin Quad Flat Pack	Industrial
9	CY7C09359-9AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C09359-9AI	A100	100-Pin Thin Quad Flat Pack	Industrial
12	CY7C09359-12AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C09359-12AI	A100	100-Pin Thin Quad Flat Pack	Industrial

Shaded areas contain advance information.

Document #: 38-00672-C

Package Diagram
100-Pin Thin Plastic Quad Flat Pack (TQFP) A100




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CY7C09359

CY7C036 Dual Port Design Consideration – Data Sheet Addendum

This design consideration applies to the Internal Power-On-Reset (POR) circuit used on the CY7C036 and its derivatives listed below.

Power supply ramp—The devices will function properly and meet all data sheet specifications if the power supply ramp rate is greater than 100 ns. If ramp is less than 100 ns, you may see a non-destructive failure in which the device will not respond to changes in address or clock, but the I/Os will respond to the output enable.

Applications consideration—If the power supply ramps in less than 100 ns, a small resistor (20–50 Ω), a large capacitor, or an RC network can be connected at the output of the power supply to ground. The addition of a resistor will help clean up the power lines, while the capacitor will slow down the ramp rate

without the loss of any power. Contact your local Cypress FAE for assistance as needed.

Troubleshooting—If a problem occurs with the part, power down the device to ground and then power up again at slower ramp rate (greater than 100 ns) in order to confirm that the problem might be due to the POR circuit. If the dual-port functions properly once the ramp rate is slowed to 100 ns or greater, then the POR circuit is at fault.

Applicable devices—All speed/package/temperature combinations of the following:

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Cypress design change—Cypress design team has identified the root cause. A permanent circuit change and die revision will be available beginning in October and will be identified by the letter “A” in the part number.