



# CY7C128A

## 2K x 8 Static RAM

### Features

- Automatic power-down when deselected
- CMOS for optimum speed/power
- High speed
  - 15 ns
- Low active power
  - 660 mW (commercial)
  - 688 mW (military—20 ns)
- Low standby power
  - 110 mW (20 ns)
- TTL-compatible inputs and outputs
- Capable of withstanding greater than 2001V electrostatic discharge
- $V_{IH}$  of 2.2V

### Functional Description

The CY7C128A is a high-performance CMOS static RAM organized as 2048 words by 8 bits. Easy memory expansion is

provided by an active LOW Chip Enable ( $\overline{CE}$ ), and active LOW Output Enable ( $\overline{OE}$ ) and three-state drivers. The CY7C128A has an automatic power-down feature, reducing the power consumption by 83% when deselected.

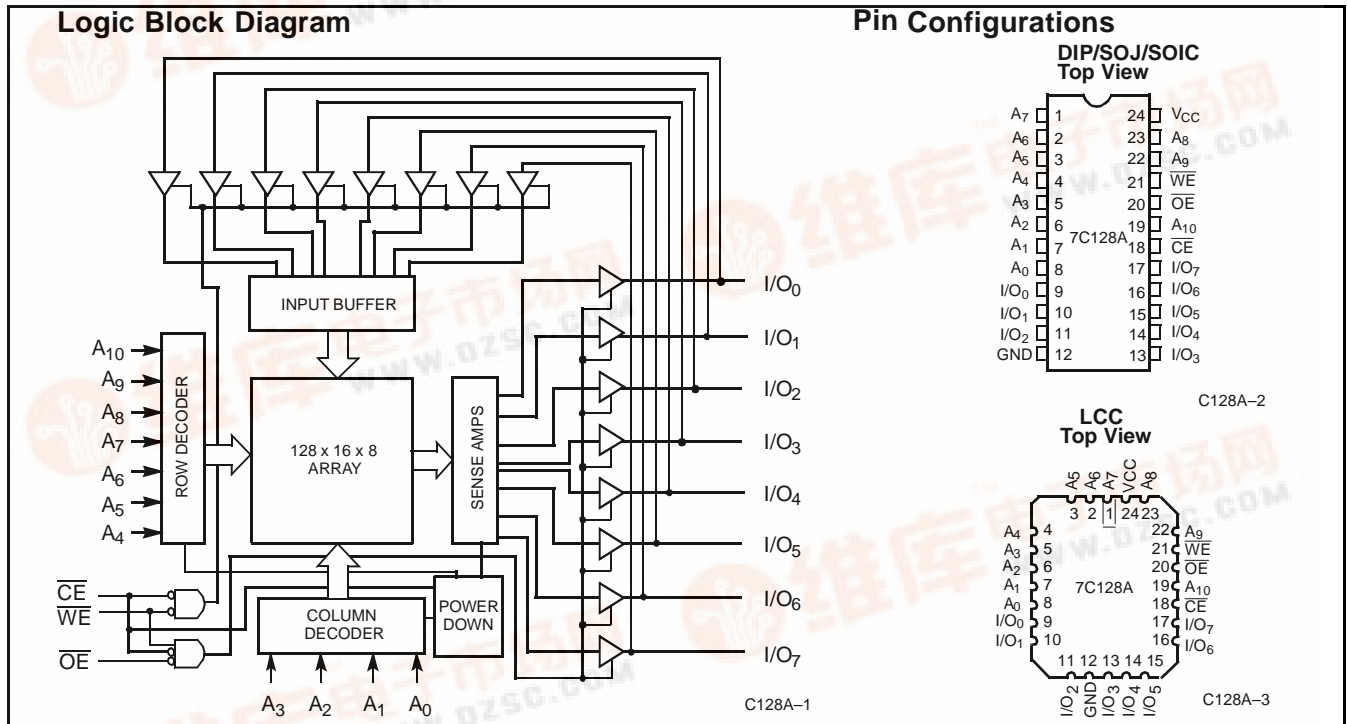
Writing to the device is accomplished when the Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs are both LOW.

Data on the eight I/O pins (I/O<sub>0</sub> through I/O<sub>7</sub>) is written into the memory location specified on the address pins (A<sub>0</sub> through A<sub>10</sub>).

Reading the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while Write Enable ( $\overline{WE}$ ) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the eight I/O pins.

The I/O pins remain in high-impedance state when Chip Enable ( $\overline{CE}$ ) or Output Enable ( $\overline{OE}$ ) is HIGH or Write Enable ( $\overline{WE}$ ) is LOW.

The CY7C128A utilizes a die coat to insure alpha immunity.



### Selection Guide

		7C128A-15	7C128A-20	7C128A-25	7C128A-35	7C128A-45
Maximum Access Time (ns)		15	20	25	35	45
Maximum Operating Current (mA)	Commercial	120	120	120	120	120
	Military	-	125	125	125	125
Maximum Standby Current (mA)	Commercial	40	20	20	20	20
	Military	-	20	20	20	20





**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with Power Applied ..... -55°C to +125°C

Supply Voltage to Ground Potential (Pin 28 to Pin 14) ..... -0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... -0.5V to +7.0V

DC Input Voltage ..... -3.0V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

**Operating Range**

Range	Ambient Temperature	V <sub>CC</sub>
Commercial	0°C to +70°C	5V ± 10%
Military <sup>[1]</sup>	-55°C to +125°C	5V ± 10%

**Electrical Characteristics** Over the Operating Range<sup>[2]</sup>

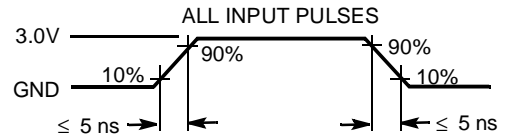
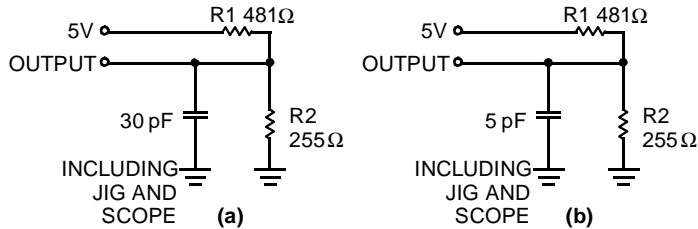
Parameter	Description	Test Conditions	7C128A-15		7C128A-20		7C128A-25		7C128A-35,45		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA	2.4		2.4		2.4		2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA		0.4		0.4		0.4		0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>CC</sub>	2.2	V <sub>CC</sub>	2.2	V <sub>CC</sub>	2.2	V <sub>CC</sub>	V
V <sub>IL</sub>	Input LOW Voltage <sup>[3]</sup>		-0.5	0.8	-0.5	0.8	-0.5	0.8	-0.5	0.8	V
I <sub>Ix</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-10	+10	-10	+10	-10	+10	-10	+10	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub> Output Disabled	-10	+10	-10	+10	-10	+10	-10	+10	μA
I <sub>OS</sub>	Output Short Circuit Current <sup>[4]</sup>	V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND		-300		-300		-300		-300	mA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max. I <sub>OUT</sub> = 0 mA	Com'l	120		120		120		120	mA
			Mil	-		125		125		125	
I <sub>SB1</sub>	Automatic $\overline{CE}$ Power-Down Current	Max. V <sub>CC</sub> , $\overline{CE} \geq V_{IH}$ , Min. Duty Cycle = 100%	Com'l	40		40		20		20	mA
			Mil	-		40		40		20	
I <sub>SB2</sub>	Automatic $\overline{CE}$ Power-Down Current	Max. V <sub>CC</sub> , $\overline{CE}_1 \geq V_{CC} - 0.3V$ , $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$	Com'l	40		20		20		20	mA
			Mil	-		20		20		20	

**Capacitance<sup>[5]</sup>**

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 5.0V	10	pF
C <sub>OUT</sub>	Output Capacitance		10	pF

**Notes:**

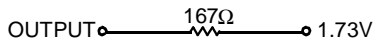
- T<sub>A</sub> is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.
- V<sub>IL</sub> (min.) = -3.0V for pulse durations less than 30 ns.
- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- Tested initially and after any design or process changes that may affect these parameters.

**AC Test Loads and Waveforms**


C128A-4

C128A-5

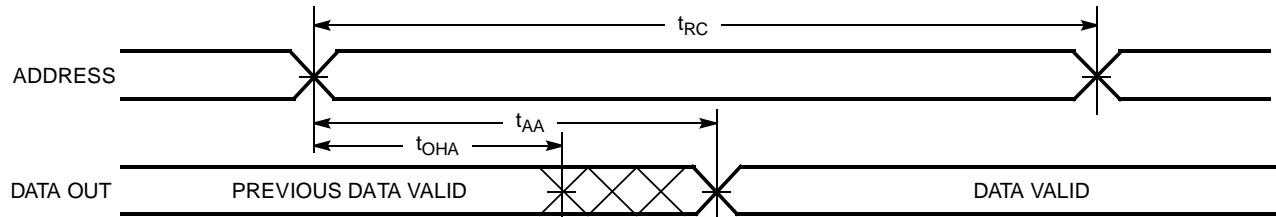
Equivalent to: THÉVENIN EQUIVALENT


**Switching Characteristics** Over the Operating Range<sup>[2, 6]</sup>

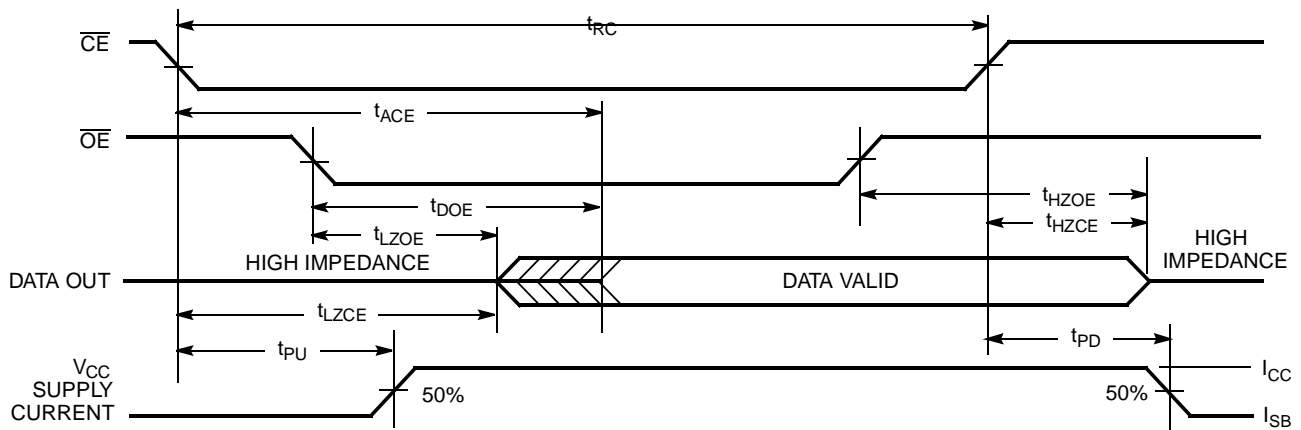
Parameter	Description	7C128A-15		7C128A-20		7C128A-25		7C128A-35		7C128A-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>												
$t_{RC}$	Read Cycle Time	15		20		25		35		45		ns
$t_{AA}$	Address to Data Valid		15		20		25		35		45	ns
$t_{OHA}$	Data Hold from Address Change	5		5		5		5		5		ns
$t_{ACE}$	$\overline{CE}$ LOW to Data Valid		15		20		25		35		45	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid		10		10		12		15		20	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low Z	3		3		3		3		3		ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High Z <sup>[7]</sup>		8		8		10		12		15	ns
$t_{LZCE}$	$\overline{CE}$ LOW to Low Z <sup>[8]</sup>	5		5		5		5		5		ns
$t_{HZCE}$	$\overline{CE}$ HIGH to High Z <sup>[7, 8]</sup>		8		8		10		15		15	ns
$t_{PU}$	$\overline{CE}$ LOW to Power-Up	0		0		0		0		0		ns
$t_{PD}$	$\overline{CE}$ HIGH to Power-Down		15		20		20		20		25	ns
<b>WRITE CYCLE<sup>[9]</sup></b>												
$t_{WC}$	Write Cycle Time	15		20		20		25		40		ns
$t_{SCE}$	$\overline{CE}$ LOW to Write End	12		15		20		25		30		ns
$t_{AW}$	Address Set-Up to Write End	12		15		20		25		30		ns
$t_{HA}$	Address Hold from Write End	0		0		0		0		0		ns
$t_{SA}$	Address Set-Up to Write Start	0		0		0		0		0		ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	12		15		15		20		20		ns
$t_{SD}$	Data Set-Up to Write End	10		10		10		15		15		ns
$t_{HD}$	Data Hold from Write End	0		0		0		0		0		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High Z <sup>[7]</sup>		7		7		7		10		15	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low Z	5		5		5		5		5		ns

**Notes:**

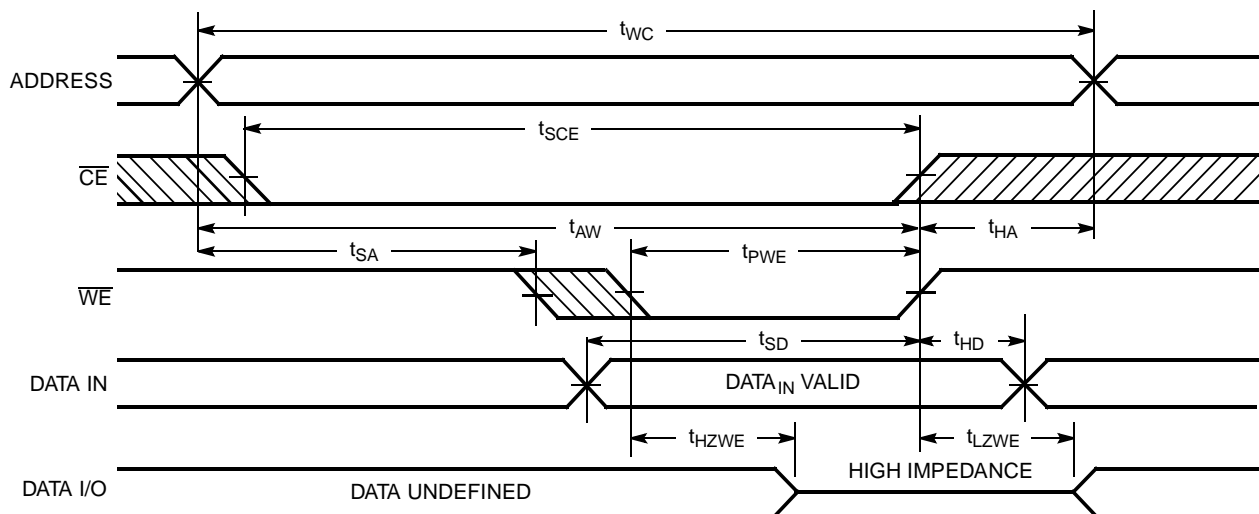
- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified  $I_{OL}/I_{OH}$  and 30-pF load capacitance.
- $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with  $C_L = 5$  pF as in part (b) of AC Test Loads. Transition is measured  $\pm 500$  mV from steady state voltage.
- At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$  for any given device.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

**Switching Waveforms**
**Read Cycle No. 1<sup>[10, 11]</sup>**


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**Read Cycle No. 2<sup>[10, 12]</sup>**


C128A-7

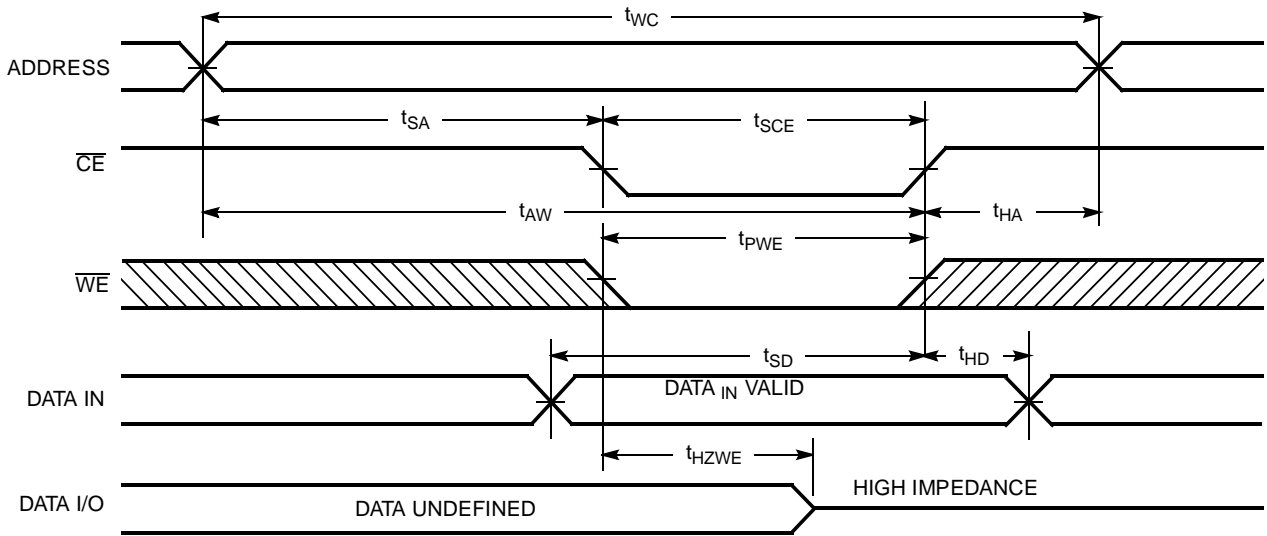
**Write Cycle No. 1 ( $\overline{WE}$  Controlled)<sup>[9, ]</sup>**


C128A-8

**Notes:**

10.  $\overline{WE}$  is HIGH for read cycle.
11. Device is continuously selected.  $\overline{OE}, \overline{CE} = V_{IL}$ .
12. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.
13. Data I/O pins enter high-impedance state, as shown, when  $\overline{OE}$  is held LOW during write.

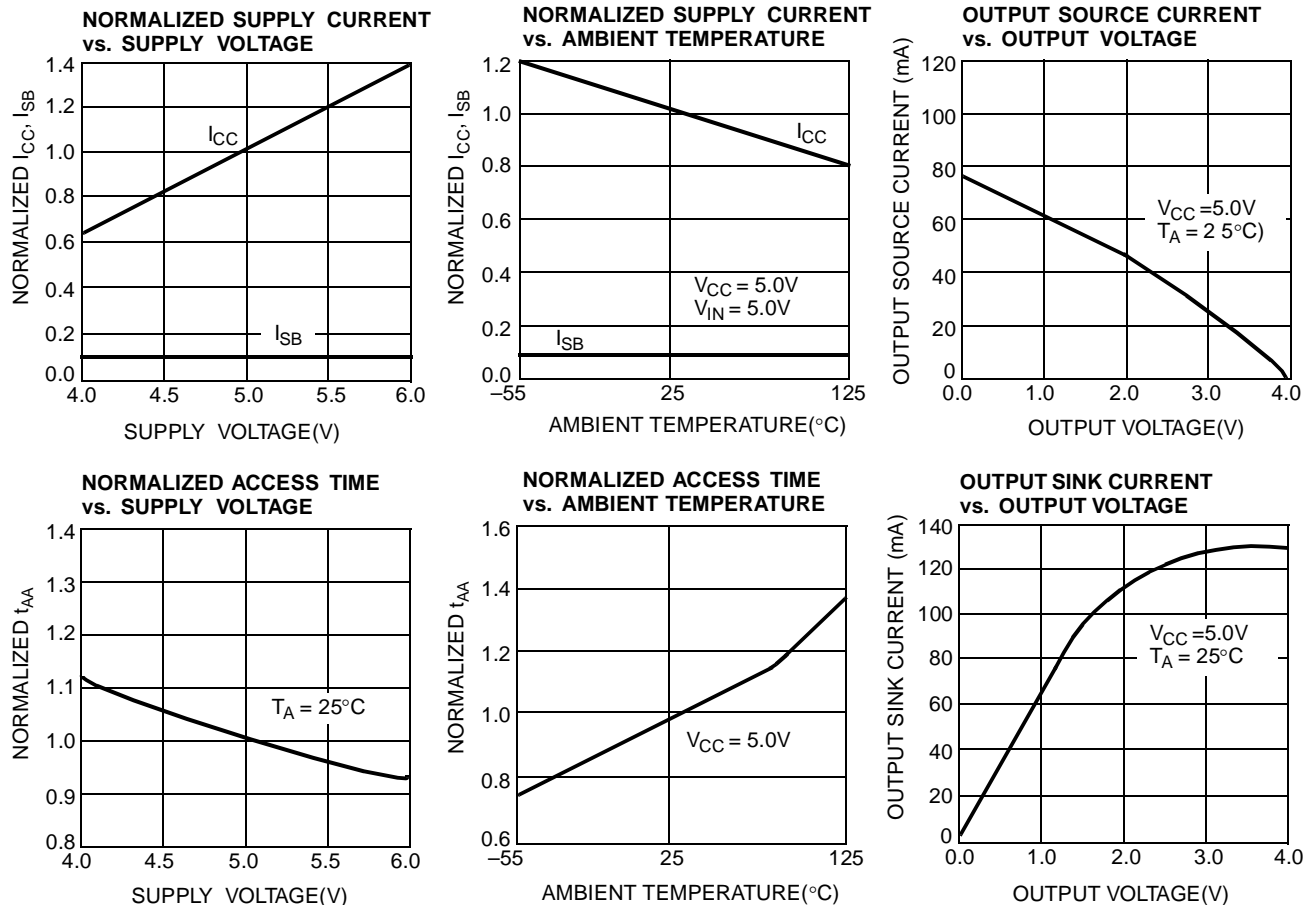
**Switching Waveforms** (continued)

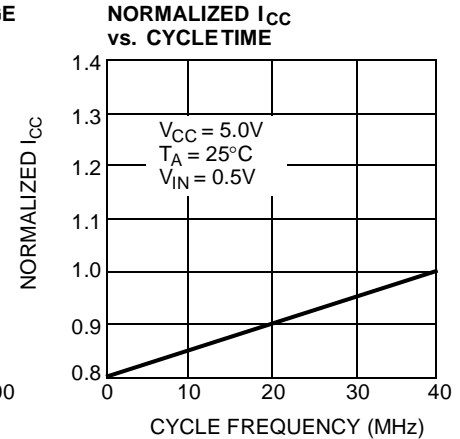
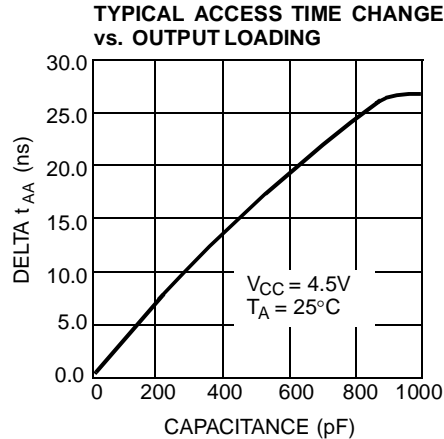
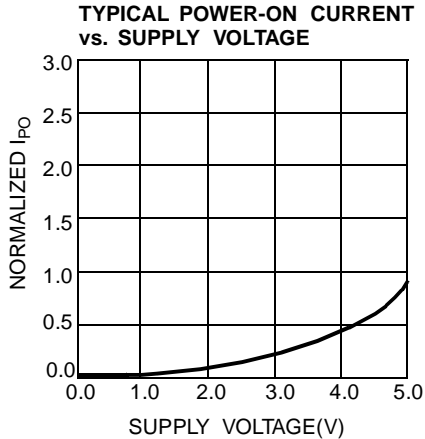
**Write Cycle No. 2 ( $\overline{CE}$  Controlled)**<sup>[9, 13, 14]</sup>


C128A-9

**Notes:**

 14. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high-impedance state.

**Typical DC and AC Characteristics**


**Typical DC and AC Characteristics (continued)**

**Ordering Information**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C128A-15PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C128A-15VC	V13	24-Lead Molded SOJ	
	CY7C128A-15SC	S13	24-Lead (300-Mil) Molded SOIC	
20	CY7C128A-20PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C128A-20VC	V13	24-Lead Molded SOJ	
	CY7C128A-20SC	S13	24-Lead (300-Mil) Molded SOIC	
	CY7C128A-20DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C128A-20LMB	L53	24-Pin Rectangular Leadless Chip Carrier	
25	CY7C128A-25PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C128A-25VC	V13	24-Lead Molded SOJ	
	CY7C128A-25SC	S13	24-Lead (300-Mil) Molded SOIC	
	CY7C128A-25DMB	D14	24-Lead (300-Mil) CerDIP	Military
35	CY7C128A-35PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C128A-35VC	V13	24-Lead Molded SOJ	
	CY7C128A-35SC	S13	24-Lead (300-Mil) Molded SOIC	
	CY7C128A-35DMB	D14	24-Lead (300-Mil) CerDIP	Military
45	CY7C128A-45PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C128A-45VC	V13	24-Lead Molded SOJ	
	CY7C128A-45SC	S13	24-Lead (300-Mil) Molded SOIC	
	CY7C128A-45DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C128A-45LMB	L53	24-Pin Rectangular Leadless Chip Carrier	



**MILITARY SPECIFICATIONS**

**Group A Subgroup Testing**

**DC Characteristics**

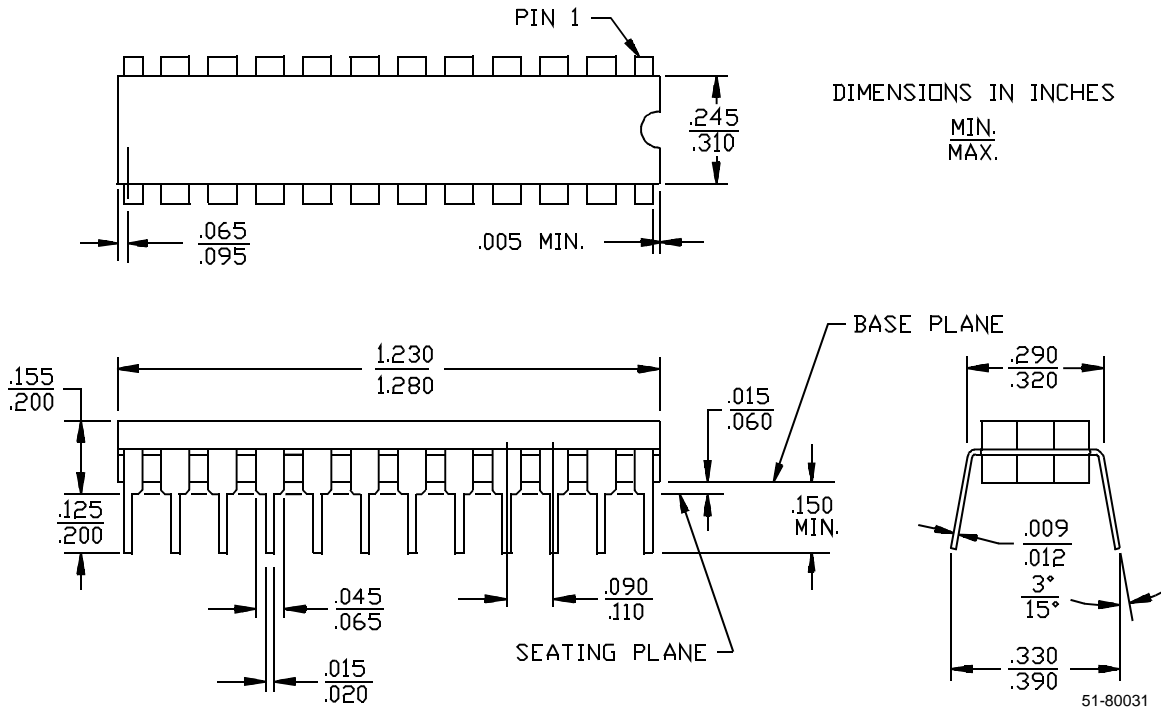
Parameter	Subgroups
V <sub>OH</sub>	1, 2, 3
V <sub>OL</sub>	1, 2, 3
V <sub>IH</sub>	1, 2, 3
V <sub>IL</sub> Max.	1, 2, 3
I <sub>Ix</sub>	1, 2, 3
I <sub>OZ</sub>	1, 2, 3
I <sub>CC</sub>	1, 2, 3
I <sub>SB</sub>	1, 2, 3

**Switching Characteristics**

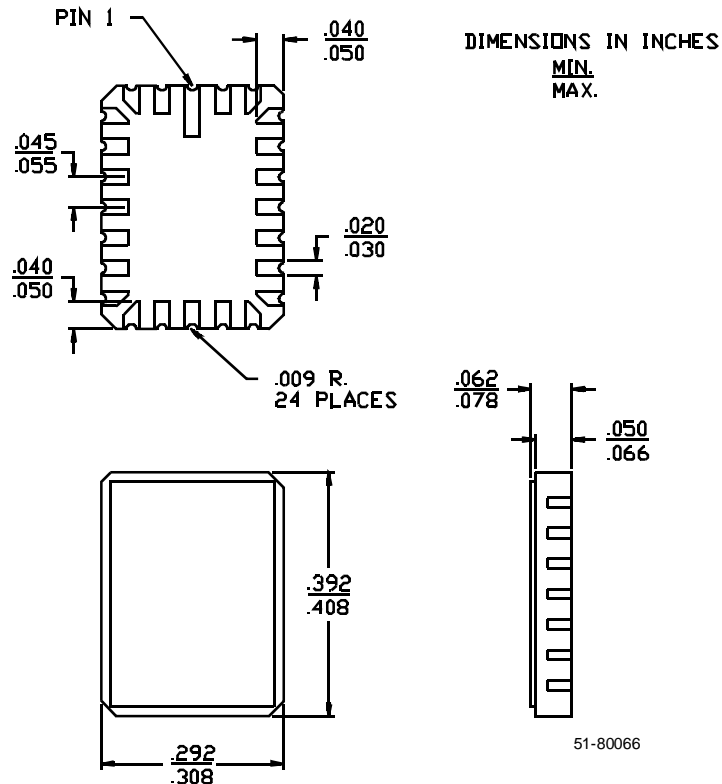
Parameter	Subgroups
<b>READ CYCLE</b>	
t <sub>RC</sub>	7, 8, 9, 10, 11
t <sub>AA</sub>	7, 8, 9, 10, 11
t <sub>OHA</sub>	7, 8, 9, 10, 11
t <sub>ACE</sub>	7, 8, 9, 10, 11
t <sub>DOE</sub>	7, 8, 9, 10, 11
<b>WRITE CYCLE</b>	
t <sub>WC</sub>	7, 8, 9, 10, 11
t <sub>SCE</sub>	7, 8, 9, 10, 11
t <sub>AW</sub>	7, 8, 9, 10, 11
t <sub>HA</sub>	7, 8, 9, 10, 11
t <sub>SA</sub>	7, 8, 9, 10, 11
t <sub>PWE</sub>	7, 8, 9, 10, 11
t <sub>SD</sub>	7, 8, 9, 10, 11
t <sub>HD</sub>	7, 8, 9, 10, 11

Package Diagrams

**24-Lead (300-Mil) CerDIP D14**  
MIL-STD-1835 D-9 Config.A

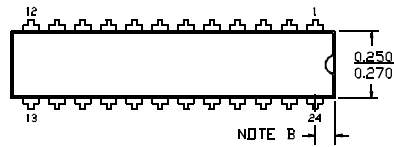


**24-Pin Rectangular Leadless Chip Carrier L53**

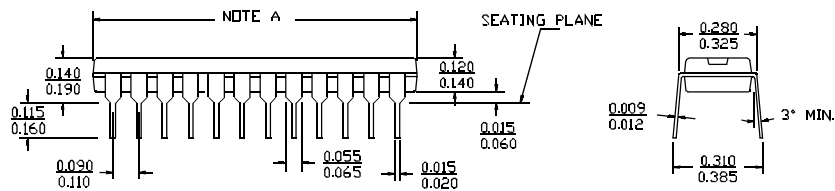




**Package Diagrams (continued)**
**24-Lead (300-Mil) Molded DIP P13/P13A**

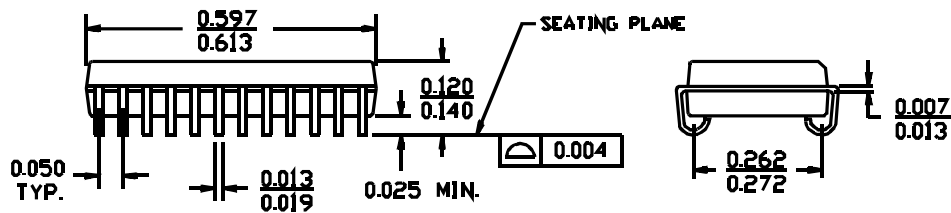
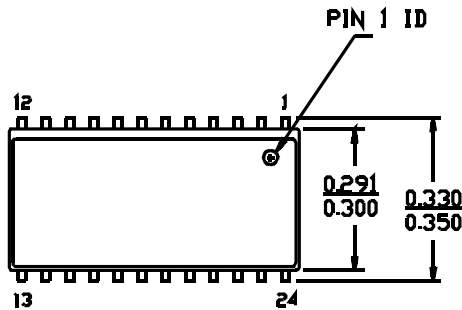
 DIMENSIONS IN INCHES MIN.  
MAX.


	P 13	P 13A
NOTE A	1.170 1.200	1.230 1.260
NOTE B	0.030 0.050	0.060 0.080



51-85013-A

**24-Lead (300-Mil) Molded SOJ V13**

 DIMENSIONS IN INCHES MIN.  
MAX.


51-85030-A