CY7C150

1Kx4 Static RAM

Features

- **Memory reset function**
- **1024 x 4 static RAM for control store in high-speed computers**
- **CMOS for optimum speed/power**
- **High speed**
  - **— 10 ns (commercial)**
  - **— 12 ns (military)**
- **Low power**
  - **— 495 mW (commercial)**
  - **— 550 mW (military)**
- **Separate inputs and outputs**
- **5-volt power supply ±10% tolerance in both commercial and military**
- **Capable of withstanding greater than 2001V static discharge**
- **TTL-compatible inputs and outputs**

Functional Description

The CY7C150 is a high-performance CMOS static RAM designed for use in cache memory, high-speed graphics, and data-acquisition applications. The CY7C150 has a memory reset feature that allows the entire memory to be reset in two memory cycles.

Separate I/O paths eliminates the need to multiplex data in and data out, providing for simpler board layout and faster system performance. Outputs are three-stated during write, reset, deselect, or when output enable ($\overline{OE}$) is held HIGH, allowing for easy memory expansion.

Reset is initiated by selecting the device ($\overline{CS}$ = LOW) and taking the reset ($\overline{RS}$) input LOW. Within two memory cycles all bits are internally cleared to zero. Since chip select must be LOW for the device to be reset, a global reset signal can be employed, with only selected devices being cleared at any given time.

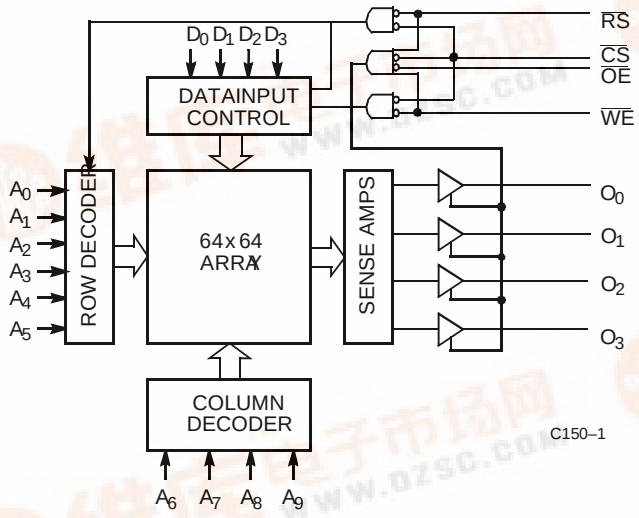
Writing to the device is accomplished when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the four data inputs (D_0–D_3) is written into the memory location specified on the address pins (A_0 through A_9).

Reading the device is accomplished by taking chip select ($\overline{CS}$) and output enable ($\overline{OE}$) LOW while write enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the four output pins (O_0 through O_3).

The output pins remain in high-impedance state when chip enable ($\overline{CE}$) or output enable ($\overline{OE}$) is HIGH, or write enable ($\overline{WE}$) or reset ($\overline{RS}$) is LOW.

A die coat is used to insure alpha immunity.

Logic Block Diagram



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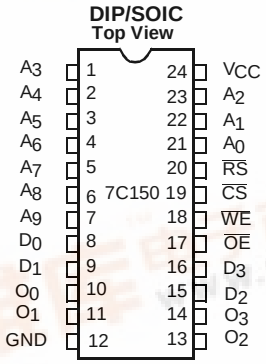
Pin Configuration



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Selection Guide

		7C150–10	7C150–12	7C150–15	7C150–25	7C150–35
Maximum Access Time (ns)	Commercial	10	12	15	25	
	Military		12	15	25	35
Maximum Operating Current (mA)	Commercial	90	90	90	90	90
	Military		100	100	100	100

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied..... –55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12)..... –0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State..... –0.5V to +7.0V

DC Input Voltage ..... –3.0V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military[1]	–55°C to +125°C	5V ± 10%

Note:
1. T_A is the "instant on" case temperature.

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions		7C150 Min.	7C150 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 0.4 mA		2.4		V
V_{OL}	Output LOW Current	V_{CC} = Min., I_{OL} = 12 mA			0.4	V
V_{IH}	Input HIGH Level			2.0	V_{CC}	V
V_{IL}	Input LOW Level			–3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		–10	+10	µA
I_{OZ}	Output Current (High Z)	V_{OL} ≤ V_{OUT} ≤ V_{OH}, Output Disabled		–50	+50	µA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND			–300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Commercial		90	mA
			Military		100	mA

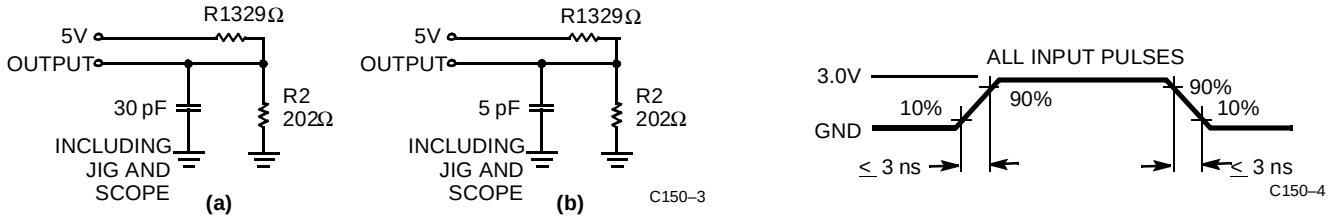
Notes:
2. See the last page of this specification for Group A subgroup testing information.
3. Not more than 1 output should be shorted at a time. Duration of the short circuit should not exceed 30 seconds.

Capacitance[4]

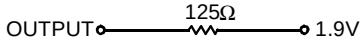
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

Note:
4. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[2,5]

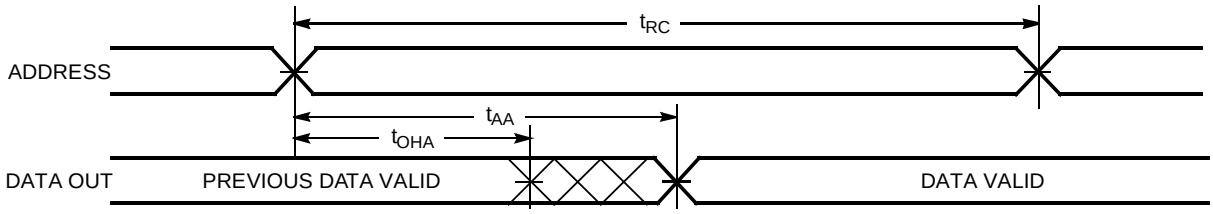
Parameter	Description	7C150–10		7C150–12		7C150–15		7C150–25		7C150–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	10		12		15		25		35		ns
t_{AA}	Address to Data Valid		10		12		15		25		35	ns
t_{OHA}	Output Hold from Address Change	2		2		2		2		2		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		8		10		12		15		20	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[6]	0		0		0		0		0		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[6,7]		6		8		11		20		25	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		6		8		10		15		20	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[6]	0		0		0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[6,7]		6		8		9		20		25	ns
WRITE CYCLE[8]												
t_{WC}	Write Cycle Time	10		12		15		25		35		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	6		8		11		15		20		ns
t_{AW}	Address Set-Up to Write End	8		10		13		20		30		ns
t_{HA}	Address Hold from Write End	2		2		2		5		5		ns
t_{SA}	Address Set-Up to Write Start	2		2		2		5		5		ns
t_{PWE}	$\overline{WE}$ Pulse Width	6		8		11		15		20		ns
t_{SD}	Data Set-Up to Write End	6		8		11		15		20		ns
t_{HD}	Data Hold from Write End	2		2		2		5		5		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[6]	0		0		0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6,7]		6		8		12		20		25	ns
RESET CYCLE												
t_{RRC}	Reset Cycle Time	20		24		30		50		70		ns
t_{SAR}	Address Valid to Beginning of Reset	0		0		0		0		0		ns
t_{SWER}	Write Enable HIGH to Beginning of Reset	0		0		0		0		0		ns
t_{SCSR}	Chip Select LOW to Beginning of Reset	0		0		0		0		0		ns
t_{PRS}	Reset Pulse Width	10		12		15		20		30		ns
t_{HCSR}	Chip Select Hold After End of Reset	0		0		0		0		0		ns
t_{HWER}	Write Enable Hold After End of Reset	8		12		15		30		40		ns
t_{HAR}	Address Hold After End of Reset	10		12		15		30		40		ns
t_{LZRS}	Reset HIGH to Output in Low Z[6]	0		0		0		0		0		ns
t_{HZRS}	Reset LOW to Output in High Z[6,7]		6		8		12		20		25	ns

Notes:

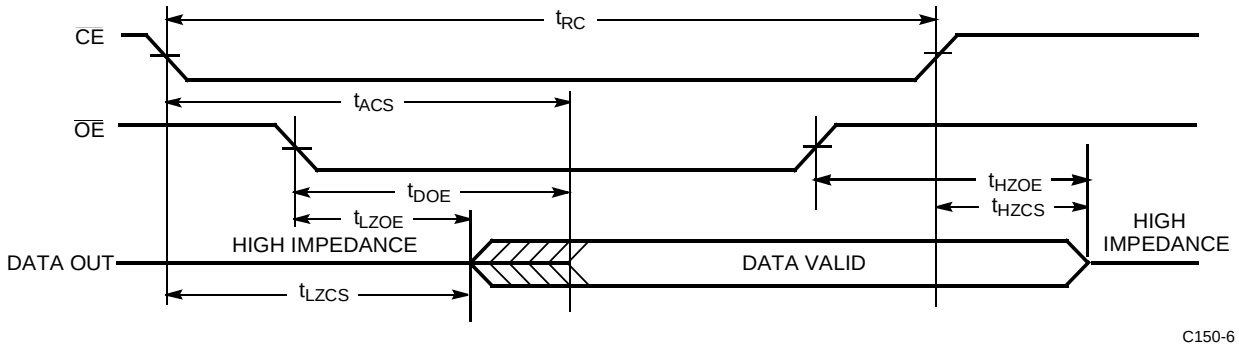
5. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
6. At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for any given device.
7. t_{HZCS}, t_{HZOE}, t_{HZR}, and t_{HZWE} are tested with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
8. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be reference to the rising edge of the signal that terminates the write.

Switching Waveforms

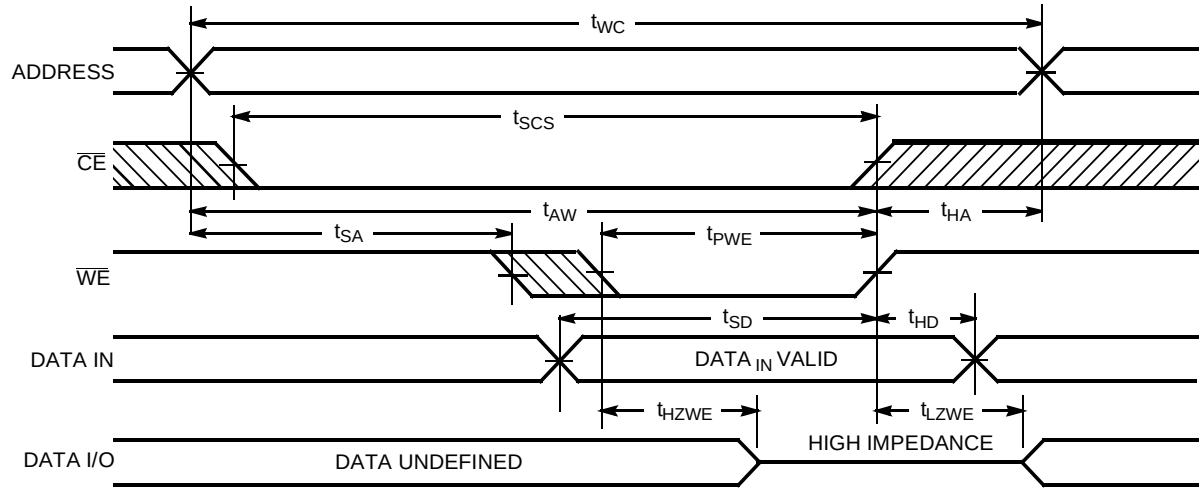
Read Cycle No.1 [9,10]



Read Cycle No. 2 [9,11]



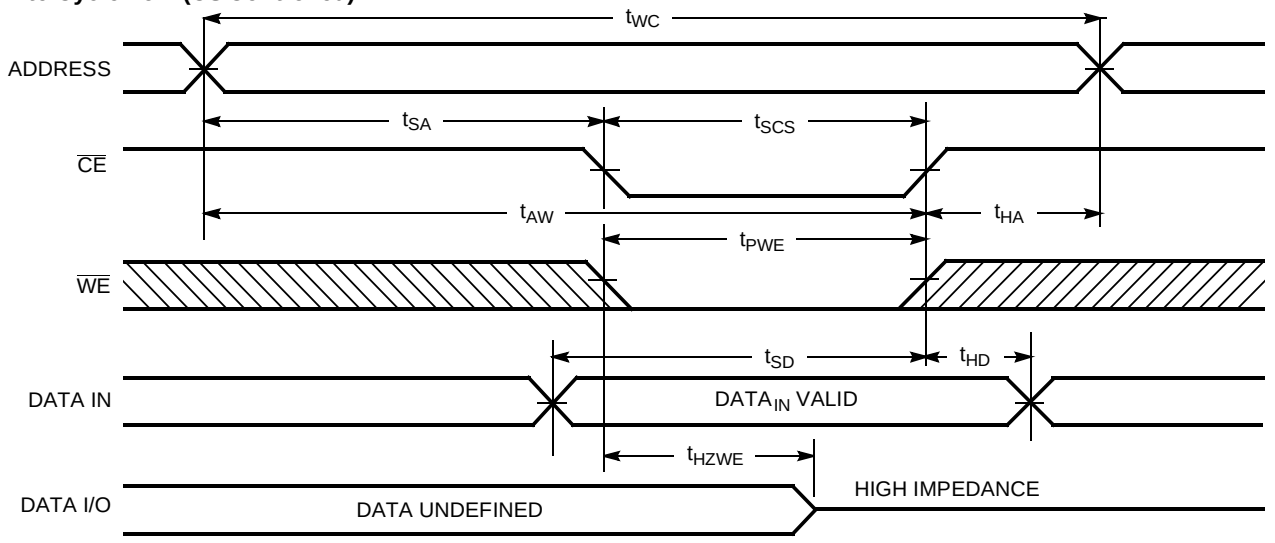
Write Cycle No.1 (WE Controlled) [8]



Notes:
9. WE is HIGH for read cycle.
10. Device is continuously selected, CS and OE = V_{IL}.
11. Address prior to or coincident with CS transition LOW.

Switching Waveforms (continued)

Write Cycle No2 ($\overline{CS}$ Controlled) [8,12]



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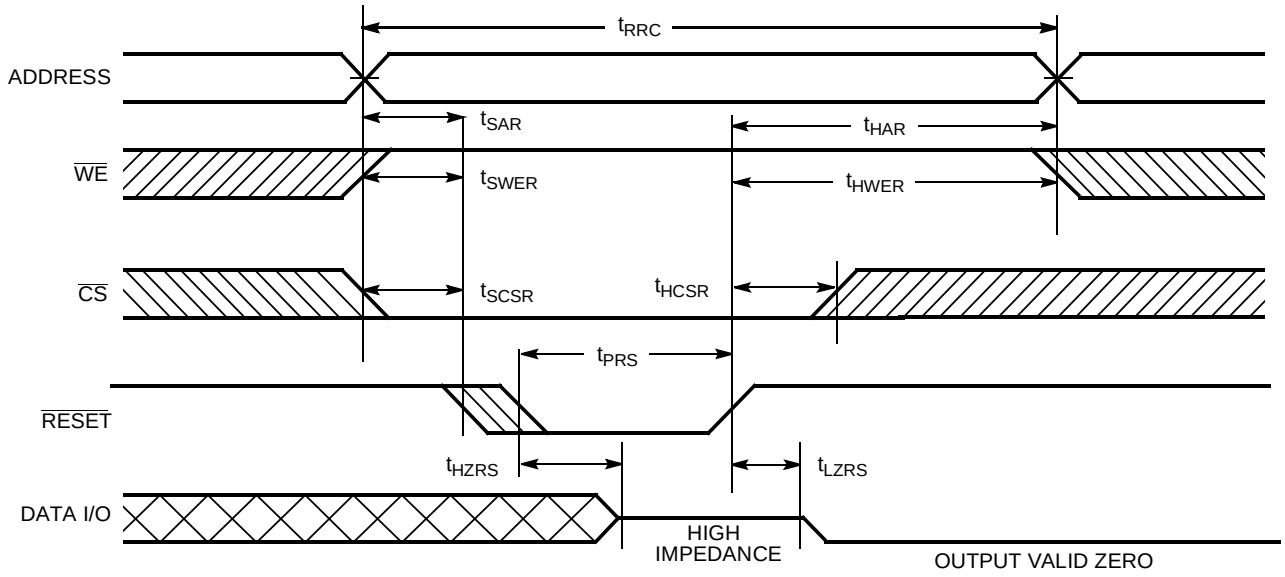
Reset Cycle [13]



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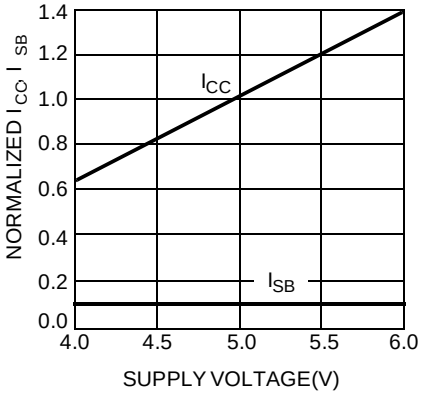
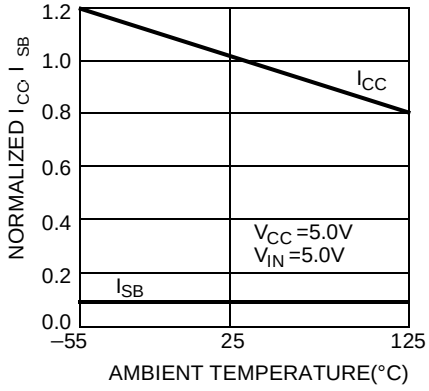
Notes:
12. If $\overline{CS}$ goes HIGH with $\overline{WE}$ HIGH, the output remains in a high-impedance state.
13. Reset cycle is defined by the overlap of $\overline{RS}$ and $\overline{CS}$ for the minimum reset pulse width.

Typical DC and AC Characteristics

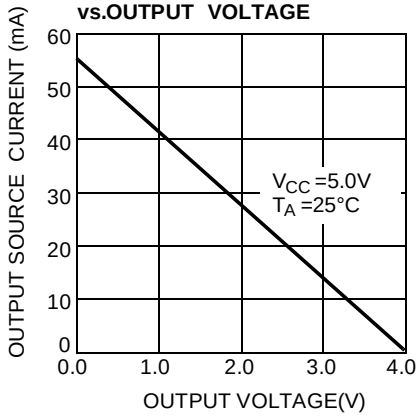
NORMALIZED SUPPLY CURRENT vs.SUPPLY VOLTAGE



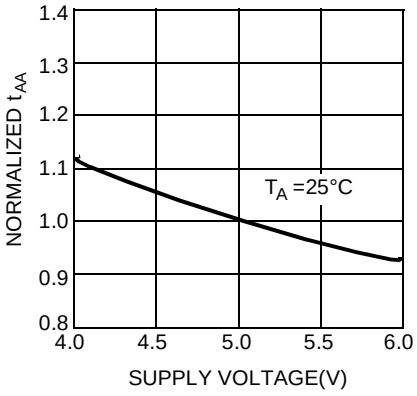
NORMALIZED SUPPLY CURRENT vs.AMBIENT TEMPERATURE



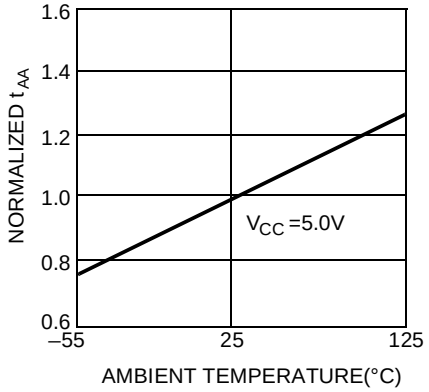
OUTPUT SOURCE CURRENT vs.OUTPUT VOLTAGE



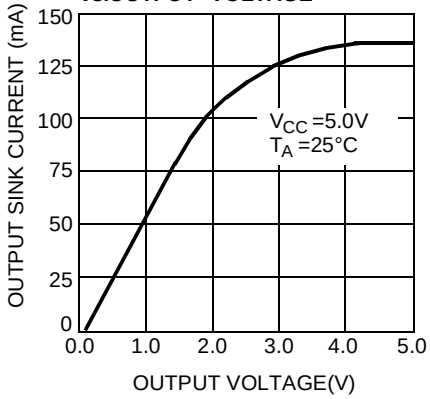
NORMALIZED ACCESS TIME vs.SUPPLY VOLTAGE



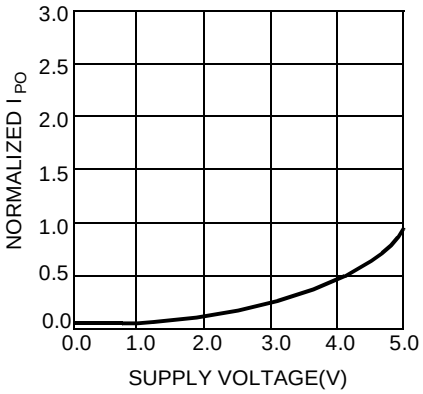
NORMALIZED ACCESS TIME vs.AMBIENT TEMPERATURE



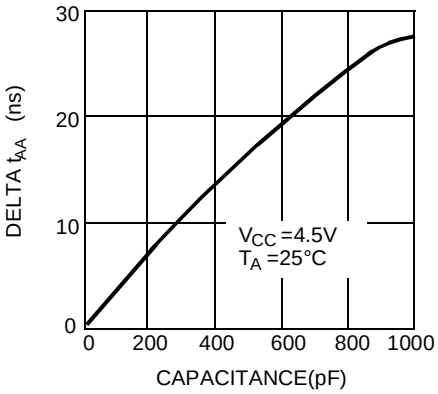
OUTPUT SINK CURRENT vs.OUTPUT VOLTAGE



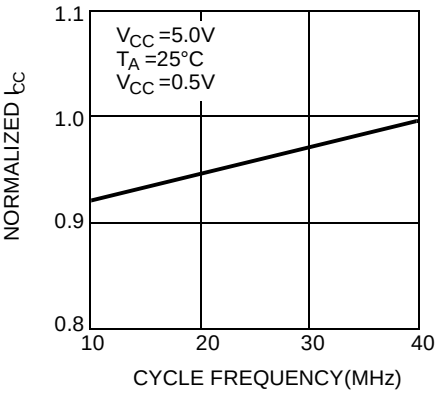
TYPICAL POWER–ON CURRENT vs.SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs.OUTPUT LOADING



NORMALIZED I_{CC} vs.CYCLE TIME



Truth Table

Inputs				Outputs	Mode
CS	WE	OE	RS		
H	X	X	X	High Z	Not Selected
L	H	X	L	High Z	Reset
L	L	X	H	High Z	Write
L	H	L	H	O_0–O_3	Read
L	X	H	H	High Z	Output Disable

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C150–10PC	P13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C150–10SC	S13	24-Lead Molded SOIC	
12	CY7C150–12PC	P13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C150–12SC	S13	24-Lead Molded SOIC	
	CY7C150–12DMB	D14	24-Lead (300-Mil) CerDIP	Military
15	CY7C150–15PC	P13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C150–15SC	S13	24-Lead Molded SOIC	
	CY7C150–15DMB	D14	24-Lead (300-Mil) CerDIP	Military
25	CY7C150–25PC	P13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C150–25SC	S13	24-Lead Molded SOIC	
	CY7C150–25DMB	D14	24-Lead (300-Mil) CerDIP	Military
35	CY7C150–35DMB	D14	24-Lead (300-Mil) CerDIP	Military

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACS}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCS}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11
RESET CYCLE	
t_{RRC}	7, 8, 9, 10, 11
t_{SAR}	7, 8, 9, 10, 11
t_{SWER}	7, 8, 9, 10, 11
t_{SCSR}	7, 8, 9, 10, 11
t_{PRS}	7, 8, 9, 10, 11
t_{HCSR}	7, 8, 9, 10, 11
t_{HWER}	7, 8, 9, 10, 11
t_{HAR}	7, 8, 9, 10, 11

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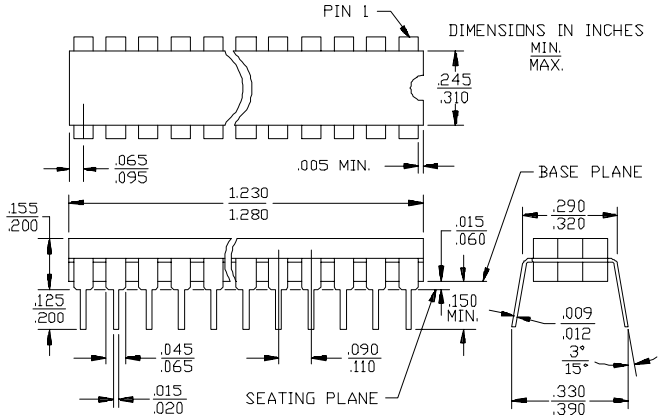
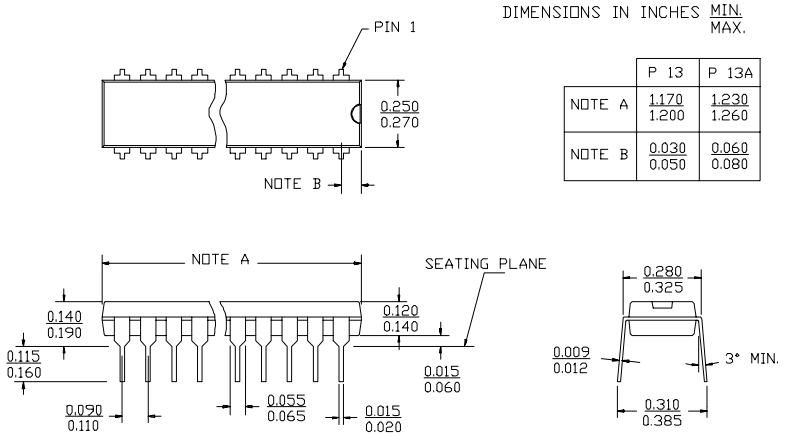
Package Diagrams

24-Lead (300-Mil) CerDIP D14
MIL-STD-1835 D- 9Config.A



24-Lead (300-Mil) Molded DIP P13/P13A



	P 13	P 13A
NOTE A	1.170 1.200	1.230 1.260
NOTE B	0.030 0.050	0.060 0.080

Package Diagrams (continued)

24-Lead Molded SOIC S13