*For new designs see CY7C371i*

# CY7C371

# UltraLogic™ 32-Macrocell Flash CPLD

## Features

- **32 macrocells in two logic blocks**
- **32 I/O pins**
- **6 dedicated inputs including 2 clock pins**
- **Bus Hold capabilities on all I/Os and dedicated inputs**
- **No hidden delays**
- **High speed**
  - **— $f_{MAX}$ = 143 MHz**
  - **— $t_{PD}$= 8.5 ns**
  - **— $t_S$ = 5 ns**
  - **— $t_{CO}$ = 6 ns**
- **Electrically alterable FLASH technology**
- **Available in 44-pin PLCC, CLCC, and TQFP packages**
- **Pin compatible with the CY7C372**

## Functional Description

The CY7C371 is a Flash erasable Complex Programmable Logic Device (CPLD) and is part of the FLASH370 family of high-density, high-speed CPLDs. Like all members of the FLASH370 family, the CY7C371 is designed to bring the ease of use and high performance of the 22V10 to high-density CPLDs.

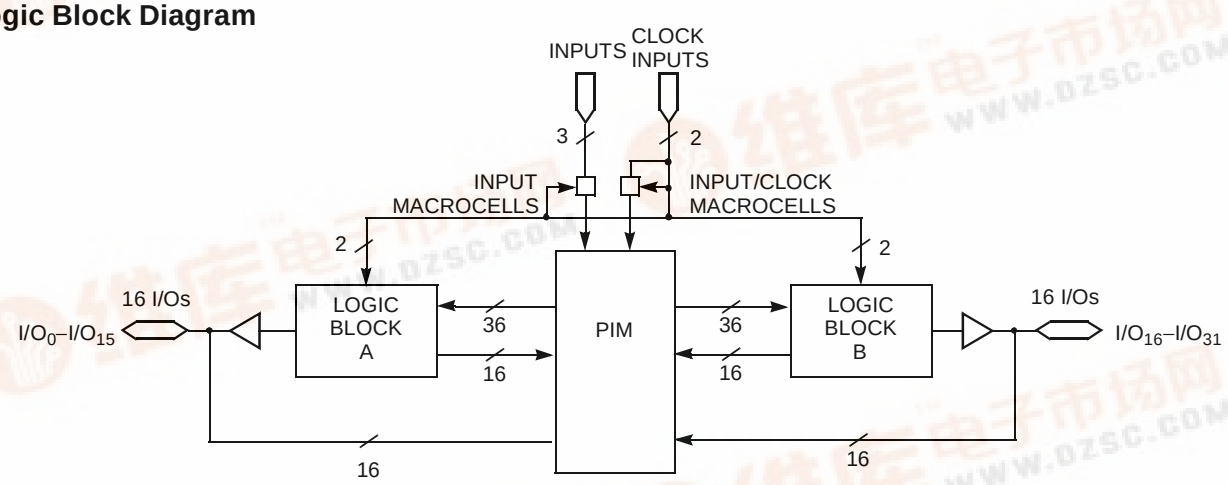
The 32 macrocells in the CY7C371 are divided between two logic blocks. Each logic block includes 16 macrocells, a 72 x 86 product term array, and an intelligent product term allocator.

The logic blocks in the FLASH370 architecture are connected with an extremely fast and predictable routing resource—the Programmable Interconnect Matrix (PIM). The PIM brings flexibility, routability, speed, and a uniform delay to the interconnect.

Like all members of the FLASH370 family, the CY7C371 is rich in I/O resources. Each macrocell in the device features an associated I/O pin, resulting in 32 I/O pins on the CY7C371. In addition, there are four dedicated inputs and two input/clock pins.

Finally, the CY7C371 features a very simple timing model. Unlike other high-density CPLD architectures, there are no hidden speed delays such as fanout effects, interconnect delays, or expander delays. Regardless of the number of resources used or the type of application, the timing parameters on the CY7C371 remain the same.

## Logic Block Diagram




## Selection Guide

| | | 7C371-143 | 7C371-110 | 7C371-83 | 7C371L-83 | 7C371-66 | 7C371L-66 |
|---|---|---|---|---|---|---|---|
| Maximum Propagation Delay, $t_{PD}$ (ns) | | 8.5 | 10 | 12 | 12 | 15 | 15 |
| Minimum Set-Up, $t_S$ (ns) | | 5 | 6 | 10 | 10 | 12 | 12 |
| Maximum Clock to Output, $t_{CO}$ (ns) | | 6 | 6.5 | 10 | 10 | 12 | 12 |
| Maximum Supply Current, $I_{CC}$ (mA) | Commercial | 220 | 175 | 175 | 90 | 175 | 90 |
| | Military/Ind. | | | 220 | 110 | 220 | 110 |

Shaded area contains preliminary information.