

## For new designs see CY7C372i

CY7C372

# UltraLogic™ 64-Macrocell Flash CPLD

#### **Features**

- 64 macrocells in four logic blocks
- 32 I/O pins
- · 6 dedicated inputs including 2 clock pins
- Bus Hold capabilities on all I/Os and dedicated inputs
- · No hidden delays
- · High speed
  - $-f_{MAX} = 125 MHz$
  - $-t_{PD} = 10 \text{ ns}$
  - $-t_{S} = 5.5 \text{ ns}$
  - $-t_{CO} = 6.5 \text{ ns}$
- Electrically alterable Flash technology
- · Available in 44-pin PLCC and CLCC packages
- Pin compatible with the CY7C371

#### **Functional Description**

The CY7C372 is a Flash erasable Complex Programmable Logic Device (CPLD) and is part of the FLASH370<sup>™</sup> family of high-density, high-speed CPLDs. Like all members of the FLASH370 family, the CY7C372 is designed to bring the ease

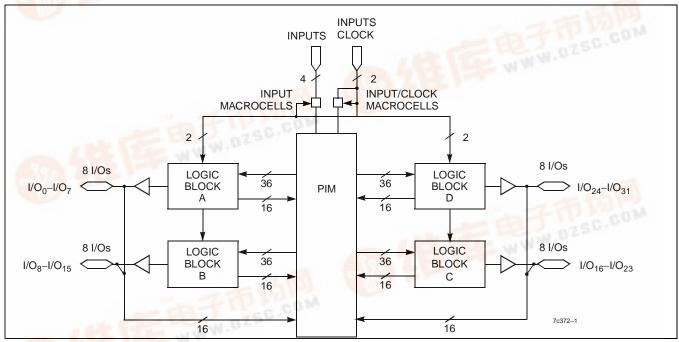
of use and high performance of the 22V10 to high-density CPLDs.

The 64 macrocells in the CY7C372 are divided between four logic blocks. Each logic block includes 16 macrocells, a 72 x 86 product term array, and an intelligent product term allocator.

The logic blocks in the FLASH370 architecture are connected with an extremely fast and predictable routing resource—the Programmable Interconnect Matrix (PIM). The PIM brings flexibility, routability, speed, and a uniform delay to the interconnect.

Like all members of the FLASH370 family, the CY7C372 is rich in I/O resources. Every two macrocells in the device feature an associated I/O pin, resulting in 32 I/O pins on the CY7C372. In addition, there are four dedicated inputs and two input/clock pins.

Finally, the CY7C372 features a very simple timing model. Unlike other high-density CPLD architectures, there are no hidden speed delays such as fanout effects, interconnect delays, or expander delays. Regardless of the number of resources used or the type of application, the timing parameters on the CY7C372 remain the same.



### **Selection Guide**

57/((p) ====		7C372-125	7C372-100	7C372-83	7C372-66	7C372L-66
Maximum Propagation Delay, t <sub>PD</sub> (ns)		10	12	15	20	20
Minimum Set-up, t <sub>S</sub> (ns)		5.5	6	8	10	10
Maximum Clock to Output, t <sub>CO</sub> (ns)		6.5	6.5	8	10	10
Maximum Supply Current, I <sub>CC</sub> (mA)	Commercial	280	250	250	250	125
	Military/Industrial			300	300	

Shaded areas contain preliminary information.