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CY7C451
CY7C453
CY7C454

512x9, 2Kx9, and 4Kx9 Cascadable Clocked FIFOs with Programmable Flags

Features

- High-speed, low-power, first-in first-out (FIFO) memories
- 512 x 9 (CY7C451)
- 2,048 x 9 (CY7C453)
- 4,096 x 9 (CY7C454)
- 0.65 micron CMOS for optimum speed/power
- High-speed 83-MHz operation (12 ns read/write cycle time)
- Low power — I_{CC}=70 mA
- Fully asynchronous and simultaneous read and write operation
- Empty, Full, Half Full, and programmable Almost Empty and Almost Full status flags
- TTL compatible
- Retransmit function
- Parity generation/checking
- Output Enable (OE) pins
- Independent read and write enable pins
- Center power and ground pins for reduced noise
- Supports free-running 50% duty cycle clock inputs
- Width Expansion Capability
- Depth Expansion Capability
- Available in PLCC packages

Functional Description

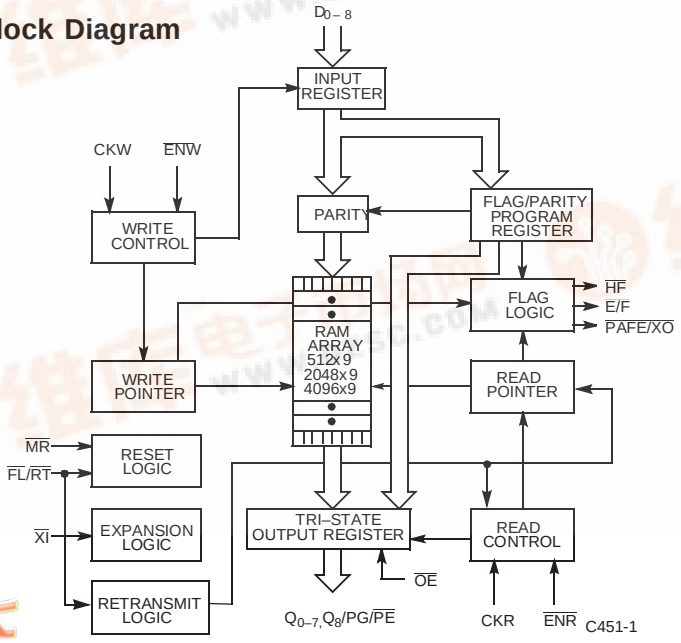
The CY7C451, CY7C453, and CY7C454 are high-speed, low-power, first-in first-out (FIFO) memories with clocked read and write interfaces. Both FIFOs are 9 bits wide. The CY7C451 has a 512-word by 9-bit memory array, the CY7C453 has a 2048-word by 9-bit memory array, and the CY7C454 has a 4096-word by 9-bit memory array. Devices can be cascaded to increase FIFO depth. Programmable features include Almost Full/Empty flags and generation/checking of parity. These FIFOs provide solutions for a wide variety of data buffering needs, including high-speed data acquisition, multiprocessor interfaces, and communications buffering.

Both FIFOs have 9-bit input and output ports that are controlled by separate clock and enable signals. The input port is controlled by a free-running clock (CKW) and a write enable pin ($\overline{ENW}$). When $\overline{ENW}$ is asserted, data is written into the FIFO on the rising edge of the CKW signal. While $\overline{ENW}$ is held active, data is continually written into the FIFO on each CKW cycle. The output port is controlled in a similar manner by a free-running read clock (CKR) and a read enable pin ($\overline{ENR}$). The read (CKR) and write (CKW) clocks may be tied together for single-clock operation or the two clocks may be run independently for asynchronous read/write applications. Clock frequencies up to 83.3 MHz are achievable in the standalone configuration, and up to 83.3 MHz is achievable when FIFOs are cascaded for depth expansion.

Depth expansion is possible using the cascade input ($\overline{XI}$) and cascade output ($\overline{XO}$). The $\overline{XO}$ signal is connected to the $\overline{XI}$ of the next device, and the $\overline{XO}$ of the last device should be connected to the $\overline{XI}$ of the first device. In standalone mode, the input ($\overline{XI}$) pin is simply tied to V_{SS}.

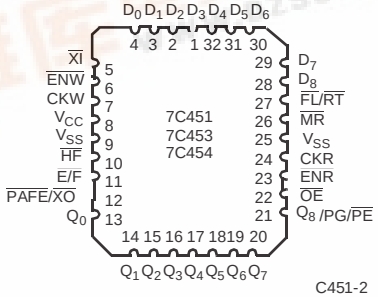
In the standalone and width expansion configurations, a LOW on the retransmit ($\overline{RT}$) input causes the FIFOs to retransmit the data. Read enable ($\overline{ENR}$) and the write enable ($\overline{ENW}$) must both be HIGH during the retransmit, and then $\overline{ENR}$ is used to access the data.

Logic Block Diagram



Pin Configurations

PLCC/LCC
Top View



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Functional Description (continued)

The CY7C451, CY7C453, and CY7C454 provide three status pins to the user. These pins are decoded to determine one of six states: Empty, Almost Empty, Less than or Equal to Half Full, Greater than Half Full, Almost Full, and Full (see *Table 1*). The Almost Empty/Full flag ($\overline{PAFE}$) and $\overline{XO}$ functions share the same pin. The Almost Empty/Full flag is valid in the standalone and width expansion configurations. In the depth expansion, this pin provides the expansion out ($\overline{XO}$) information that is used to signal the next FIFO when it will be activated.

The flags are synchronous, i.e., they change state relative to either the read clock (CKR) or the write clock (CKW). When entering or exiting the Empty and Almost Empty states, the flags are updated exclusively by the CKR. The flags denoting Half Full, Almost Full, and Full states are updated exclusively by CKW. The synchronous flag architecture guarantees that the flags maintain their status for some minimum time.

The CY7C451, CY7C453, and the CY7C454 use center power and ground for reduced noise. Both configurations are fabricated using an advanced RAM 2.8 technology. Input ESD protection is greater than 2001V, and latch-up is prevented by the use of reliable layout techniques and guard rings.

Selection Guide

		7C451-12 7C453-12 7C454-12	7C451-14 7C453-14 7C454-14	7C451-20 7C453-20 7C454-20	7C451-30 7C453-30 7C454-30
Maximum Frequency (MHz)		83.3	71.4	50	33.3
Maximum Cascadable Frequency		83.3	71.4	50	33.3
Maximum Access Time (ns)		9	10	15	20
Minimum Cycle Time (ns)		12	14	20	30
Minimum Clock HIGH Time (ns)		5	6.5	9	12
Minimum Clock LOW Time (ns)		5	6.5	9	12
Minimum Data or Enable Set-Up (ns)		4	5	6	7
Minimum Data or Enable Hold (ns)		0	0	0	0
Maximum Flag Delay (ns)		9	10	15	20
Maximum Current (mA)	Commercial	140	140	120	100
	Military/Industrial	150	150	130	110

Selection Guide (continued)

	CY7C451	CY7C453	CY7C454
Density	512 x 9	2,048 x 9	4,096 x 9
$\overline{OE}$, Depth Cascadable	Yes	Yes	Yes
Package	32-Pin PLCC	32-Pin PLCC	32-Pin PLCC

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–55°C to +125°C

Supply Voltage to Ground Potential .....–0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State.....–0.5V to +7.0V

DC Input Voltage .....–3.0V to +7.0V

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	–40°C to +85°C	5V ± 10%

Pin Definitions

Signal Name	I/O	Description
D_{0-8}	I	Data Inputs: When the FIFO is not full and $\overline{ENW}$ is active, CKW (rising edge) writes data (D_{0-8}) into the FIFO's memory. If $\overline{MR}$ is asserted at the rising edge of CKW then data is written into the FIFO's programming register. D_8 is ignored if the device is configured for parity generation.
Q_{0-7}	O	Data Outputs: When the FIFO is not empty and $\overline{ENR}$ is active, CKR (rising edge) reads data (Q_{0-7}) out of the FIFO's memory. If $\overline{MR}$ is active at the rising edge of CKR then data is read from the programming register.
Q_8/PG/$\overline{PE}$	O	Function varies according to mode: Parity disabled - same function as Q_{0-7} Parity enabled, generation - parity generation bit (PG) Parity enabled, check - Parity Error Flag ($\overline{PE}$)
$\overline{ENW}$	I	Enable Write: enables the CKW input (for both non-program and program modes)
$\overline{ENR}$	I	Enable Read: enables the CKR input (for both non-program and program modes)
CKW	I	Write Clock: the rising edge clocks data into the FIFO when $\overline{ENW}$ is LOW; updates Half Full, Almost Full, and Full flag states. When $\overline{MR}$ is asserted, CKW writes data into the program register.
CKR	I	Read Clock: the rising edge clocks data out of the FIFO when $\overline{ENR}$ is LOW; updates the Empty and Almost Empty flag states. When $\overline{MR}$ is asserted, CKR reads data out of the program register.
$\overline{HF}$	O	Half Full Flag - synchronized to CKW.
$\overline{E}$/$\overline{F}$	O	Empty or Full Flag - $\overline{E}$ is synchronized to CKR; $\overline{F}$ is synchronized to CKW
$\overline{PAFE}$/$\overline{XO}$	O	Dual-Mode Pin: Not Cascaded - Programmable Almost Full is synchronized to CKW; Programmable Almost Empty is synchronized to CKR Cascaded - Expansion Out signal, connected to $\overline{XI}$ of next device
$\overline{XI}$	I	Not Cascaded - $\overline{XI}$ is tied to V_{SS} Cascaded - Expansion Input, connected to $\overline{XO}$ of previous device
$\overline{FL}$/$\overline{RT}$	I	First Load/ Retransmit Pin: Cascaded - the first device in the daisy chain will have $\overline{FL}$ tied to V_{SS}; all other devices will have $\overline{FL}$ tied to V_{CC} (*Figure 2*) Not Cascaded - tied to V_{CC}; Retransmit function is also available in stand alone mode by strobing $\overline{RT}$
$\overline{MR}$	I	Master Reset: resets device to empty condition. Non-Programming Mode: program register is reset to default condition of no parity and $\overline{PAFE}$ active at 16 or less locations from Full/Empty. Programming Mode: Data present on D_{0-8} is written into the programmable register on the rising edge of CKW. Program register contents appear on Q_{0-8} after the rising edge of CKR.
$\overline{OE}$	I	Output Enable for Q_{0-7} and Q_8/PG/$\overline{PE}$ pins

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		7C451-12 7C453-12 7C454-12		7C451-14 7C453-14 7C454-14		7C451-20 7C453-20 7C454-20		7C451-30 7C453-30 7C454-30		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –2.0 mA		2.4		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4		0.4	V
V_{IH}[1]	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}[1]	Input LOW Voltage			–0.5	0.8	–0.5	0.8	–0.5	0.8	–0.5	0.8	V
I_{IX}	Input Leakage Current	V_{CC} = Max.		–10	+10	–10	+10	–10	+10	–10	+10	µA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = GND		–90		–90		–90		–90		mA
I_{OZL} I_{OZH}	Output OFF, High Z Current	$\overline{OE} \geq V_{IH}$, $V_{SS} < V_O < V_{CC}$		–10	+10	–10	+10	–10	+10	–10	+10	µA
I_{CC1}[3]	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		140		140		120		100	mA
			Mil/Ind		150		150		130		110	mA
I_{CC2}[4]	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		70		70		70		70	mA
			Mil/Ind		80		80		80		80	mA
I_{SB}[5]	Standby Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		30		30		30		30	mA
			Mil/Ind		30		30		30		30	mA

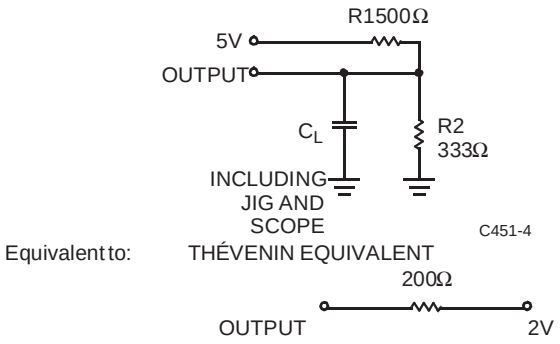
Capacitance[6]

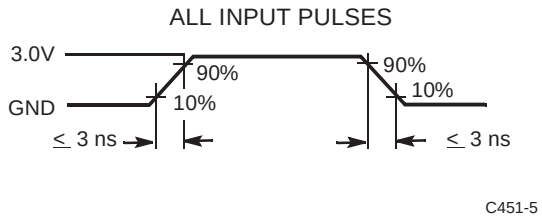
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		12	pF

Notes:

1. The V_{IH} and V_{IL} specifications apply for all inputs except $\overline{XI}$. The $\overline{XI}$ pin is not a TTL input. It is connected to either $\overline{XO}$ of the previous device or V_{SS}.
2. Test no more than one output at a time for not more than one second.
3. Input signals switch from 0V to 3V with a rise/fall time of less than 3 ns, clocks and clock enables switch at maximum frequency (f_{MAX}), while data inputs switch at $f_{MAX}/2$. Outputs are unloaded.
4. Input signals switch from 0V to 3V with a rise/fall time less than 3 ns, clocks and clock enables switch at 20 MHz, while the data inputs switch at 10 MHz. Outputs are unloaded.
5. All input signals are connected to V_{CC}. All outputs are unloaded. Read and write clocks switch at maximum frequency (f_{MAX}).
6. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms[7, 8, 9, 10, 11]





Switching Characteristics Over the Operating Range[12]

Parameter	Description	7C451-12 7C453-12 7C454-12		7C451-14 7C453-14 7C454-14		7C451-20 7C453-20 7C454-20		7C451-30 7C453-30 7C454-30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{CKW}	Write Clock Cycle	12		14		20		30		ns
t_{CKR}	Read Clock Cycle	12		14		20		30		ns
t_{CKH}	Clock HIGH	5		6.5		9		12		ns
t_{CKL}	Clock LOW	5		6.5		9		12		ns
t_A[13]	Data Access Time		9		10		15		20	ns
t_{OH}	Previous Output Data Hold After Read HIGH	0		0		0		0		ns
t_{FH}	Previous Flag Hold After Read/Write HIGH	0		0		0		0		ns
t_{SD}	Data Set-Up	4		5		6		7		ns
t_{HD}	Data Hold	0		0		0		0		ns
t_{SEN}	Enable Set-Up	4		5		6		7		ns
t_{HEN}	Enable Hold	0		0		0		0		ns
t_{OE}	$\overline{OE}$ LOW to Output Data Valid		9		10		15		20	ns
t_{OLZ}[6,14]	$\overline{OE}$ LOW to Output Data in Low Z	0		0		0		0		ns
t_{OHZ}[6,14]	$\overline{OE}$ HIGH to Output Data in High Z		9		10		15		20	ns
t_{PG}	Read HIGH to Parity Generation		9		10		15		20	ns
t_{PE}	Read HIGH to Parity Error Flag		9		10		15		20	ns
t_{FD}	Flag Delay		9		10		15		20	ns
t_{SKEW1}[15]	Opposite Clock After Clock	0		0		0		0		ns

Notes:

7. C_L = 30 pF for all AC parameters except for t_{OHZ}.
8. C_L = 5 pF for t_{OHZ}.
9. All AC measurements are referenced to 1.5V except t_{OE}, t_{OLZ}, and t_{OHZ}.
10. t_{OE} and t_{OLZ} are measured at ± 100 mV from the steady state.
11. t_{OHZ} is measured at +500 mV from V_{OL} and – 500 mV from V_{OH}.
12. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, and output loading as shown in AC Test Loads and Waveforms and capacitance as in notes 7 and 8, unless otherwise specified.
13. Access time includes all data outputs switching simultaneously.
14. At any given temperature and voltage condition, t_{OLZ} is greater than t_{OHZ} for any given device.
15. t_{SKEW1} is the minimum time an opposite clock can occur after a clock and still be guaranteed not to be included in the current clock cycle (for purposes of flag update). If the opposite clock occurs less than t_{SKEW1} after the clock, the decision of whether or not to include the opposite clock in the current clock cycle is arbitrary. *Note*: The opposite clock is the signal to which a flag is not synchronized; i.e., CKW is the opposite clock for Empty and Almost Empty flags, CKR is the opposite clock for the Almost Full, Half Full, and Full flags. The clock is the signal to which a flag is synchronized; i.e., CKW is the clock for the Half Full, Almost Full, and Full flags, CKR is the clock for Empty and Almost Empty flags.

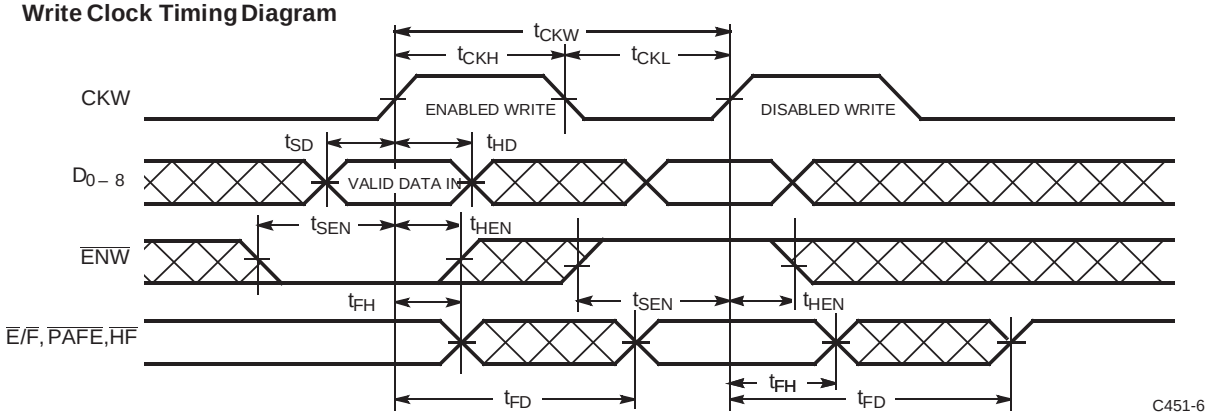
Switching Characteristics Over the Operating Range[12] (continued)

Parameter	Description	7C451-12 7C453-12 7C454-12		7C451-14 7C453-14 7C454-14		7C451-20 7C453-20 7C454-20		7C451-30 7C453-30 7C454-30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{SKEW2}[16]	Opposite Clock Before Clock	12		14		20		30		ns
t_{PMR}	Master Reset Pulse Width ($\overline{MR}$ LOW)	12		14		20		30		ns
t_{SCMR}	Last Valid Clock LOW Set-Up to $\overline{MR}$ LOW	0		0		0		0		ns
t_{OHMR}	Data Hold From $\overline{MR}$ LOW	0		0		0		0		ns
t_{MRR}	Master Reset Recovery ($\overline{MR}$ HIGH Set-Up to First Enabled Write/Read)	12		14		20		30		ns
t_{MRF}	$\overline{MR}$ HIGH to Flags Valid		12		14		20		30	ns
t_{AMR}	$\overline{MR}$ HIGH to Data Outputs LOW		12		14		20		30	ns
t_{SMRP}	Program Mode—$\overline{MR}$ LOW Set-Up	12		14		20		30		ns
t_{HMRP}	Program Mode—$\overline{MR}$ LOW Hold	9		10		15		25		ns
t_{FTP}	Program Mode—Write HIGH to Read HIGH	12		14		20		30		ns
t_{AP}	Program Mode—Data Access Time		12		14		20		30	ns
t_{OHP}	Program Mode—Data Hold Time from $\overline{MR}$ HIGH	0		0		0		0		ns
t_{PRT}	Retransmit Pulse Width	12		14		20		30		
t_{RTR}	Retransmit Recovery Time	12		14		20		30		

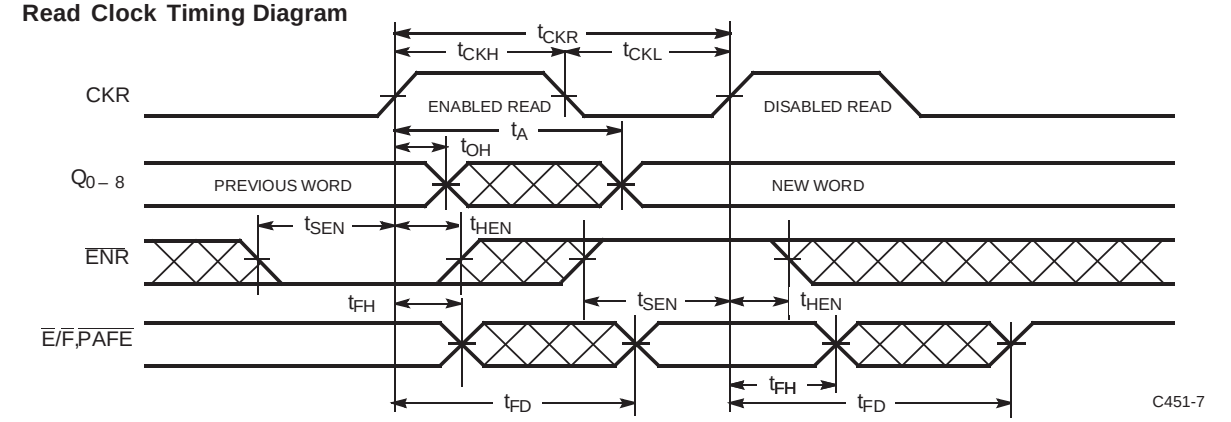
16. t_{SKEW2} is the minimum time an opposite clock can occur before a clock and still be guaranteed to be included in the current clock cycle (for purposes of flag update). If the opposite clock occurs less than t_{SKEW2} before the clock, the decision of whether or not to include the opposite clock in the current clock cycle is arbitrary. See Note 15 for definition of clock and opposite clock.

Switching Waveforms

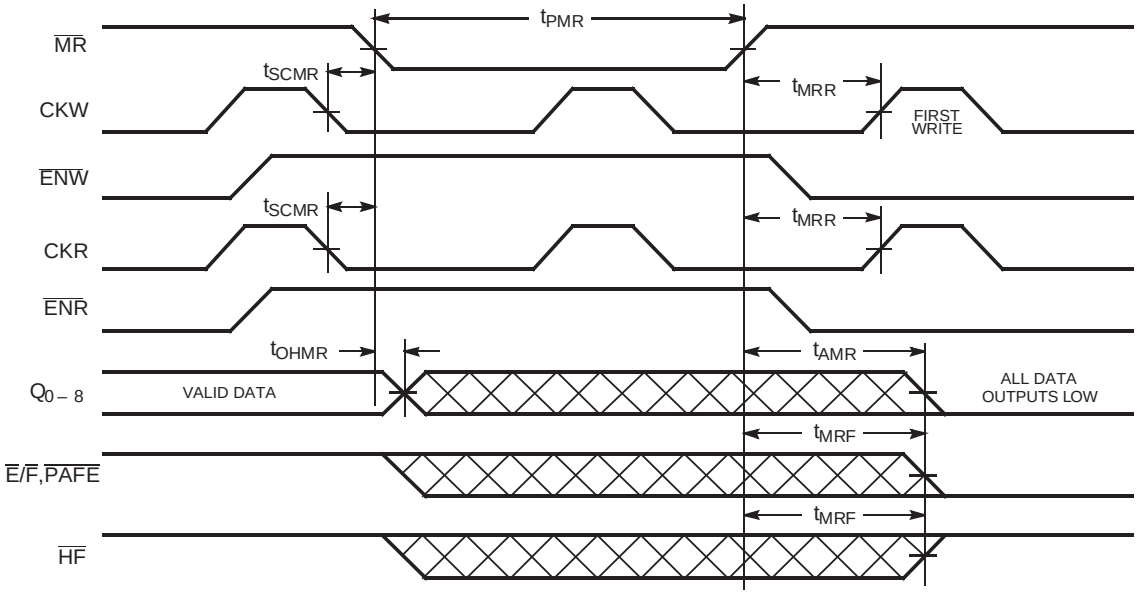
Write Clock Timing Diagram



Read Clock Timing Diagram



Master Reset (Default with Free-Running Clocks) Timing Diagram [17,18,19,20]

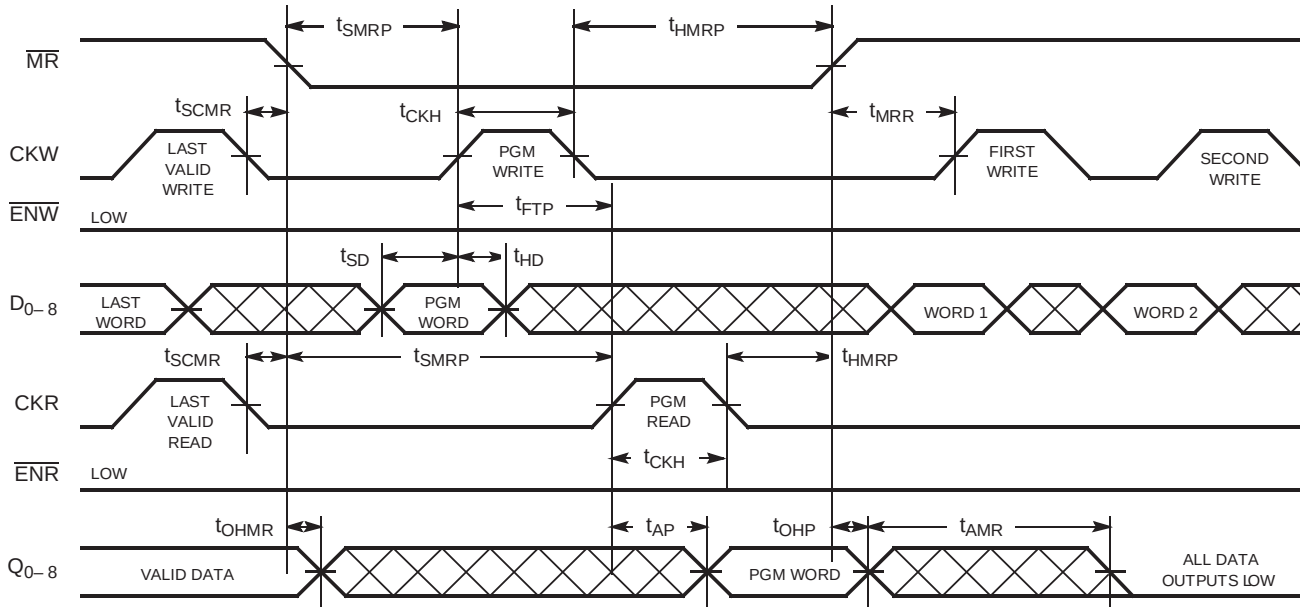


Notes:

17. To only perform reset (no programming), the following criteria must be met: ENW or CKW must be inactive while MR is LOW.
18. To only perform reset (no programming), the following criteria must be met: ENR or CKR must be inactive while MR is LOW.
19. All data outputs (Q_{0-8}) go LOW as a result of the rising edge of MR after t_{AMR}.
20. In this example, Q_{0-8} will remain valid until t_{OHMR} if either the first read shown did not occur or if the read occurred soon enough such that the valid data was caused by it.

Switching Waveforms (continued)

Master Reset (Programming Mode) Timing Diagram[19,20]



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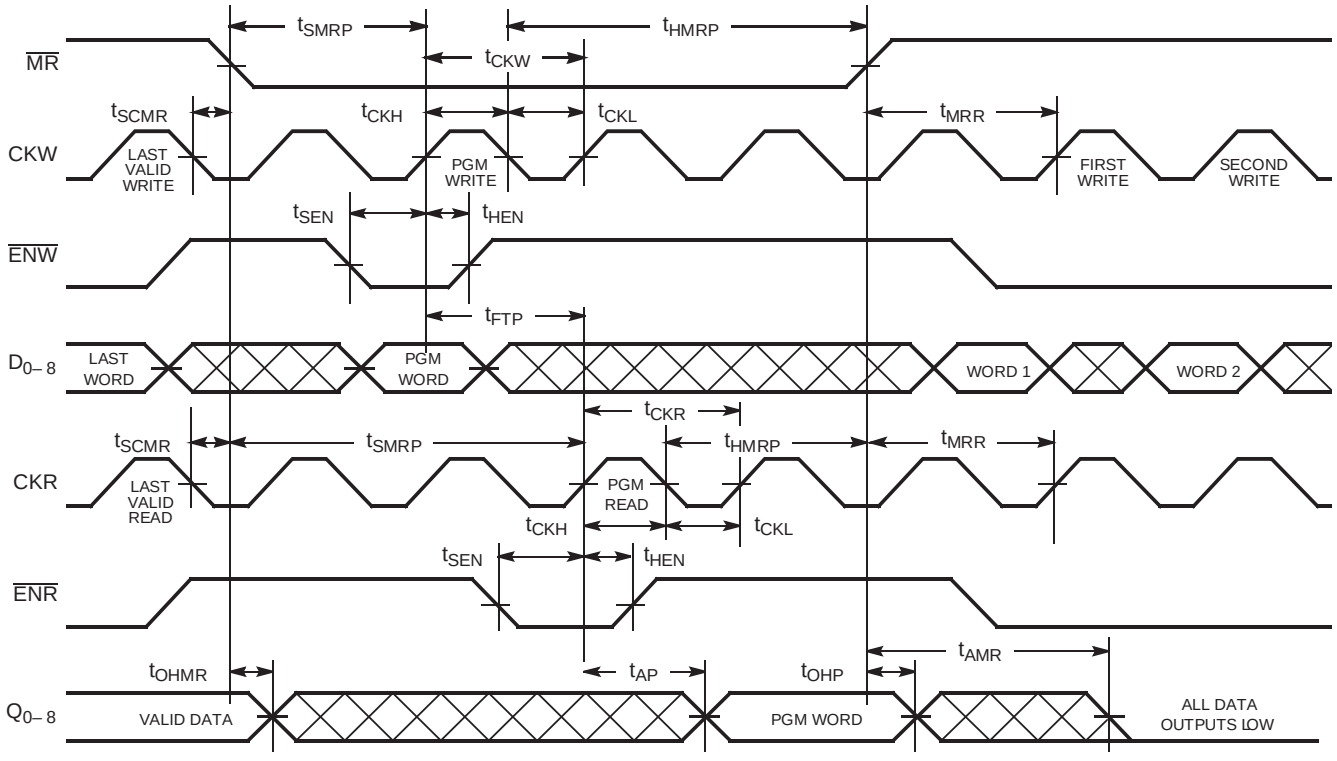
Master Reset (Programming Mode with Free-Running Clocks) Timing Diagram[19,20]



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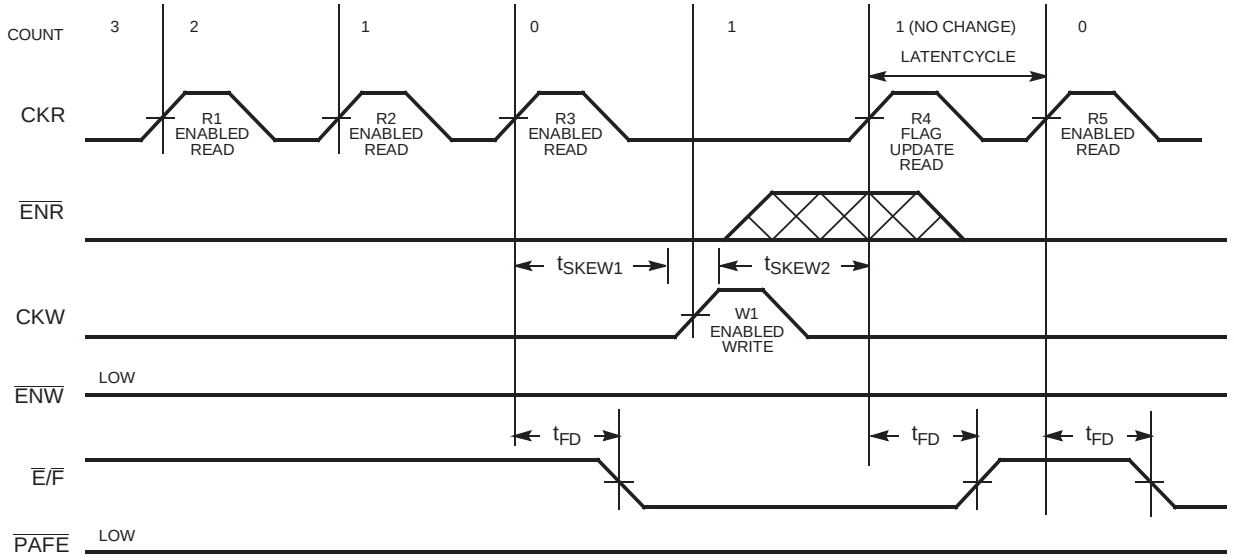
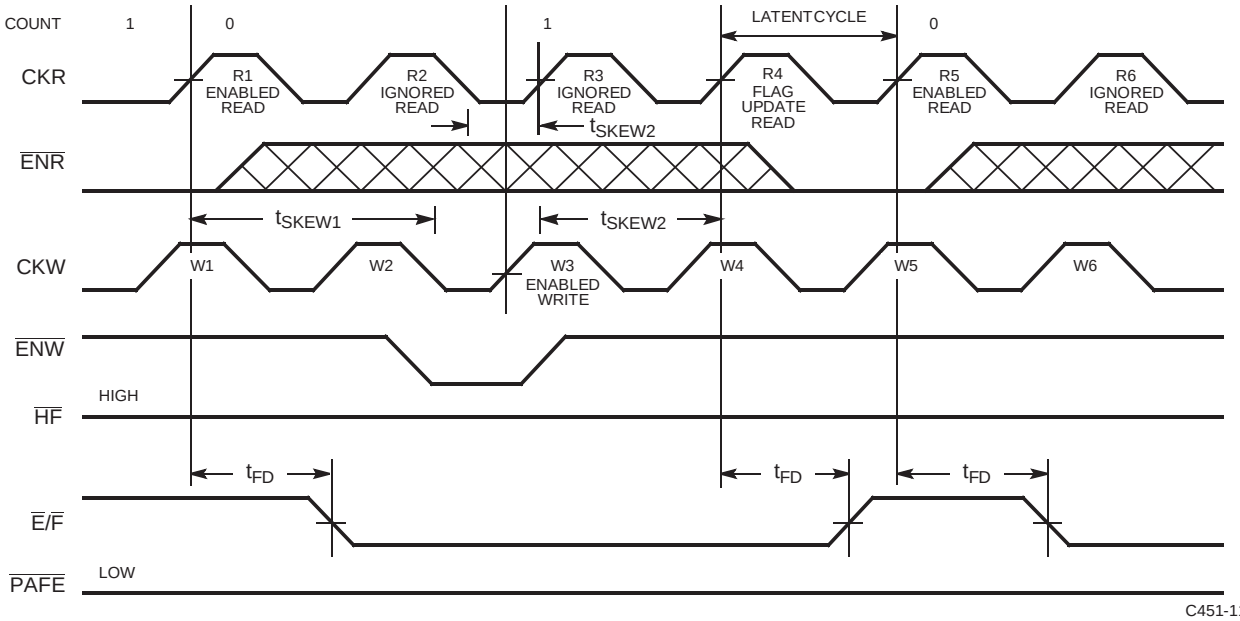
Switching Waveforms (continued)

Read to Empty Timing Diagram[21,24,25]



C451-12

Read to Empty Timing Diagram with Free-Running Clocks[21,22,23,24]



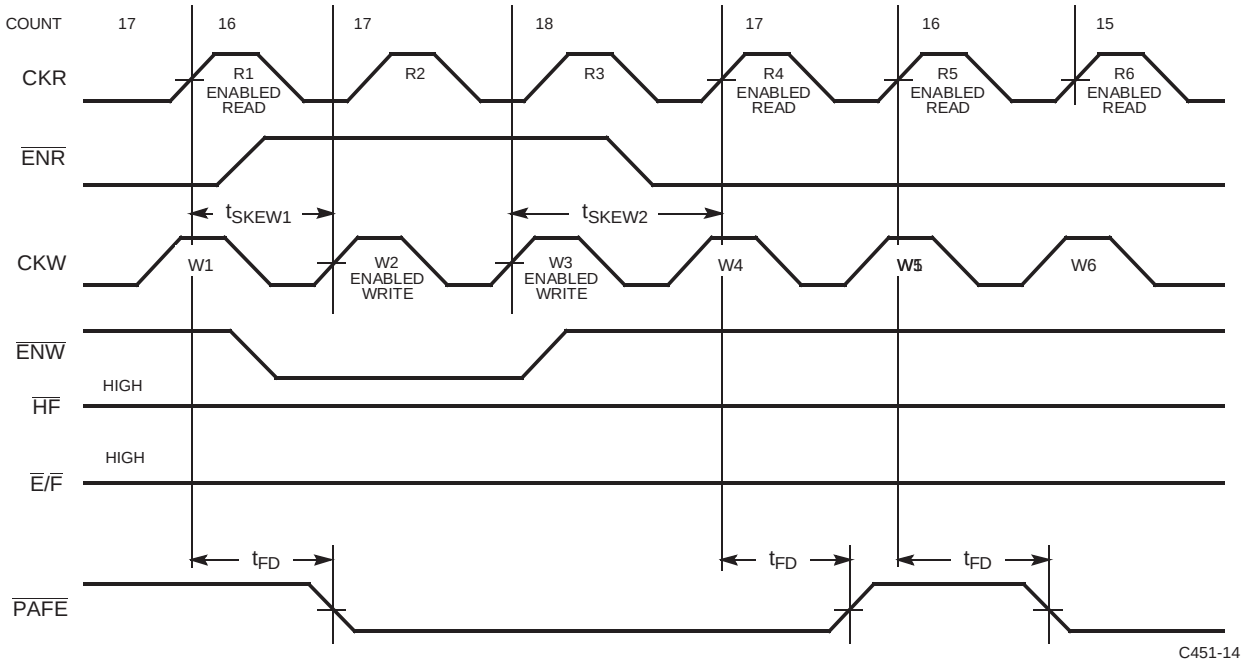
C451-11

Notes:

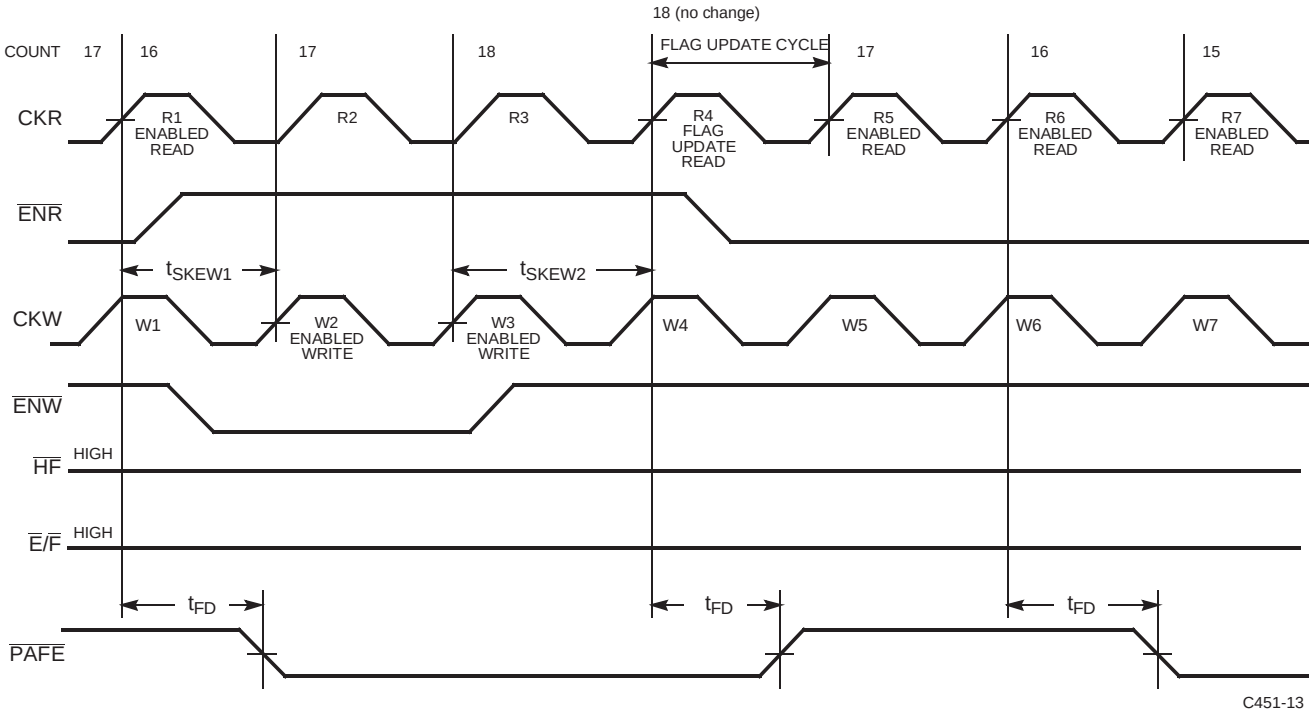
21. "Count" is the number of words in the FIFO.
22. The FIFO is assumed to be programmed with P>0 (i.e., $\overline{PAFE}$ does not transition at Empty or Full).
23. R2 is ignored because the FIFO is empty (count = 0). It is important to note that R3 is also ignored because W3, the first enabled write after empty, occurs less than t_{SKEW2} before R3. Therefore, the FIFO still appears empty when R3 occurs. Because W3 occurs greater than t_{SKEW2} before R4, R4 includes W3 in the flag update.
24. CKR is clock; CKW is opposite clock.
25. R3 updates the flag to the Empty state by asserting $\overline{E}/\overline{F}$. Because W1 occurs greater than t_{SKEW1} after R3, R3 does not recognize W1 when updating flag status. But because W1 occurs greater than t_{SKEW2} before R4, R4 includes W1 in the flag update and, therefore, updates FIFO to Almost Empty state. It is important to note that R4 is a latent cycle; i.e., it only updates the flag status regardless of the state of $\overline{ENR}$. It does not change the count or the FIFO's data outputs.

Switching Waveforms (continued)

Read to Almost Empty Timing Diagram with Free-Running Clocks [21,24,26]



Read to Almost Empty Timing Diagram with Read Flag Cycle and Update Free-Running Clocks [21,24,26,27,28]

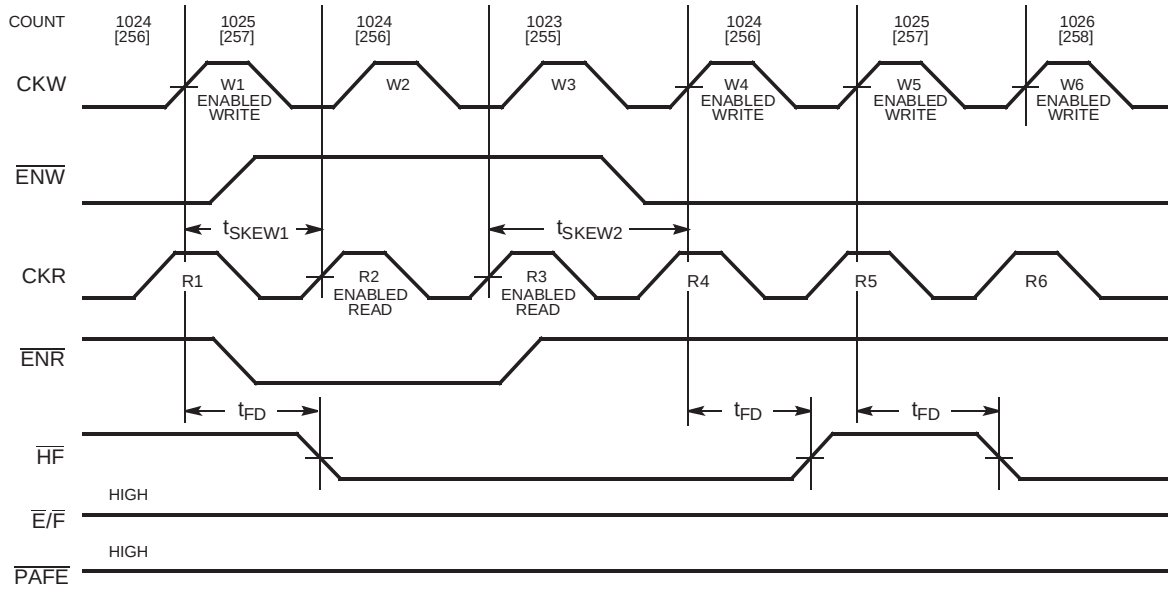


Notes:

26. The FIFO in this example is assumed to be programmed to its default flag values. Almost Empty is 16 words from Empty; Almost Full is 16 locations from Full.
27. R4 only updates the flag status. It does not affect the count because $\overline{ENR}$ is HIGH.
28. When making the transition from Almost Empty to Intermediate, the count must increase by two (16 =>18; two enabled writes: W2, W3) before a read (R4) can update flags to the Less Than Half Full state.

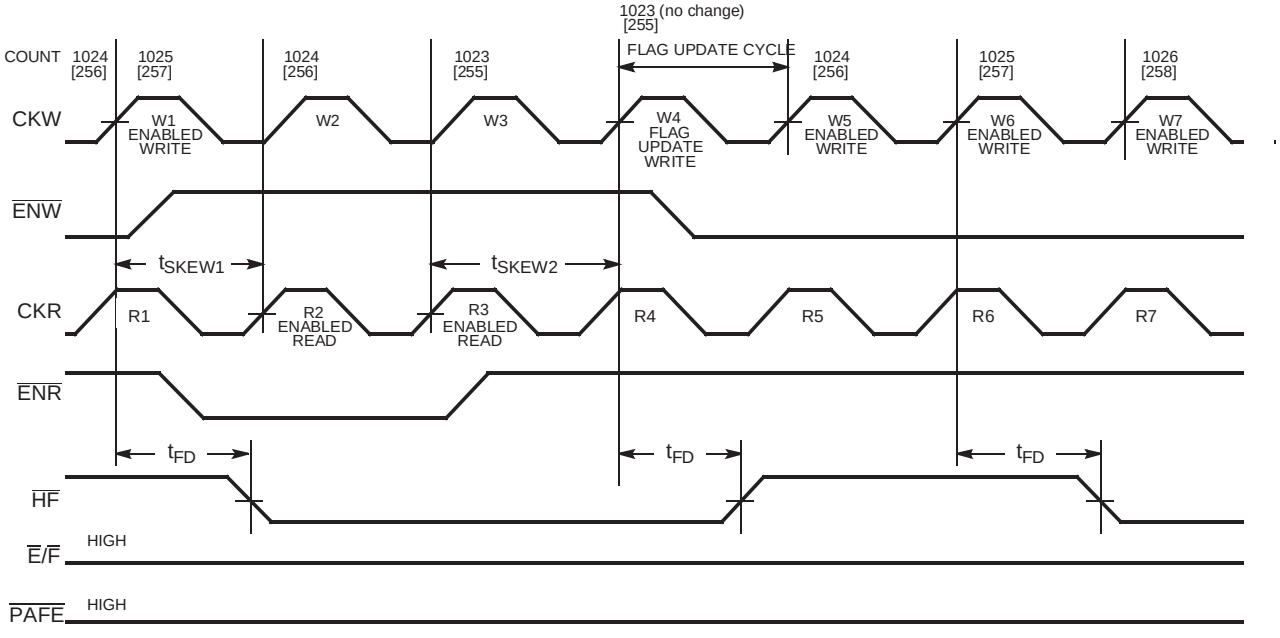
Switching Waveforms (continued)

Write to Half Full Timing Diagram with Free-Running Clocks [21,29,30,31]



C451-15

Write to Half Full Timing Diagram with Write Flag Update Cycle with Free-Running Clocks [21,29,30,31,32,33]



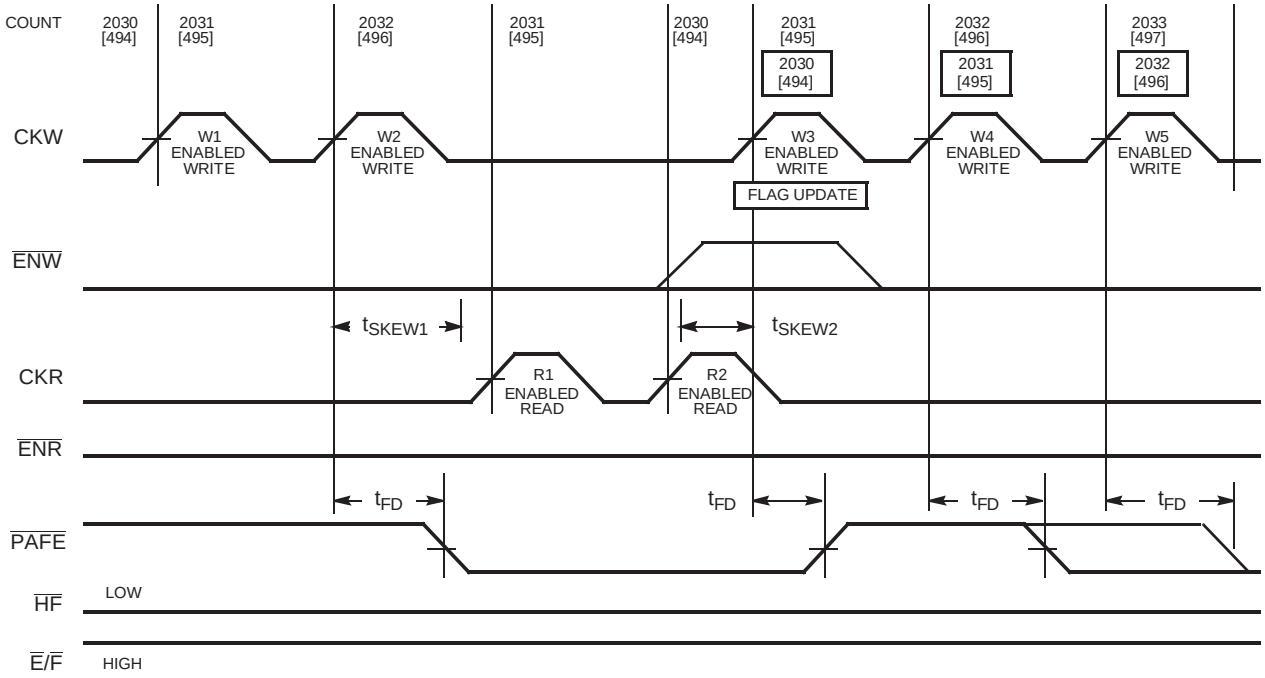
C451-16

Notes:

29. CKW is clock and CKR is opposite clock.
30. Count = 2,049 indicates Half Full for the CY7C454, count=1,025 indicates Half Full for the CY7C453, and count = 257 indicates Half Full for the CY7C451. Values for CY7C451 count are shown in brackets.
31. When the FIFO contains 2048[1024,256] words, the rising edge of the next enabled write causes the $\overline{HF}$ to be true (LOW).
32. The $\overline{HF}$ write flag update cycle does not affect the count because $\overline{ENW}$ is HIGH. It only updates $\overline{HF}$ to HIGH.
33. When making the transition from Half Full to Less Than Half Full, the count must decrease by two (1,025 =>1,023; two enabled reads: R2 and R3) before a write (W4) can update flags to less than Half Full.

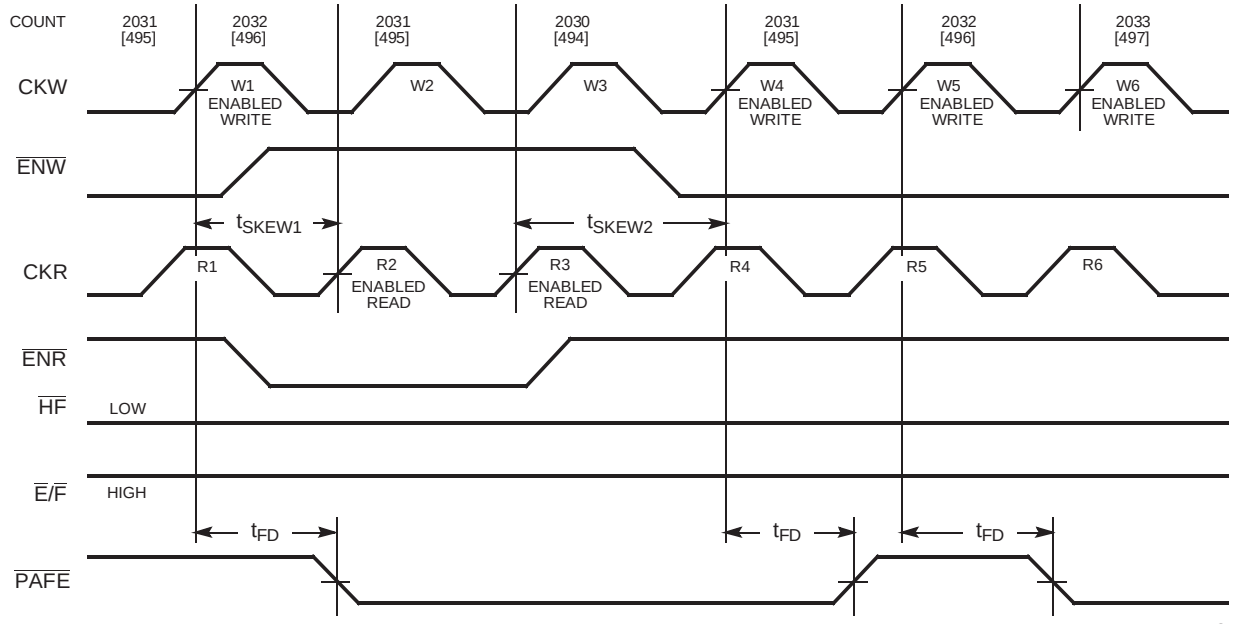
Switching Waveforms (continued)

Write to Almost Full Timing Diagram [21,26,29,34,35]



C451-18

Write to Almost Full Timing Diagram with Free-Running Clocks [21,26,29]



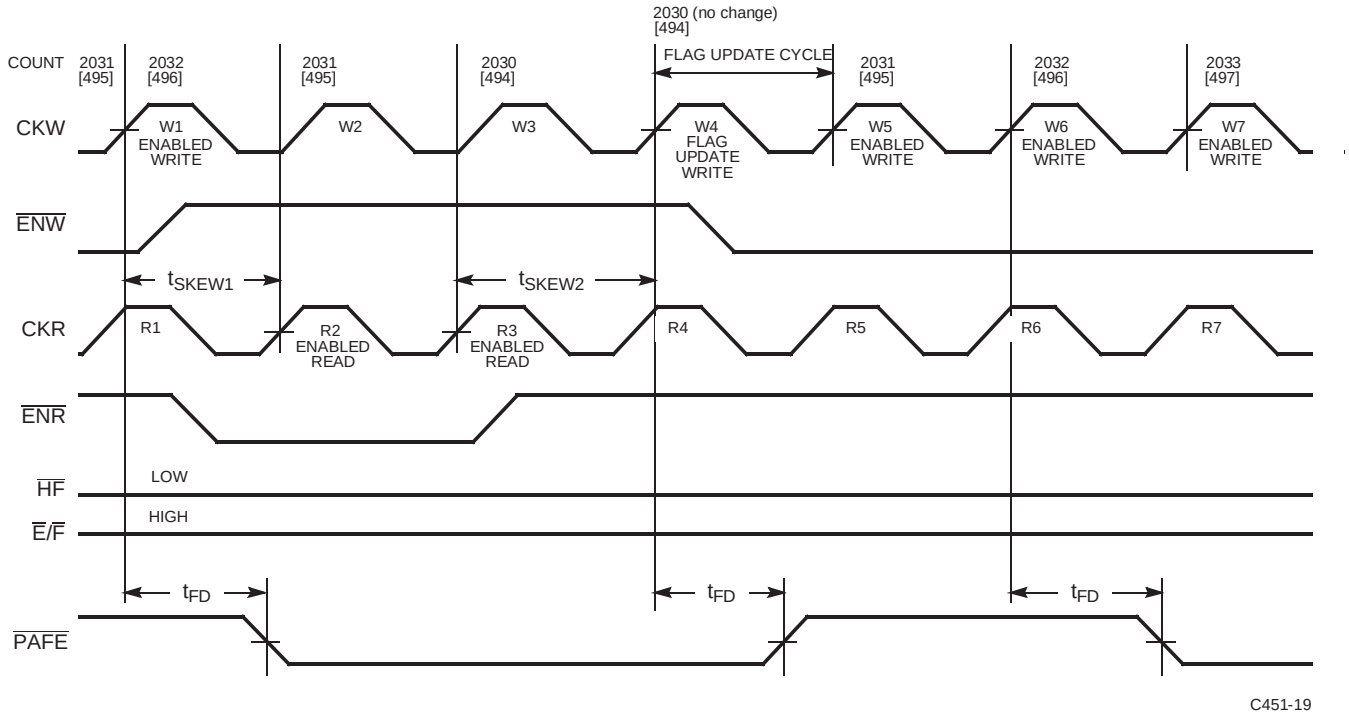
C451-17

Notes:

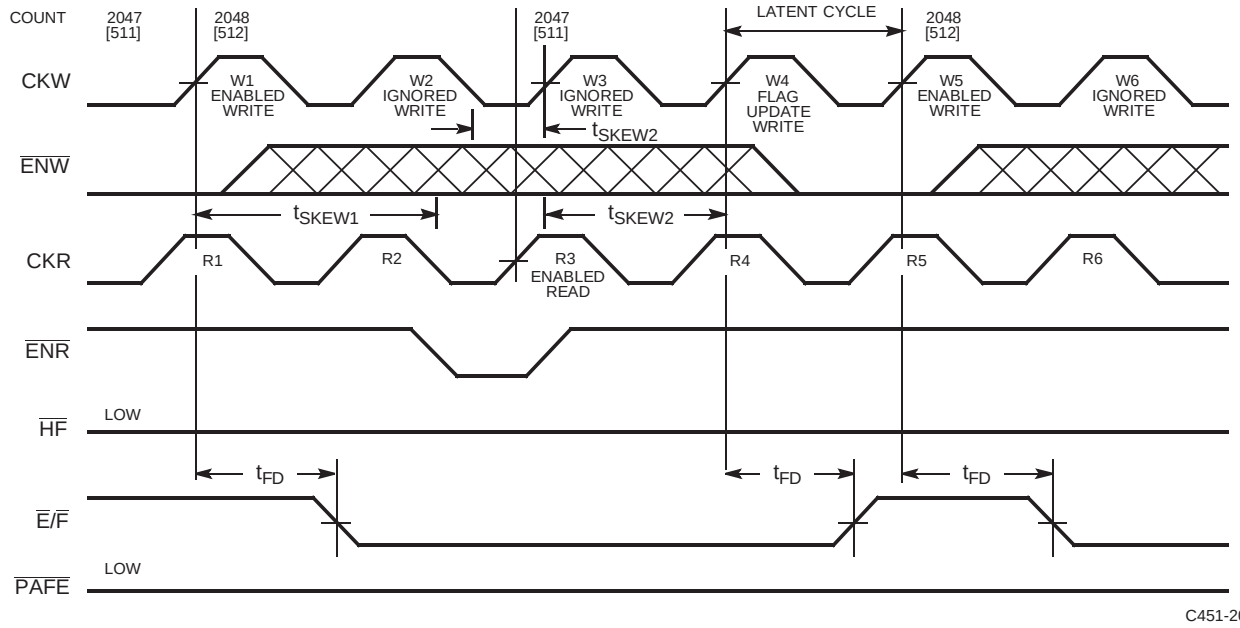
34. W2 updates the flag to the Almost Full state by asserting $\overline{PAFE}$. Because R1 occurs greater than t_{SKEW1} after W2, W2 does not recognize R1 when updating the flag status. W3 includes R2 in the flag update because R2 occurs greater than t_{SKEW2} before W3. Note that W3 does not have to be enabled to update flags.
35. The dashed lines show W3 as a flag update write rather than an enabled write because $\overline{ENW}$ is deasserted.

Switching Waveforms (continued)

Write to Almost Full Timing Diagram with Write Flag Update Cycle and Free-Running Clocks[21,26,29]



Write to Full Flag Timing Diagram with Free-Running Clocks[21,22,29,36]

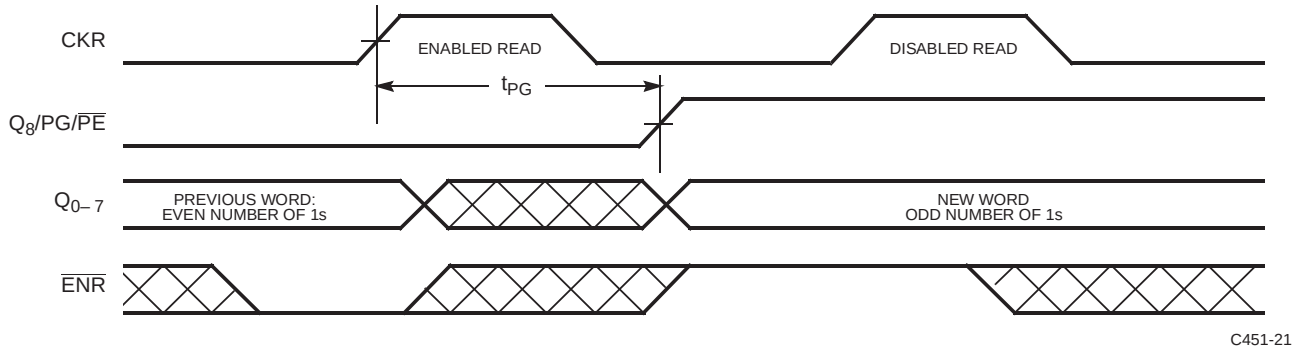


Note:

36. W2 is ignored because the FIFO is full (count = 4096[2048,512]). It is important to note that W3 is also ignored because R3, the first enabled read after full, occurs less than t_{SKEW2} before W3. Therefore, the FIFO still appears full when W3 occurs. Because R3 occurs greater than t_{SKEW2} before W4, W4 includes R3 in the flag update.

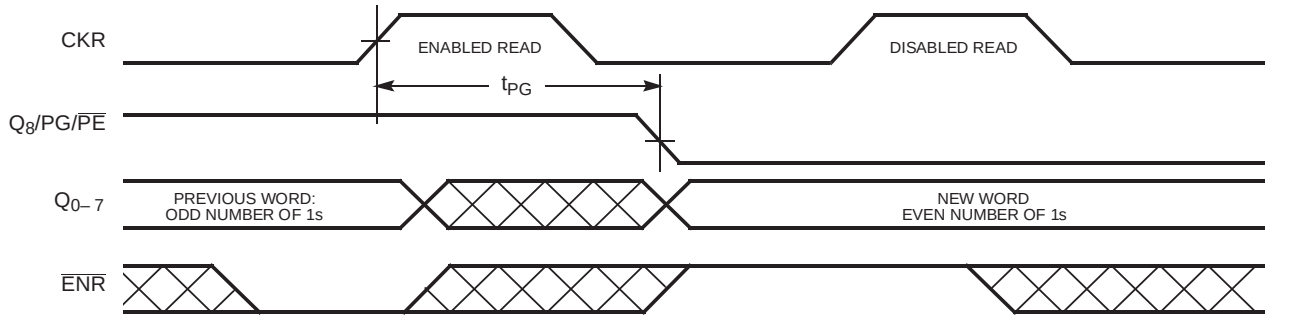
Switching Waveforms (continued)

Even Parity Generation Timing Diagram [37,38]



C451-21

Even Parity Generation Timing Diagram [37,39]



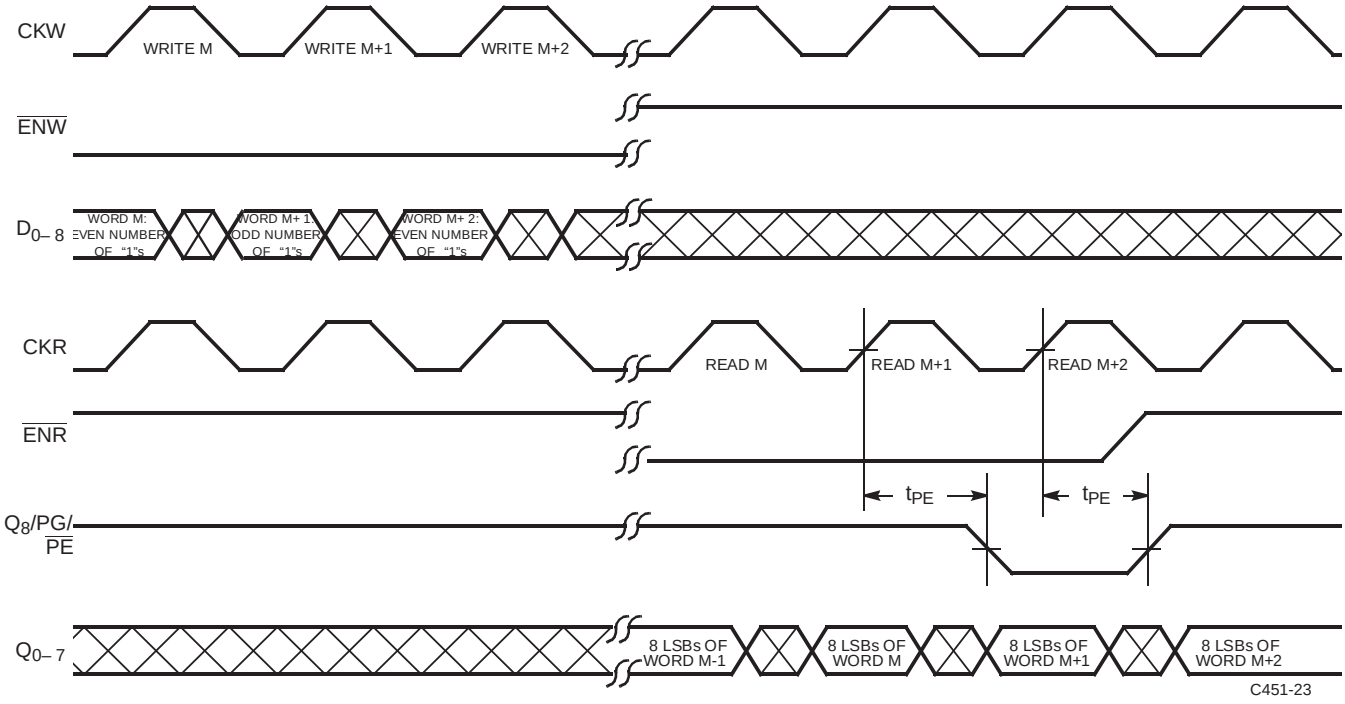
C451-22

Notes:

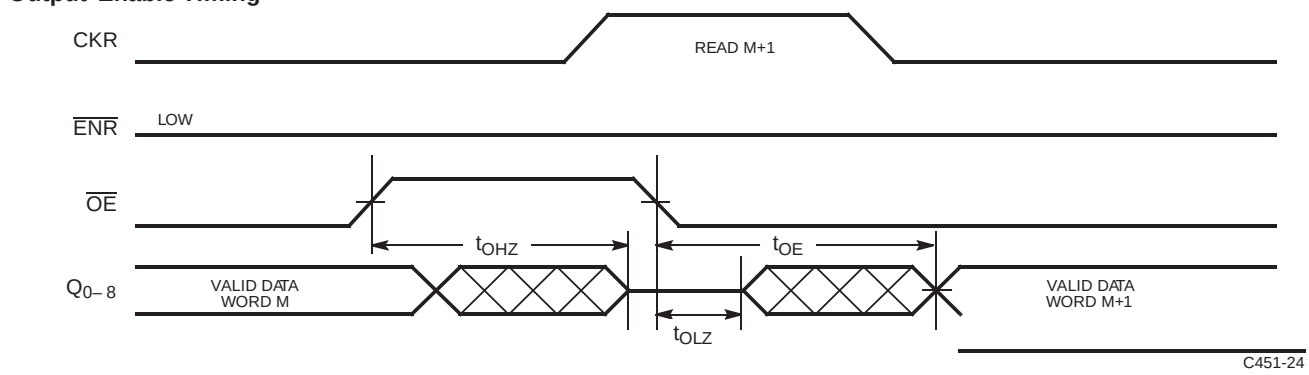
37. In this example, the FIFO is assumed to be programmed to generate even parity.
38. If Q_{0-7} "new word" also has an even number of 1s, then PG stays LOW.
39. If Q_{0-7} "new word" also has an odd number of 1s, then PG stays HIGH.

Switching Waveforms (continued)

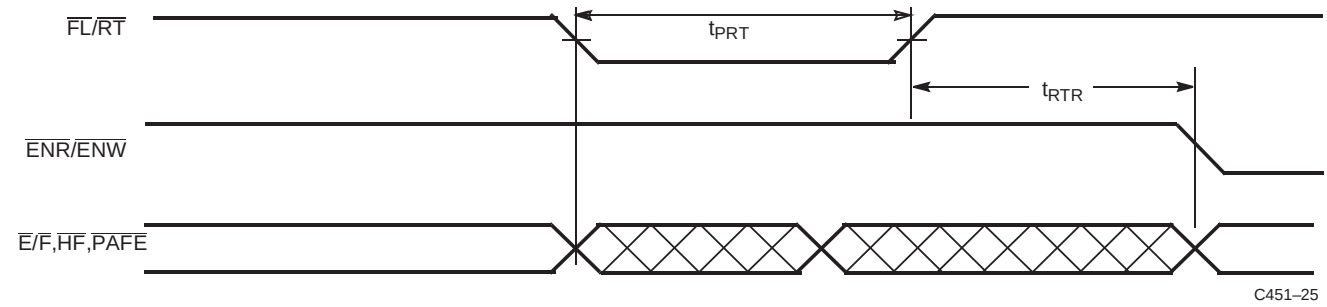
Even Parity Checking [40]



Output Enable Timing [41,42]



Retransmit Timing [43, 44]



Notes:

40. In this example, the FIFO is assumed to be programmed to check for even parity.
41. This example assumes that the time from the CKR rising edge to valid word M+1 ≥ t_A.
42. If ENR was HIGH around the rising edge of CKR (i.e., read disabled), the valid data at the far right would once again be word M instead of word M+1.
43. Clocks are free running in this case.
44. The flags may change state during Retransmit as a result of the offset of the read and write pointers, but flags will be valid at t_{RTR}.

Architecture

The CY7C451, CY7C453, and CY7C454 consist of an array of 512/2048/4096 words of 9 bits each (implemented by an array of dual-port RAM cells), a read pointer, a write pointer, control signals (CKR, CKW, $\overline{ENR}$, $\overline{ENW}$, $\overline{MR}$, $\overline{OE}$, FL/$\overline{RT}$, $\overline{XI}$, $\overline{XO}$), and flags ($\overline{HF}$, E/$\overline{F}$, $\overline{PAFE}$).

Resetting the FIFO

Upon power-up, the FIFO must be reset with a Master Reset ($\overline{MR}$) cycle. This causes the FIFO to enter the Empty condition signified by E/$\overline{F}$ and $\overline{PAFE}$ being LOW and $\overline{HF}$ being HIGH. All data outputs (Q_{0-8}) go low at the rising edge of $\overline{MR}$. In order for the FIFO to reset to its default state, a falling edge must occur on $\overline{MR}$ and the user must not read or write while $\overline{MR}$ is LOW (unless $\overline{ENR}$ and $\overline{ENW}$ are HIGH or unless the device is being programmed). Upon completion of the Master Reset cycle, all data outputs will go LOW t_{AMR} after $\overline{MR}$ is deasserted. All flags are guaranteed to be valid t_{MRF} after $\overline{MR}$ is taken HIGH.

FIFO Operation

When the $\overline{ENW}$ signal is active (LOW), data present on the D_{0-8} pins is written into the FIFO on each rising edge of the CKW signal. Similarly, when the $\overline{ENR}$ signal is active, data in the FIFO memory will be presented on the Q_{0-8} outputs. New data will be presented on each rising edge of CKR while $\overline{ENR}$ is active. $\overline{ENR}$ must be set up t_{SEN} before CKR for it to be a valid read function. $\overline{ENW}$ must occur t_{SEN} before CKW for it to be a valid write function.

An output enable ($\overline{OE}$) pin is provided to tri-state the Q_{0-8} outputs when $\overline{OE}$ is not asserted. When $\overline{OE}$ is enabled, data in the output register will be available to Q_{0-8} outputs after tOE. If devices are cascaded, the $\overline{OE}$ function will only output data on the FIFO that is read enabled.

The FIFO contains overflow circuitry to disallow additional writes when the FIFO is full, and underflow circuitry to disallow additional reads when the FIFO is empty. An empty FIFO maintains the data of the last valid read on its Q_{0-8} outputs even after additional reads occur.

Programming

The CY7C451, CY7C453, and CY7C454 are programmed during a master reset cycle. If $\overline{MR}$ and $\overline{ENW}$ are LOW, a rising edge on CKW will write D_{0-8} inputs into the programming register. $\overline{MR}$ must be set up a minimum of t_{SMRP} before the program write rising edge and held t_{HMRP} after the program write falling edge. The user has the ability to also perform a program read during the master reset cycle. This will occur at the rising edge of CKR when $\overline{MR}$ and $\overline{ENR}$ are asserted. The program read must be performed a minimum of t_{FTP} after a program write, and the program word will be available t_{AP} after the read occurs. If a program write does not occur, a program read may occur a minimum of t_{SMRP} after $\overline{MR}$ is asserted. This will read the default program value.

When free-running clocks are tied to CKW and CKR, programming can still occur during a master reset cycle with the adherence to a few additional timing parameters. The enable pins must be set-up t_{SEN} before the rising edge of CKW or CKR. Hold times of t_{HEN} must also be met for $\overline{ENW}$ and $\overline{ENR}$.

Data present on D_{0-5} during a program write will determine the distance from Empty (Full) that the Almost Empty (Almost Full) flags will become active. See *Table 1* for a description of the six possible FIFO states. P in 1 refers to the decimal equivalent of the binary number represented by D_{0-5}. Programming options for the CY7C451 and CY7C453 are listed in *Table 5*. Programming resolution is 16 words for either device.

The programmable $\overline{PAFE}$ function is only valid when the CY7C451/453/454 are not cascaded. If the user elects not to program the FIFO's flags, the default (P=1) is as follows: Almost Empty condition (Almost Full condition) is activated when the CY7C451/453/454 contain 16 or less words (empty locations).

Parity is programmed with the D_{6-8} bits. See *Table 6* for a summary of the various parity programming options. Data present on D_{6-8} during a program write will determine whether the FIFO will generate or check even/odd parity for the data present on D_{0-8} thereafter. If the user elects not to program the FIFO, the parity function is disabled. Flag operation and parity are described in greater detail in subsequent sections.

Flag Operation

The CY7C451/453/454 provide three status pins when not cascaded. The three pins, E/$\overline{F}$, $\overline{PAFE}$, and $\overline{HF}$, allow decoding of six FIFO states (*Table 1*). $\overline{PAFE}$ is not available when FIFOs are cascaded for depth expansion. All flags are synchronous, meaning that the change of states is relative to one of the clocks (CKR or CKW, as appropriate. See *Figure 1*). The synchronous architecture guarantees some minimum valid time for the flags. The Empty and Almost Empty flag states are exclusively updated by each rising edge of the read clock ($\overline{CKR}$). For example, when the FIFO contains 1 word, the next read (rising edge of CKR while $\overline{ENR}$=LOW) causes the flag pins to output a state that represents Empty. The Half Full, Almost Full, and Full flag states are updated exclusively by the write clock (CKW). For example, if the CY7C453 FIFO contains 2047 words (2048 words indicate Full for the CY7C453), the next write (rising edge of CKW while $\overline{ENW}$=LOW) causes the flag pins to output a state that is decoded as Full.

Table 1. Flag Truth Table[45]

$\overline{E}/\overline{F}$	$\overline{PAFE}$	$\overline{HF}$	State	CY7C451 512 x 9 Number of Words in FIFO	CY7C453 2K x 9 Number of Words in FIFO	CY7C454 4K x 9 Number of Words in FIFO
0	0	1	Empty	0	0	0
1	0	1	Almost Empty	1⇒(16•P)	1 ⇒(16•P)	1 ⇒(16•P)
1	1	1	Less than or Equal to Half Full	(16•P)+1⇒256	(16•P)+1⇒1024	(16•P)+1⇒2048
1	1	0	Greater than Half Full	257⇒511–(16•P)	1025⇒2047–(16•P)	2049 ⇒ 4095–(16•P)
1	0	0	Almost Full	512– (16•P) ⇒ 511	2048–(16•P) ⇒ 2047	4096–(16•P) ⇒4095
0	0	0	Full	512	2048	4096

Note:

45. P is the decimal value of the binary number represented by D_{0-5}. When programming the CY7C451/453/454, P can have values from 0 to 15 for the CY7C451 and values from 0 to 63 for the CY7C453 and CY7C454. See *Table 5* for D_{0-5} representation. P = 0 signifies Almost Empty state = Empty state.

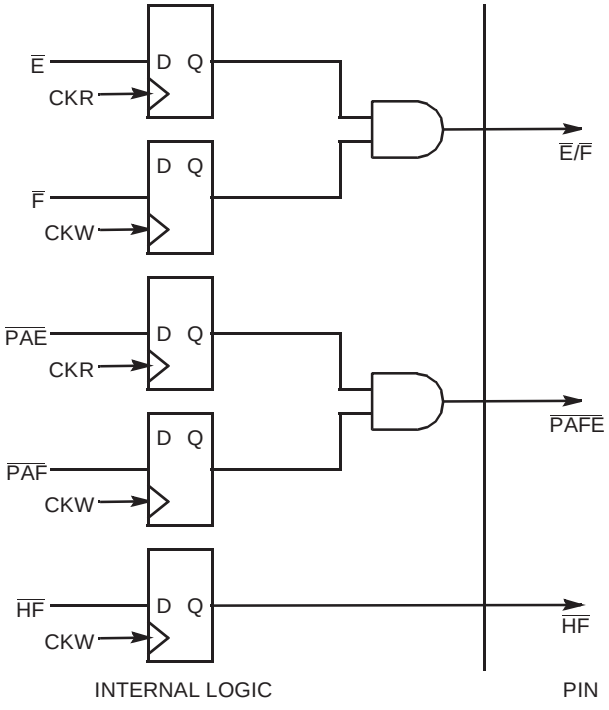


Figure 1. Flag Logic Diagram

Flag Operation (continued)

Since the flags denoting emptiness (Empty, Almost Empty) are only updated by CKR and the flags signifying fullness (Half Full, Almost Full, Full) are exclusively updated by CKW, careful attention must be given to the flag operation. The user must be aware that if a boundary (Empty, Almost Empty, Half Full, Almost Full, or Full) is crossed due to an operation from a clock that the flag is not synchronized to (i.e., CKW does not affect Empty or Almost Empty), a flag update cycle is necessary to represent the FIFO's new state. The signal to which a flag is not synchronized will be referred to as the opposite clock (CKW is opposite clock for Empty and Almost Empty flags; CKR is the opposite clock for Half Full, Almost Full, and Full flags). Until a proper flag update cycle is executed, the synchronous flags will not show the new state of the FIFO.

When updating flags, the CY7C451/453/454 must make a decision as to whether or not the opposite clock was recognized when a clock updates the flag. For example (when updating the Empty flag), if a write occurs at least t_{SKEW1} after a read, the write is guaranteed not to be included when CKR updates the flag. If a write occurs at least t_{SKEW2} before a read, the write is guaranteed to be included when CKR updates flag. If a write occurs within t_{SKEW1}/t_{SKEW2} after or before CKR, then the decision of whether or not to include the write when the flag is updated by CKR is arbitrary.

The update cycle for non-boundary flags (Almost Empty, Half Full, Almost Full) is different from that used to update the boundary flags (Empty, Full). Both operations are described below.

Boundary and Non-Boundary Flags

Boundary Flags (Empty)

The Empty flag is synchronized to the CKR signal (i.e., the Empty flag can only be updated by a clock pulse on the CKR pin). An empty FIFO that is written to will be described with an Empty flag state until a rising edge is presented to the CKR pin. When making the transition from Empty to Almost Empty (or Empty to Less than or Equal to Half Full), a clock cycle on the CKR is necessary to update the flags to the current state. In such a state (flags showing Empty even though data has been written to the FIFO), two read cycles are required to read data out of FIFO. The first read serves only to update the flags to the Almost Empty or Less than or Equal to Half Full state, while the second read outputs the data. This first read cycle is known as the latent or flag update cycle because it does not affect the data in the FIFO or the count (number of words in FIFO). It simply deasserts the Empty flag. The flag is updated regardless of the $\overline{ENR}$ state. Therefore, the update occurs even when $\overline{ENR}$ is unasserted (HIGH), so that a valid read is not necessary to update the flags to correctly describe the FIFO. In this example, the write must occur at least t_{SKEW2} before the flag update cycle in order for the FIFO to guarantee that the write will be included in the count when CKR updates the flags. When a free-running clock is connected to CKR, the flag is updated each cycle. *Table 2* shows an example of a sequence of operations that update the Empty flag.

Boundary Flags (Full)

The Full flag is synchronized to the CKW signal (i.e., the Full flag can only be updated by a clock pulse on the CKW pin). A full FIFO that is read will be described with a Full flag until a rising edge is presented to the CKW pin. When making the transition from Full to Almost Full (or Full to Greater Than Half Full), a clock cycle on the CKW is necessary to update the flags to the current state. In such a state (flags showing Full even through data has been read from the FIFO), two write cycles are required to write data into the FIFO. The first write serves only to update the flags to the Almost Full or Greater Than Half Full state, while the second write inputs the data. This first write cycle is known as the latent or flag update cycle because it does not affect the data in the FIFO or the count (number of words in the FIFO). It simply deasserts the Full flag. The flag is updated regardless of the $\overline{ENW}$ state. Therefore, the update occurs even when $\overline{ENW}$ is deasserted (HIGH), so that a valid write is not necessary to update the flags to correctly describe the FIFO. In this example, the read must occur at least t_{SKEW2} before the flag update cycle in order for the FIFO to guarantee that the read will be included in the count when CKW updates the flags. When a free-running clock is connected to CKW, the flag updates each cycle. Full flag operation is similar to the Empty flag operation described in *Table 2*.

Non-Boundary Flags (Almost Empty, Half Full, Almost Full)

The CY7C451/453/454 feature programmable Almost Empty and Almost Full flags. Each flag can be programmed a specific distance from the corresponding boundary flags (Empty or Full). The flags can be programmed to be activated at the Empty or Full boundary, or at a distance of up to 1008 words/locations for the CY7C453 and CY7C454 (240 words/locations for the CY7C451) from the Empty/Full boundary. The programming resolution is 16 words/locations. When the FIFO contains the number of words or fewer for which the flags have been programmed, the $\overline{PAFE}$ flag will be asserted signifying that the FIFO is Almost Empty. When the FIFO is within that same number of empty locations from being Full, the $\overline{PAFE}$ will also be asserted signifying that the FIFO is Almost Full. The $\overline{HF}$ flag is decoded to distinguish the states.

The default distance (CY7C451/453/454 not programmed) from where $\overline{PAFE}$ becomes active to the boundary (Empty, Full) is 16 words/locations. The Almost Full and Almost Empty flags can be programmed so that they are only active at Full and Empty boundaries. However, the operation will remain consistent with the non-boundary flag operation that is discussed below.

Almost Empty is only updated by CKR while Half Full and Almost Full are updated by CKW. Non-boundary flags employ flag update cycles similar to the boundary flag latent cycles in order to update the FIFO status. For example, if the FIFO just reaches the Greater than Half Full state, and then two words are read from the FIFO, a write clock (CKW) will be required to update the flags to the Less than Half Full state. However, unlike the boundary flag latent cycle, the state of the enable pin ($\overline{ENW}$ in this case) affects the operation. Therefore, set-up and hold times for the enable pins must be met (t_{SEN} and t_{HEN}). If the enable pin is active during the flag update cycle, the count and data are updated in addition to $\overline{PAFE}$ and $\overline{HF}$. If the enable pin is not asserted during the flag update cycle, only the flags are updated. *Table 3* and *Table 4* show an example of a sequence of operations that update the Almost Empty and Almost Full flags.

Programmable Parity

The CY7C451/453/454 also features even or odd parity checking and generation. D_{6-8} are used during a program write to describe the parity option desired. *Table 6* gives a summary of programmable parity options. If the user elects not to program the device, then parity is disabled. Parity information is provided on one multi-mode output pin (Q8/PG/$\overline{PE}$). The three possible modes are described in the following paragraphs. Regardless of the mode selected, the $\overline{OE}$ pin retains three-state control of all 9 Q_{0-8} bits.

Table 2. Empty Flag (Boundary Flag) Operation Example

Status Before Operation						Status After Operation					
Current State of FIFO	$\overline{E}/\overline{F}$	$\overline{AFE}$	$\overline{HF}$	Number of Words in FIFO	Operation	Next State of FIFO	$\overline{E}/\overline{F}$	$\overline{AFE}$	$\overline{HF}$	Number of words in FIFO	Comments
Empty	0	0	1	0	Write ($\overline{ENW}$ = 0)	Empty	0	0	1	1	Write
Empty	0	0	1	1	Write ($\overline{ENW}$ = 0)	Empty	0	0	1	2	Write
Empty	0	0	1	2	Read ($\overline{ENR}$ = X)	AE	1	0	1	2	Flag Update
AE	1	0	1	2	Read ($\overline{ENR}$ = 0)	AE	1	0	1	1	Read
AE	1	0	1	1	Read ($\overline{ENR}$ = 0)	Empty	0	0	1	0	Read (transition from Almost Empty to Empty)
Empty	0	0	1	0	Write ($\overline{ENR}$ = 0)	Empty	0	0	1	1	Write
Empty	1	0	1	1	Read ($\overline{ENR}$ = X)	AE	1	0	1	1	Flag Update
AE	1	0	1	1	Read ($\overline{ENR}$ = 0)	Empty	0	0	1	0	Read (transition from Almost Empty to Empty)

Parity Disabled (Q8 mode)

When parity is disabled (or user does not program parity option) the CY7C451/453/454 stores all 9 bits present on D_{0-8} inputs internally and will output all 9 bits on Q_{0-8} Parity Generate (PG mode)

This mode is used to generate either even or odd parity (as programmed) from D_{0-7}. D8 input is ignored. The parity bit is stored internally as D8 and during a subsequent read will be available on the PG pin along with the data word from which the parity was generated (Q_{0-7}). For example, if parity generate is set to ODD and the D_{0-7} inputs have an EVEN number of 1s, PG will be HIGH.

Parity Check ($\overline{PE}$ mode)

If the CY7C451/453/454 is programmed for parity checking, the FIFO will compare the parity of D_{0-8} with the program register. If the expected parity is present, D8 will be set HIGH internally. When this word is later read, $\overline{PE}$ will be HIGH. If a parity error occurs, D8 will be set LOW internally. When this word is later read, $\overline{PE}$ will be LOW. For example, if parity check is set to odd and D_{0-8} have an even number of 1s, a parity error occurs. When that word is later read, $\overline{PE}$ will be asserted (LOW).

Retransmit

The retransmit feature is beneficial when transferring packets of data. It enables the receipt of data to be acknowledged by the receiver and retransmitted if necessary.

The Retransmit ($\overline{RT}$) input is active in the standalone and width expansion modes. The retransmit feature is intended for use when a number of writes equal to or less than the depth of the FIFO have occurred since the last $\overline{MR}$ cycle. A LOW pulse on $\overline{RT}$ resets the internal read pointer to the first physical location of the FIFO. WCLK and RCLK may be free running but must be disabled during and t_{RTR} after the retransmit pulse. With every valid read cycle after retransmit, previously accessed data is read and the read pointer is incremented until it is equal to the write pointer. Flags are governed by the relative locations of the read and write pointers and are updated during a retransmit cycle. Data written to the FIFO after activation of $\overline{RT}$ are transmitted also.

The full depth of the FIFO can be repeatedly retransmitted.

Width Expansion Modes

During width expansion all flags (programmable and nonprogrammable) are available. The CY7C451/453/454 can be expanded in width to provide word width greater than nine in increments of nine. During width expansion mode all control line inputs are common. When the FIFO is being read near the Empty (Full) boundary, it is important to note that both sets of flags should be checked to see if they have been updated to the Not Empty (Not Full) condition to insure that the next read (write) will perform the same operation on all devices.

Checking all sets of flags is critical so that data is not read from the FIFOs "staggered" by one clock cycle. This situation could occur when the first write to an empty FIFO and a read are very close together. If the read occurs less than t_{SKEW2} after the first write to two width-expanded devices, A and B, device A may go Almost Empty (read recognized as flag update) while device B stays Empty (read ignored). This occurs because a read can be either recognized or ignored if it occurs within t_{SKEW2} of a write. The next read cycle outputs the first half of the first word on device A while device B updates its flags to Almost Empty. Subsequent reads will continue to output "staggered" data assuming more data has been written to the FIFOs.

Depth Expansion Mode

The CY7C451/453/454 can operate up to 83.3 MHz when cascaded. Depth expansion is accomplished by connecting expansion out ($\overline{XO}$) of the first device to expansion in ($\overline{XI}$) of the next device, with $\overline{XO}$ of the last device connected to $\overline{XI}$ of the first device. The first device has its first load pin ($\overline{FL}$) tied to VSS while all other devices must have this pin tied to VCC. The first device will be the first to be write and read enabled after a master reset.

Proper operation also requires that all cascaded devices have common CKW, CKR, $\overline{ENW}$, $\overline{ENR}$, D_{0-8}, Q_{0-8}, and $\overline{MR}$ pins. When cascaded, one device at a time will be read enabled so as to avoid bus contention. By asserting $\overline{XO}$ when appropriate, the currently enabled FIFO alerts the next FIFO that it should be enabled. The next rising edge on CKR puts Q_{0-8} outputs of the first device into a high-impedance state. This occurs regardless of the state of $\overline{ENR}$ or the next FIFO's Empty flag. Therefore, if the next FIFO is empty or undergoing a latent cycle, the Q_{0-8} bus will be in a high-impedance state until the next device receives its first read, which brings its data to the Q_{0-8} bus.

Program Write/Read of Cascaded Devices

Programming of cascaded FIFOs is the same as for a single device. Because the controls of the FIFOs are in parallel when cascaded, they all get programmed the same. During program mode, only parity is programmed since Almost Full and Almost Empty flags are not available when CY7C451/453/454 are cascaded. Only the "first device" (FIFO with $\overline{FL}$=LOW) will output its program register contents on Q_{0-8} during a program read. Q_{0-8} of all other devices will remain in a high-impedance state to avoid bus contention.

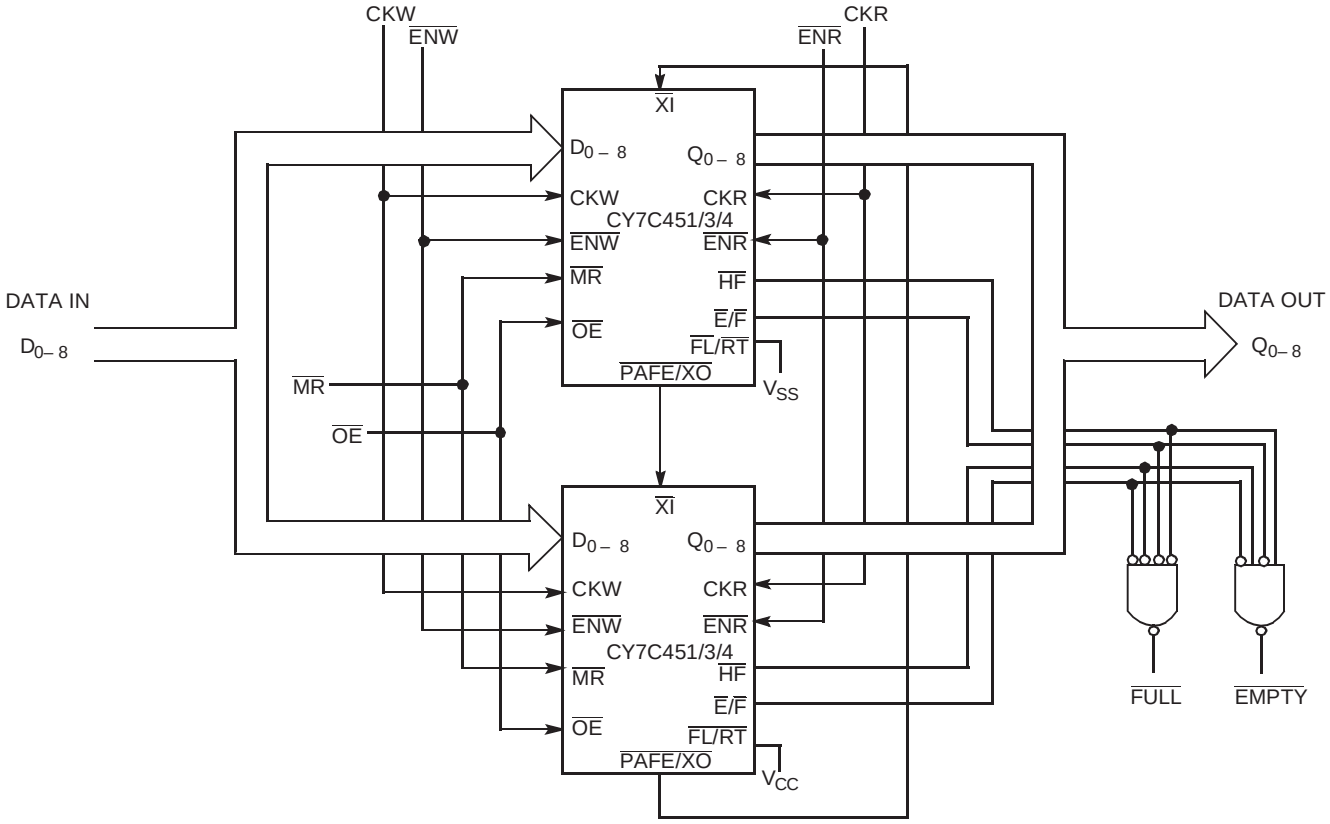


Figure 2. Depth Expansion with CY7C451/3/4

Table 3. Almost Empty Flag (Non-Boundary Flag) Operation Example[46]

Status Before Operation						Status After Operation					
Current State of FIFO	$\overline{E}/\overline{F}$	$\overline{AFE}$	$\overline{HF}$	Number of Words in FIFO	Operation	Next State of FIFO	$\overline{E}/\overline{F}$	$\overline{PAFE}$	$\overline{HF}$	Number of words in FIFO	Comments
AE	1	0	1	32	Write ($\overline{ENW}$ = 0)	AE	1	0	1	33	Write
AE	1	0	1	33	Write ($\overline{ENW}$ = 0)	AE	1	0	1	34	Write
AE	1	0	1	34	Read ($\overline{ENR}$ = 0)	<HF	1	1	1	33	Flag Update and Read
<HF	1	1	1	33	Read ($\overline{ENR}$ = 1)	<HF	1	1	1	33	Ignored Read ($\overline{ENR}$ = 1)
<HF	1	1	1	33	Read ($\overline{ENR}$ = 0)	AE	1	0	1	32	Read (Transition from <HF to AE)

Note:
46. Applies to both CY7C451, CY7C453, and CY7C454 operations when devices are programmed so that Almost Empty becomes active when the FIFO contains 32 or fewer words.

Table 4. Almost Full Flag Operation Example[47]

Operation		State of FIFO	$\overline{E}/\overline{F}$	$\overline{PAFE}$	$\overline{HF}$	Number of Words in FIFO CY7C451	Number of Words in FIFO CY7C453	Number of Words in FIFO CY7C454	Comments
Read ($\overline{ENR}$=0)	Current	AF	1	0	0	496	2032	4080	Read
	Next	AF	1	0	0	495	2031	4079	
Read ($\overline{ENR}$=0)	Current	AF	1	0	0	495	2031	4079	Read
	Next	AF	1	0	0	494	2030	4078	
Write ($\overline{ENW}$=1)	Current	AF	1	0	0	494	2030	4078	Flag Update
	Next	AF	1	1	0	494	2030	4078	
Write ($\overline{ENW}$=0)	Current	>HF	1	1	0	494	2030	4078	Write
	Next	>HF	1	1	0	495	2031	4079	
Write ($\overline{ENW}$ =0)	Current	>HF	1	1	0	495	2031	4079	Write (Transition from >HF to AF)
	Next	>HF	1	0	0	496	2032	4080	

Table 5. Programmable Almost Full/Almost Empty Options - CY7C451/CY7C453/CY7C454[48]

D5	D4	D3	D2	D1	D0	PAFE Active when CY7C451/453/454 is:	P[49]
0	0	0	0	0	0	Completely Full and Empty.	0
0	0	0	0	0	1	16 or less locations from Empty/Full (default)	1
0	0	0	0	1	0	32 or less locations from Empty/Full	2
0	0	0	0	1	1	48 or less locations from Empty/Full	3
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
0	0	1	1	1	0	224 or less locations from Empty/Full	14
0	0	1	1	1	1	240 or less locations from Empty/Full	15
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	0	992 or less locations from Empty/Full	62
1	1	1	1	1	1	1008 or less locations from Empty/Full	63

Table 6. Programmable Parity Options

D8	D7	D6	Condition
0	X	X	Parity disabled.
1	0	0	Generate even parity on PG output pin.
1	0	1	Generate odd parity on PG output pin.
1	1	0	Check for even parity. Indicate error on $\overline{PE}$ output pin.
1	1	1	Check for odd parity. Indicate error on $\overline{PE}$ output pin.

Notes:
47. Programmed so that Almost Full becomes active when the FIFO contains 16 or less empty locations.
48. D4 and D5 are don't care for CY7C451.
49. Referenced in *Table 1.*

Ordering Information

512x9 Clocked FIFO

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C451-12JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C451-12JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
14	CY7C451-14JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C451-14JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
20	CY7C451-20JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C451-20JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
30	CY7C451-30JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C451-30JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial

2Kx9 Clocked FIFO

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C453-12JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C453-12JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
14	CY7C453-14JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C453-14JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
20	CY7C453-20JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C453-20JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
30	CY7C453-30JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C453-30JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial

4Kx9 Clocked FIFO

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C454-12JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C454-12JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
14	CY7C454-14JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C454-14JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
20	CY7C454-20JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C454-20JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
30	CY7C454-30JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C454-30JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial

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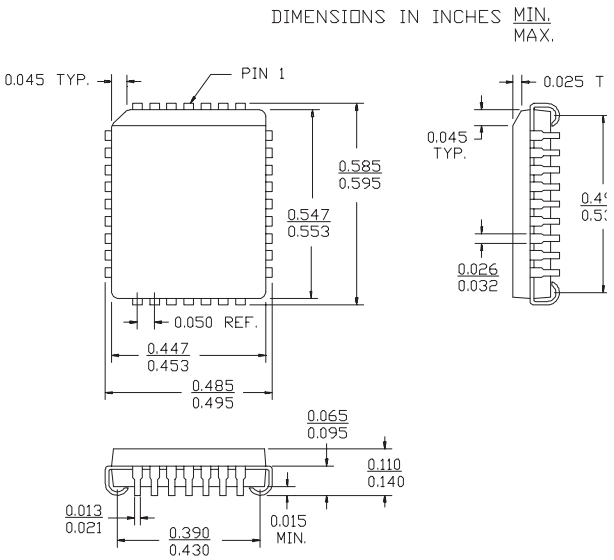
Package Diagram

32-Lead Plastic Leaded Chip Carrier J65



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