CY2267

Pentium®, Pentium® Pro, and Cyrix® 6x86 Compatible Clock Synthesizer/Driver

Features

- Complete clock solution to meet requirements of Pentium®, Pentium® Pro, or Cyrix® 6x86 motherboards including dual-processor and SDRAM designs
  - — Sixteen CPU clock outputs, up to 66.66 MHz (see Function Table)
  - — One synchronous PCI clock output
  - — One USB clock at 48 MHz, meets Intel's accuracy, jitter, as well as rise and fall time requirements
  - — One I/O clock at 24 MHz
  - — One Ref. clock at 14.318 MHz
- Two dedicated, independent Frequency Select inputs (internal pull-up) ease system design, enable in-system frequency changes, and support OE control
- Low CPU clock jitter ≤ 200 ps cycle-to-cycle
- Low skew outputs
  - — ≤ 250 ps between CPU clocks
  - — 1ns–3ns skew between CPU and PCI clocks for compatibility with SiS 55XX as well as Intel 82430TX, 82430HX, and 82430VX chipsets (CY2267–1)
- Improved output drivers are designed for low EMI
- Meets Pentium and Pentium Pro power-up stabilization requirements
- 3.3V operation, 5V tolerant inputs
- Available in space-saving 34-pin SSOP package

Functional Description

The CY2267 is a low-cost Clock Synthesizer/Driver chip for a Pentium, Pentium Pro, or Cyrix 6x86-based motherboard.

The CY2267 outputs sixteen CPU clocks, twelve of which can be used to support up to three SDRAM modules. The PCI clock output can be buffered with an external, low-cost Zero Delay Buffer (CY2305/9), thus providing a complete solution for 82430TX desktop systems.

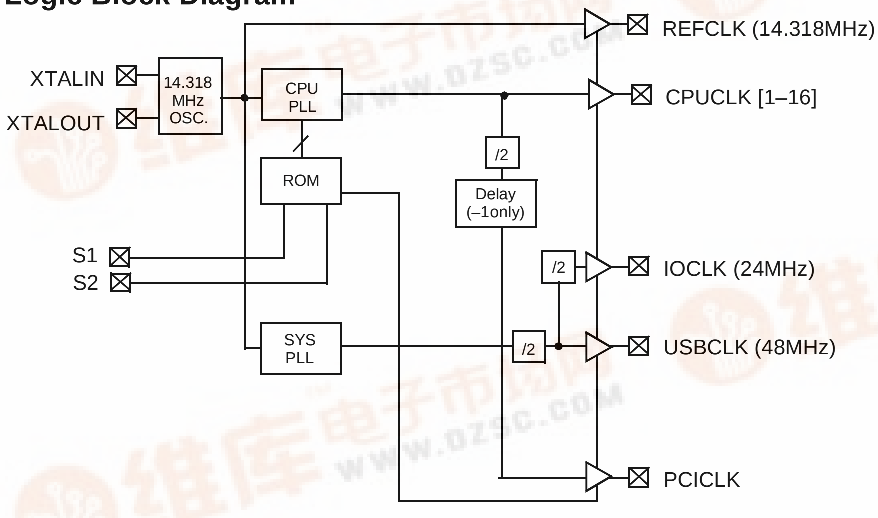
The CPU clocks of the CY2267 have less than 200 ps cycle-to-cycle jitter. Both the CPU and PCI clocks have a slew rate of greater than 1V/ns. The USB clock meets Intel's accuracy, jitter, and rise and fall time requirements.

All CPU clocks support fast clock stabilization on power-up (< 2 ms). Additionally, two dedicated Frequency Select inputs are used for Output Enable control and setting the CPU clock output frequencies.

The CY2267 clock outputs are designed for low EMI emissions. Controlled rise and fall times, unique output driver circuits, and innovative circuit layout techniques enable the CY2267 to have lower EMI than clock devices from other manufacturers. Please refer to the application note "Layout and Termination Techniques for Cypress Clock Generators" for more information on recommended system layout techniques.

The CY2267 accepts a 14.318 MHz reference crystal or clock as its input and runs off a 3.3V supply. The CY2267 is available in a space-saving, low-cost 34-pin SSOP package and is pin-compatible with the CY2264 and CY2265.

Logic Block Diagram



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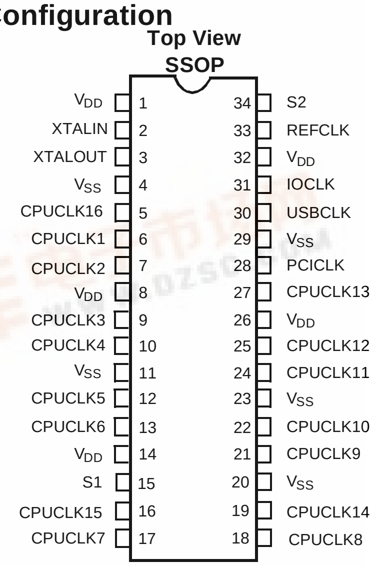
Pin Configuration



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Pin Summary

Name	Pin	Description
V_{DD}	1	Voltage supply
XTALIN[1]	2	Reference crystal input
XTALOUT[1]	3	Reference crystal feedback
V_{SS}	4	Ground
CPUCLK16	5	CPU clock output
CPUCLK1	6	CPU clock output
CPUCLK2	7	CPU clock output
V_{DD}	8	Voltage supply
CPUCLK3	9	CPU clock output
CPUCLK4	10	CPU clock output
V_{SS}	11	Ground
CPUCLK5	12	CPU clock output
CPUCLK6	13	CPU clock output
V_{DD}	14	Voltage supply
S1	15	CPU clock select input, bit 1 (internal pull-up resistor to V_{DD})
CPUCLK15	16	CPU clock output
CPUCLK7	17	CPU clock output
CPUCLK8	18	CPU clock output
CPUCLK14	19	CPU clock output
V_{SS}	20	Ground
CPUCLK9	21	CPU clock output
CPUCLK10	22	CPU clock output
V_{SS}	23	Ground
CPUCLK11	24	CPU clock output
CPUCLK12	25	CPU clock output
V_{DD}	26	Voltage supply
CPUCLK13	27	CPU clock output
PCICLK	28	PCI clock output
V_{SS}	29	Ground
USBCLK	30	USB clock output, 48 MHz
IOCLK	31	I/O clock output, 24 MHz
V_{DD}	32	Voltage supply
REFCLK	33	Reference clock output (14.318 MHz) for ISA slots (drives C_{LOAD} = 45 pF)
S2	34	CPU clock select input, bit 2 (internal pull-up resistor to V_{DD})

Notes:

1. For best accuracy, use a parallel-resonant crystal, C_{LOAD} = 17 pF.

Function Table

S2	S1	XTALIN	CPUCLK[1-16]	PCICLK	REFCLK	USBCLK	IOCLK
0	0	14.318 MHz	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
0	1	14.318 MHz	66.67 MHz	33.33 MHz	14.318 MHz	48 MHz	24 MHz
1	0	14.318 MHz	50.0 MHz	25.0 MHz	14.318 MHz	48 MHz	24 MHz
1	1	14.318 MHz	60.0 MHz	30.0 MHz	14.318 MHz	48 MHz	24 MHz

Actual Clock Frequency Values

Clock Output	Target Frequency (MHz)	Actual Frequency (MHz)	PPM
CPUCLK	50.0	49.93	–1399
CPUCLK	66.67	66.56	–1597
CPUCLK	60.0	60.0	0
USBCLK[2]	48.0	48.008	167
IOCLK	24.0	24.004	167

Notes:

2. Meets Intel USB clock requirements.

CPU and PCI Clock Driver Strengths

- Matched impedances on both rising and falling edges on the output drivers
- Output impedance: 25Ω (typical) measured at 1.5V.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage .... –0.5 to +7.0V

Input Voltage ....–0.5V to V_{DD}+0.5

Storage Temperature (Non-Condensing)... –65°C to +150°C

Max. Soldering Temperature (10 sec)...................... +260°C

Junction Temperature .... +150°C

Package Power Dissipation... 1W

Static Discharge Voltage .... >2000V
(per MIL-STD-883, Method 3015)

Operating Conditions[3]

Parameter	Description	Min.	Max.	Unit
V_{DD}	Supply Voltage	3.135	3.6	V
T_A	Operating Temperature, Ambient	0	70	°C
C_L	Max. Capacitive Load on CPUCLK PCICLK USBCLK IOCLK REFCLK		 30 30 20 20 45	pF
$f_{(REF)}$	Reference Frequency, Oscillator Nominal Value	14.318	14.318	MHz

Note:

3. Electrical parameters are guaranteed with these operating conditions.

Electrical Characteristics V_{DD} = 3.135V to 3.6V, T_A = 0°C to +70°C

Parameter	Description	Test Conditions			Min.	Max.	Unit
V_{IH}	High-level Input Voltage	Except Crystal Inputs			2.0		V
V_{IL}	Low-level Input Voltage	Except Crystal Inputs				0.8	V
V_{OH}	High-level Output Voltage	V_{DD} = V_{DD} Min.	I_{OH} = 12 mA	CPUCLK	2.4		V
			I_{OH} = 12 mA	PCICLK			
			I_{OH} = 8 mA	USBCLK			
			I_{OH} = 8 mA	IOCLK			
			I_{OH} = 12 mA	REFCLK			
V_{OL}	Low-level Output Voltage	V_{DD} = V_{DD} Min.	I_{OL} = 12 mA	CPUCLK		0.4	V
			I_{OL} = 12 mA	PCICLK			
			I_{OL} = 8 mA	USBCLK			
			I_{OL} = 8 mA	IOCLK			
			I_{OL} = 12 mA	REFCLK			
I_{IH}	Input High Current	V_{IH} = V_{DD}				10	µA
I_{IL}	Input Low Current	V_{IL} = 0V				100	µA
I_{OZ}	Output Leakage Current	Three-state			–10	+10	µA
I_{DD}	Power Supply Current	V_{DD} = 3.6V, V_{IN} = 0 or V_{DD}, Loaded Outputs, CPU clocks = 66.67 MHz				180	mA
I_{DD}	Power Supply Current	V_{DD} = 3.6V, V_{IN} = 0 or V_{DD}, Unloaded Outputs				120	mA

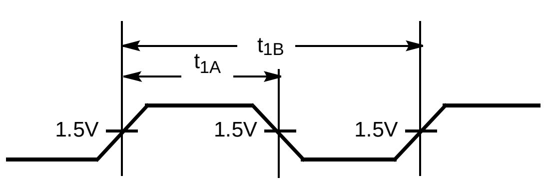
Switching Characteristics[4]

Parameter	Output	Description	Test Conditions	Min.	Typ.	Max.	Unit
t_1	All	Output Duty Cycle[5]	$t_1 = t_{1A} \div t_{1B}$	45	50	55	%
t_{1C}	CPUCLK	CPU Clock HIGH Time	Measured at 2.4V, 66.67 MHz	5.0			ns
t_{1C}	PCICLK	PCI Clock HIGH Time[6]	Measured at 2.4V, 33.33 MHz	12.0			ns
t_{1D}	CPUCLK	CPU Clock LOW Time	Measured at 0.4V, 66.67 MHz	5.0			ns
t_{1D}	PCICLK	PCI Clock LOW Time[6]	Measured at 0.4V, 33.33 MHz	12.0			ns
t_2	CPUCLK	CPU Clock Rising and Falling Edge Rate	Measured between 0.8V and 2.0V	1.0		4.0	V/ns
t_2	PCICLK	PCI Clock Rising and Falling Edge Rate	Measured between 0.8V and 2.0V	1.0		4.0	V/ns
t_2	REFCLK	Reference Clock Rising and Falling Edge Rate	Measured between 0.8V and 2.0V	0.5			V/ns
t_3	CPUCLK	CPU Clock Rise Time	Measured between 0.8V and 2.0V	0.3		1.2	ns
t_3	USBCLK, IOCLK	USB Clock and I/O Clock Rise Time	Measured between 0.8V and 2.0V			1.2	ns
t_4	CPUCLK	CPU Clock Fall Time	Measured between 2.0V and 0.8V	0.3		1.2	ns
t_4	USBCLK, IOCLK	USB Clock and I/O Clock Fall Time	Measured between 2.0V and 0.8V			1.2	ns
t_5	CPUCLK	CPU-CPU Clock Skew	Measured at 1.5V		100	250	ps
t_6	CPUCLK, PCICLK	CPU-PCI Clock Skew (CY2267–1)	Measured at 1.5V	1.0	2.0	3.0	ns
t_7	CPUCLK	Cycle-Cycle Clock Jitter	CPU Clock jitter			200	ps
t_7	USBCLK, IOCLK, PCICLK	Cycle-Cycle Clock Jitter	USB Clock, I/O Clock, and PCI Clock jitter			500	ps
t_8	CPUCLK	Power-up Time	CPU clock stabilization from power-up			2	ms
t_8	PCICLK	Power-up Time	PCI clock stabilization from power-up			2	ms

Notes:
4. All parameters specified with loaded outputs.
5. Duty cycle is measured at 1.5V.
6. A LOW and HIGH time of 12 ns corresponds to a PCICLK frequency of 33.33 MHz. For PCICLK frequencies of 30 MHz and 25 MHz, the LOW and HIGH times are each respectively 13.33 ns and 16 ns.

Switching Waveforms

Duty Cycle Timing



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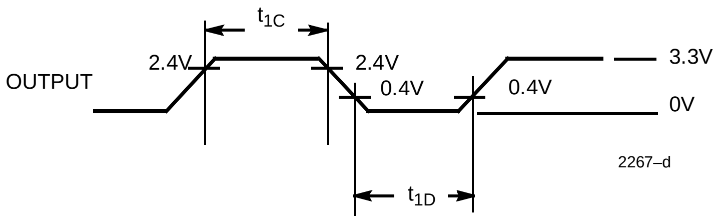
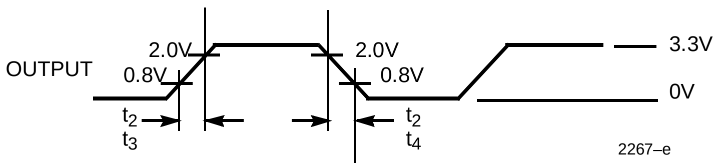
Switching Waveforms (continued)

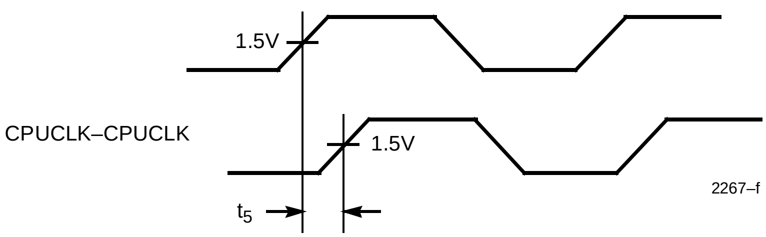
CPUCLK Outputs HIGH/LOW Time



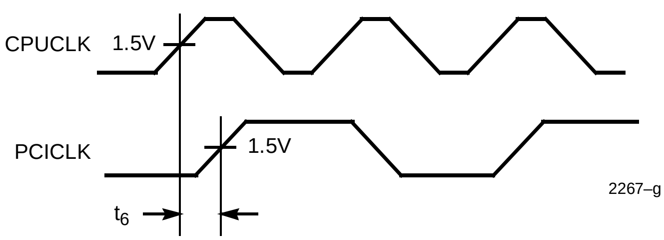
All Outputs Rise/Fall Time



Clock Skew



CPU-PCI Clock Skew

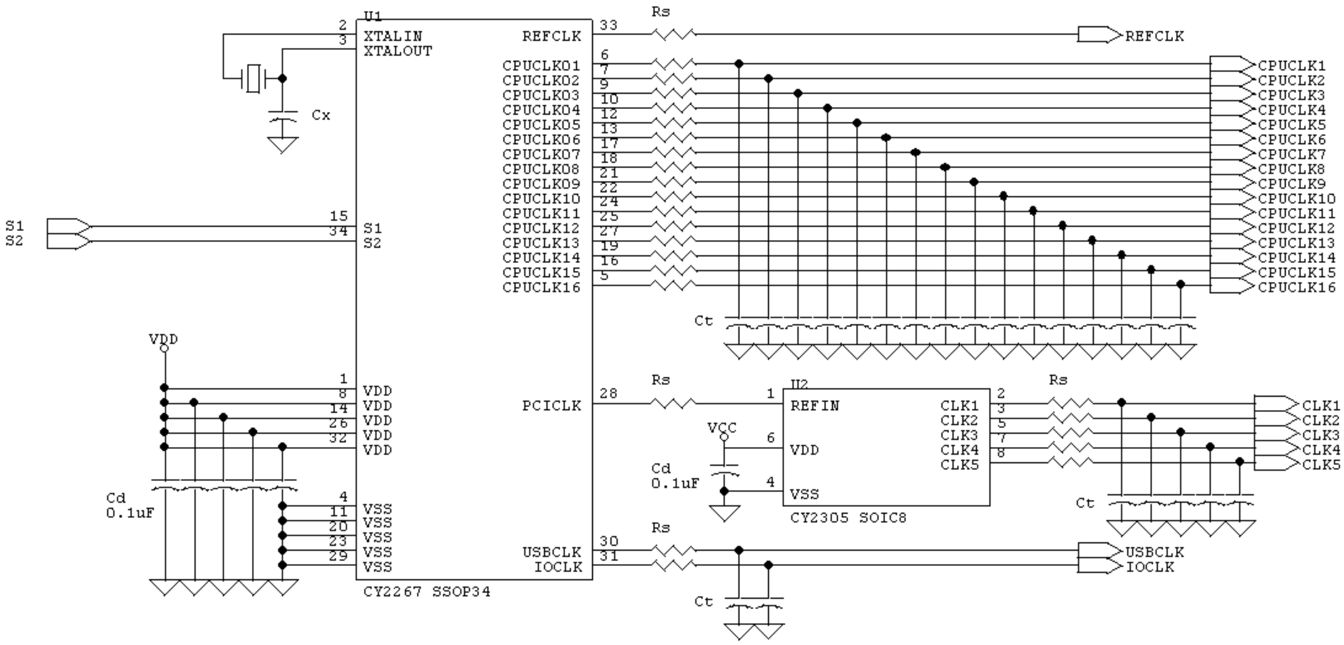


Application Information

Clock traces must be terminated with either series or parallel termination, as they are normally done.

The Application Circuit is shown below.

Application Circuit



Cd = DECOUPLING CAPACITORS

Ct = OPTIONAL EMI-REDUCING CAPACITORS

Cx = OPTIONAL LOAD MATCHING CAPACITOR

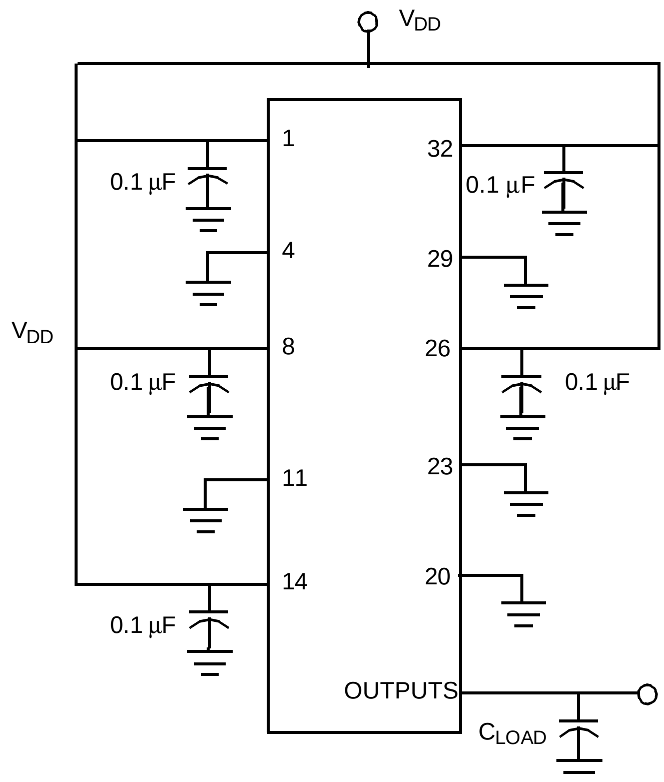
Rs = SERIES TERMINATING RESISTORS

Summary

- A parallel-resonant crystal should be used as the reference to the clock generator. The operating frequency and C_{LOAD} of this crystal should be as specified in the data sheet. Optional trimming capacitors may be needed if a crystal with a different C_{LOAD} is used. Footprints must be laid out for flexibility.
- Surface mount, low-ESR, ceramic capacitors should be used for filtering. Typically, these capacitors have a value of 0.1 µF. In some cases, smaller value capacitors may be required.
- The value of the series terminating resistor satisfies the following equation, where R_{trace} is the loaded characteristic impedance of the trace, R_{out} is the output impedance of the clock generator (specified in the data sheet), and R_{series} is the series terminating resistor.

  $$R_{series} \geq R_{trace} - R_{out}$$
- Footprints must be laid out for optional EMI-reducing capacitors, which should be placed as close to the terminating resistor as is physically possible. Typical values of these capacitors range from 4.7 pF to 22 pF.
- A Ferrite Bead **may** be used to isolate the Board V_{DD} from the clock generator V_{DD} island. Ensure that the Ferrite Bead offers greater than 50Ω impedance at the clock frequency, under loaded DC conditions. Please refer to the application note “Layout and Termination Techniques for Cypress Clock Generators” for more details.
- If a Ferrite Bead is used, a 10 µF– 22 µF tantalum bypass capacitor should be placed close to the Ferrite Bead. This capacitor prevents power supply droop during current surges.

Test Circuit



Note: All capacitors should be placed as close to each pin as possible.

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
CY2267PVC–1	O34	34-Pin SSOP	Commercial

Document #: 38–00534–A

Package Diagram

34-Pin Shrunk Small Outline Package O34