



CY62136V MoBL™ CY62136V18 MoBL2™

128K x 16 Static RAM

Features

- **Low voltage range:**
 - CY62136V18: 1.65V–1.95V
 - CY62136V: 2.7V–3.6V
- **Ultra-low active, standby power**
- **Easy memory expansion with \overline{CE} and \overline{OE} features**
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**

Functional Description

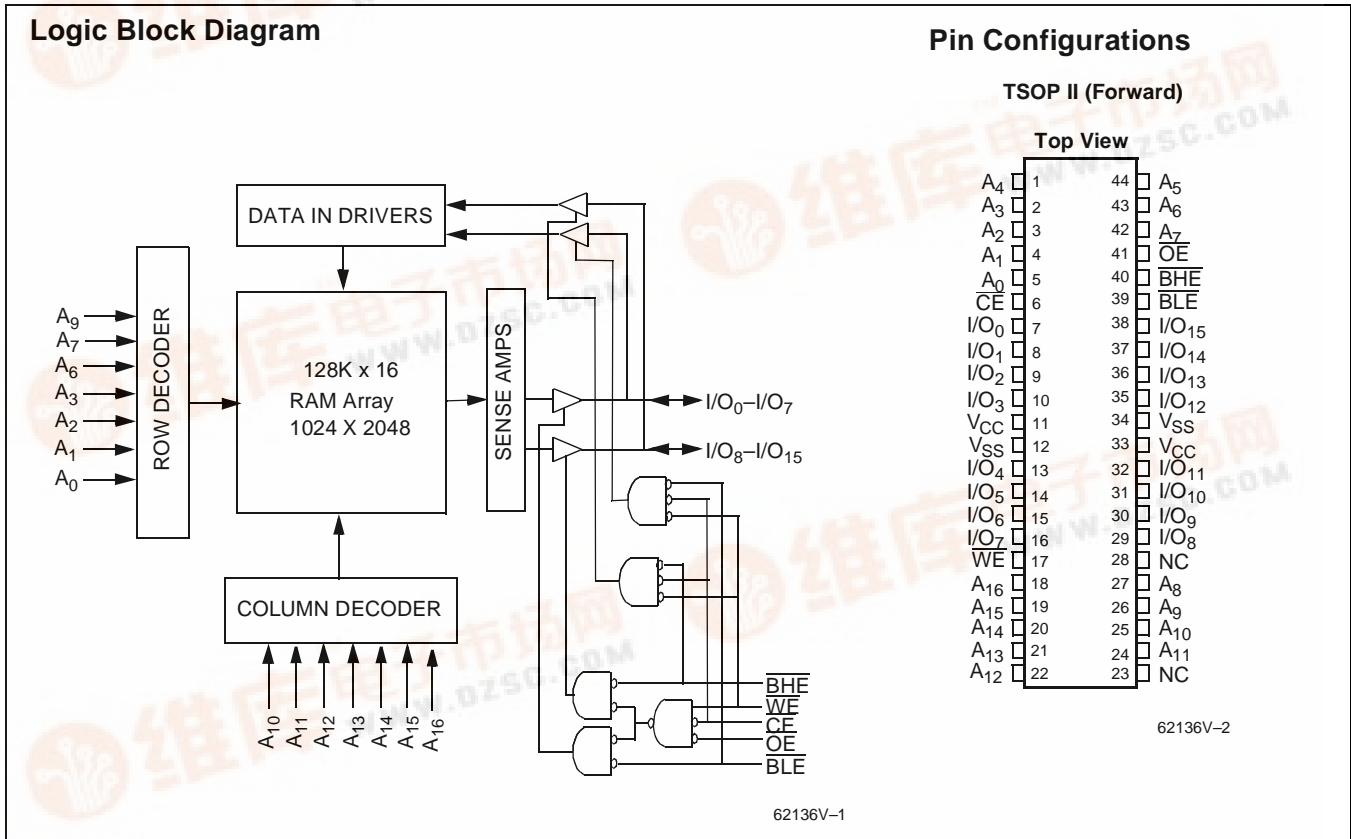
The CY62136V and CY62136V18 are high-performance CMOS static RAMs organized as 131,072 words by 16 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL™) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption by 99% when addresses are not toggling. The device can also be put into standby mode when deselected (CE HIGH). The in-

put/output pins (I/O₀ through I/O₁₅) are placed in a high-impedance state when: deselected (\overline{CE} HIGH), outputs are disabled (\overline{OE} HIGH), BHE and BLE are disabled (BHE, BLE HIGH), or during a write operation (\overline{CE} LOW, and \overline{WE} LOW).

Writing to the device is accomplished by taking Chip Enable (\overline{CE}) and Write Enable (\overline{WE}) inputs LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O₀ through I/O₇), is written into the location specified on the address pins (A₀ through A₁₆). If Byte High Enable (BHE) is LOW, then data from I/O pins (I/O₈ through I/O₁₅) is written into the location specified on the address pins (A₀ through A₁₆).

Reading from the device is accomplished by taking Chip Enable (\overline{CE}) and Output Enable (\overline{OE}) LOW while forcing the Write Enable (\overline{WE}) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins will appear on I/O₀ to I/O₇. If Byte High Enable (BHE) is LOW, then data from memory will appear on I/O₈ to I/O₁₅. See the Truth Table at the back of this data sheet for a complete description of read and write modes.

The CY62136V and CY62136V18 are available in 48-ball FBGA and standard 44-pin TSOP Type II (forward pinout) packaging.

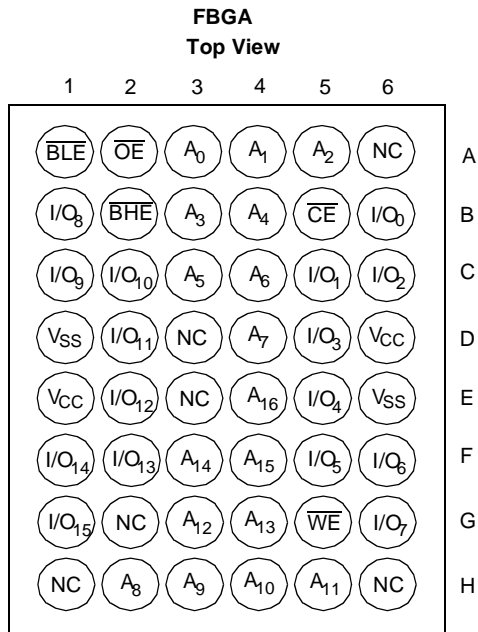


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Pin Configuration (continued)



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Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C
 Ambient Temperature with Power Applied -55°C to +125°C
 Supply Voltage to Ground Potential -0.5V to +4.6V

DC Voltage Applied to Outputs

in High Z State^[1] -0.5V to V_{CC} + 0.5V
 DC Input Voltage^[1] -0.5V to V_{CC} + 0.5V
 Output Current into Outputs (LOW) 20 mA
 Static Discharge Voltage >2001V (per MIL-STD-883, Method 3015)
 Latch-Up Current >200 mA

Operating Range

Device	Range	Ambient Temperature	V _{CC}
CY62136V18	Industrial	-40°C to +85°C	1.65V to 1.95V
CY62136V	Industrial	-40°C to +85°C	2.7V to 3.6V

Product Portfolio

Product	V _{CC} Range			Speed	Power Dissipation (Industrial)			
	V _{CC(min)}	V _{CC(typ)} ^[2]	V _{CC(max)}		Operating (I _{CC})		Standby (I _{SB2})	
					Typ. ^[2]	Maximum	Typ. ^[2]	Maximum
CY62136V	2.7V	3.0V	3.6V	70 ns	7 mA	15 mA	1 µA	15 µA
CY62136V18	1.65	1.80	1.95	70 ns	3 mA	7 mA	1 µA	15 µA

Shaded areas contain preliminary information.

Notes:

- V_{IL} (min) = -2.0V for pulse durations less than 20 ns.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC} Typ, T_A = 25°C.



Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		CY62136V			Unit
				Min.	Typ. ^[2]	Max.	
V _{OH}	Output HIGH Voltage	I _{OH} = -1.0 mA	V _{CC} = 2.7V	2.4			V
V _{OL}	Output LOW Voltage	I _{OL} = 2.1 mA	V _{CC} = 2.7V			0.4	V
V _{IH}	Input HIGH Voltage		V _{CC} = 3.6V	2.2		V _{CC} + 0.5V	V
V _{IL}	Input LOW Voltage		V _{CC} = 2.7V	-0.5		0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}		-1	±1	+1	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled		-1	+1	+1	μA
I _{CC}	V _{CC} Operating Supply Current	I _{OUT} = 0 mA, f = f _{MAX} = 1/t _{RC} , CMOS levels	V _{CC} = 3.6V		7	15	mA
		I _{OUT} = 0 mA, f = 1 MHz, CMOS Levels			1	2	mA
I _{SB1}	Automatic CE Power-Down Current—CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.3V$, V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V, f = f _{MAX}				100	μA
I _{SB2}	Automatic CE Power-Down Current—CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.3V$ V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V, f = 0	V _{CC} = 3.6V	LL	1	15	μA

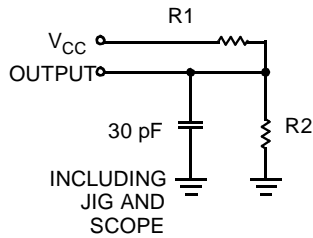
Parameter	Description	Test Conditions		CY62136V18			Unit
				Min.	Typ. ^[2]	Max.	
V _{OH}	Output HIGH Voltage	I _{OH} = -0.1 mA	V _{CC} = 1.65V	1.5			V
V _{OL}	Output LOW Voltage	I _{OL} = 0.1 mA	V _{CC} = 1.65V			0.2	V
V _{IH}	Input HIGH Voltage		V _{CC} = 1.95V	1.4		V _{CC} + 0.3V	V
V _{IL}	Input LOW Voltage		V _{CC} = 1.65V	-0.5		0.4	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}		-1	±1	+1	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled		-1	+1	+1	μA
I _{CC}	V _{CC} Operating Supply Current	I _{OUT} = 0 mA, f = f _{MAX} = 1/t _{RC} , CMOS levels	V _{CC} = 1.95V		3	7	mA
		I _{OUT} = 0 mA, f = 1 MHz, CMOS Levels			1	2	mA
I _{SB1}	Automatic CE Power-Down Current—CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.3V$, V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V, f = f _{MAX}				100	μA
I _{SB2}	Automatic CE Power-Down Current—CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.3V$ V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V, f = 0	V _{CC} = 1.95V	LL	1	15	μA

Capacitance^[3]

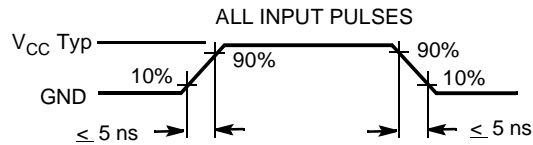
Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = V _{CC} (typ)	6	pF
C _{OUT}	Output Capacitance		8	pF

Note:

3. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms


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62136V-5

Equivalent to: THÉVENIN EQUIVALENT

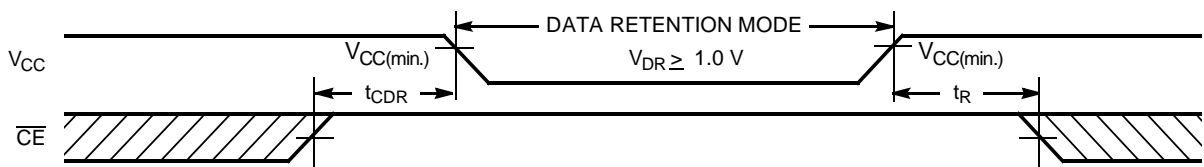


Parameters	3.0V	1.8V	UNIT
R1	1105	15294	Ohms
R2	1550	11300	Ohms
R _{TH}	645	6500	Ohms
V _{TH}	1.75V	0.85V	Volts

Shaded areas contain preliminary information.

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions ^[5]	Min.	Typ. ^[2]	Max.	Unit
V _{DR}	V _{CC} for Data Retention (CY62136V18)		1.0		1.95	V
V _{DR}	V _{CC} for Data Retention (CY62136V)		1.0		3.6	V
I _{CCDR}	Data Retention Current	V _{CC} = 1.0V CE ≥ V _{CC} - 0.3V, V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V No input may exceed V _{CC} +0.3V	LL	0.1	5	μA
t _{CDR} ^[3]	Chip Deselect to Data Retention Time		0			ns
t _R ^[4]	Operation Recovery Time		100			μs

Data Retention Waveform


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Notes:

- Full device operation requires linear V_{CC} ramp from V_{DR} to V_{CC(min)} ≥ 100 μs or stable at V_{CC(min)} ≥ 100 μs.
- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to V_{CC} typ., and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.

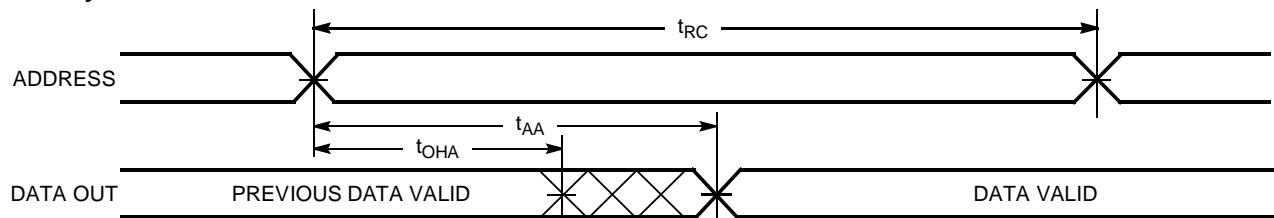


Switching Characteristics Over the Operating Range^[5]

Parameter	Description	70 ns		Unit
		Min.	Max.	
READ CYCLE				
t _{RC}	Read Cycle Time	70		ns
t _{AA}	Address to Data Valid		70	ns
t _{OHA}	Data Hold from Address Change	10		ns
t _{ACE}	\overline{CE} LOW to Data Valid		70	ns
t _{DOE}	\overline{OE} LOW to Data Valid		35	ns
t _{LZOE}	\overline{OE} LOW to Low Z ^[6]	5		ns
t _{HZOE}	\overline{OE} HIGH to High Z ^[6, 7]		25	ns
t _{LZCE}	\overline{CE} LOW to Low Z ^[6]	10		ns
t _{HZCE}	\overline{CE} HIGH to High Z ^[6, 7]		25	ns
t _{PU}	\overline{CE} LOW to Power-Up	0		ns
t _{PD}	\overline{CE} HIGH to Power-Down		70	ns
t _{DBE}	$\overline{BLE} / \overline{BHE}$ LOW to Data Valid		35	ns
t _{LZBE}	$\overline{BLE} / \overline{BHE}$ LOW to Low Z ^[6, 7]	5		ns
t _{HZBE}	$\overline{BLE} / \overline{BHE}$ HIGH to High Z ^[8]		25	ns
WRITE CYCLE^[8, 9]				
t _{WC}	Write Cycle Time	70		ns
t _{SCE}	\overline{CE} LOW to Write End	60		ns
t _{AW}	Address Set-Up to Write End	60		ns
t _{HA}	Address Hold from Write End	0		ns
t _{SA}	Address Set-Up to Write Start	0		ns
t _{PWE}	\overline{WE} Pulse Width	50		ns
t _{BW}	$\overline{BLE} / \overline{BHE}$ LOW to Write End	60		ns
t _{SD}	Data Set-Up to Write End	30		ns
t _{HD}	Data Hold from Write End	0		ns
t _{HZWE}	\overline{WE} LOW to High Z ^[6, 7]		25	ns
t _{LZWE}	\overline{WE} HIGH to Low Z ^[6]	10		ns

Switching Waveforms

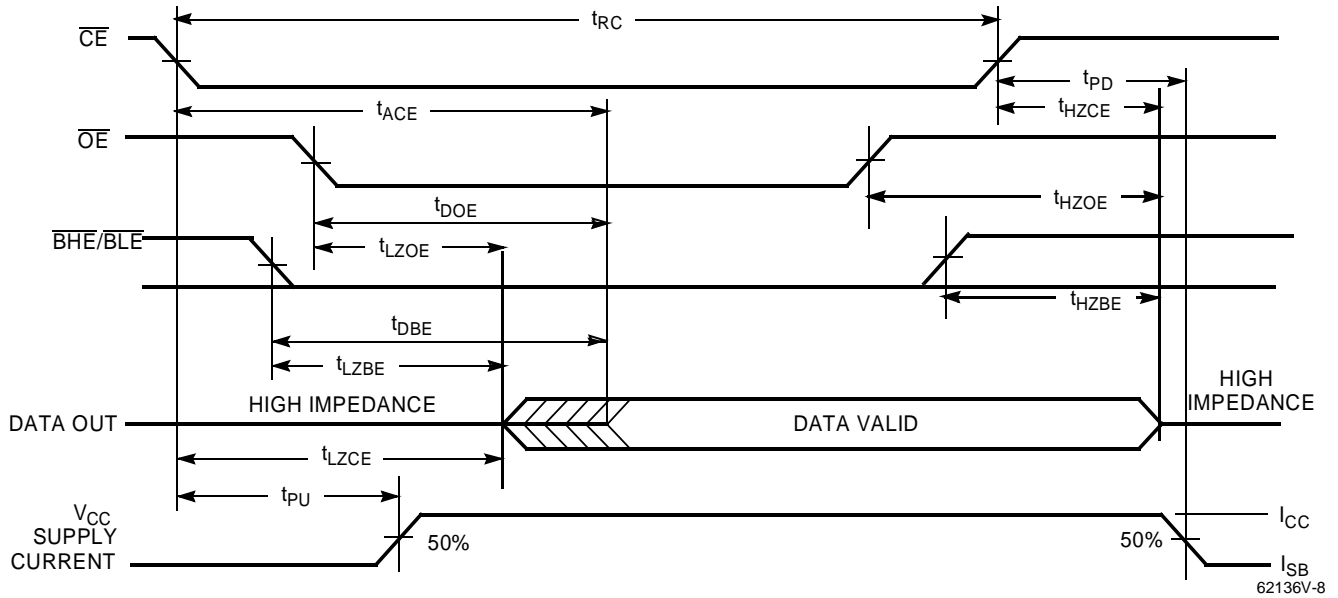
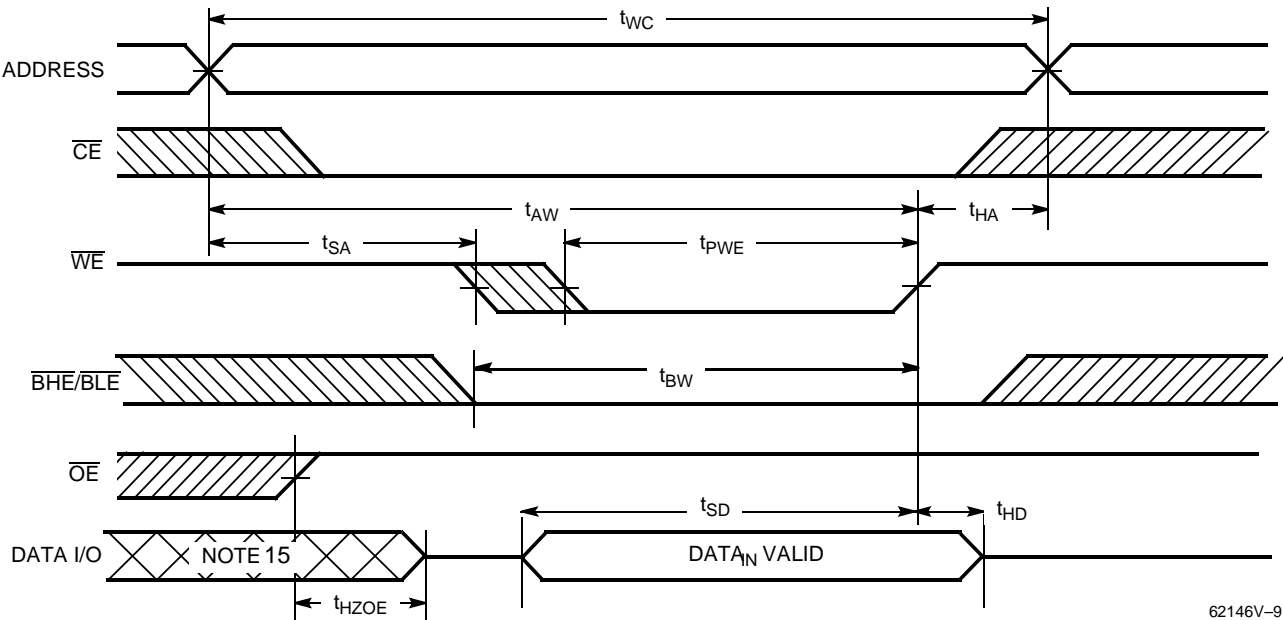
Read Cycle No. 1^[10, 11]



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Notes:

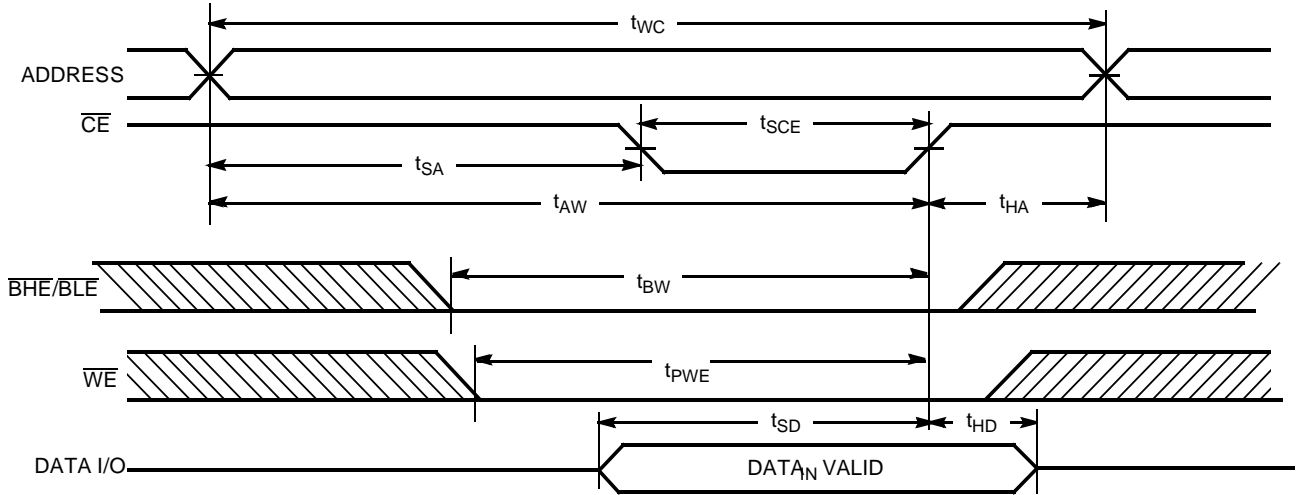
6. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}; t_{HZOE} is less than t_{LZOE}; and t_{HZWE} is less than t_{LZWE} for any given device.
7. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
8. The internal write time of the memory is defined by the overlap of CE LOW and WE LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
9. The minimum write cycle time for write cycle #3 (WE controlled, OE LOW) is the sum of t_{HZWE} and t_{SD}.
10. Device is continuously selected. OE, CE = V_{IL}.
11. WE is HIGH for read cycle.

Switching Waveforms (continued)
Read Cycle No. 2 [11, 12]

Write Cycle No. 1 (\overline{WE} Controlled) [8, 13, 14]

Notes:

12. Address valid prior to or coincident with \overline{CE} transition LOW.
13. Data I/O is high impedance if $OE = V_{IH}$.
14. If \overline{CE} goes HIGH simultaneously with \overline{WE} HIGH, the output remains in a high-impedance state.
15. During this period, the I/Os are in output state and input signals should not be applied.

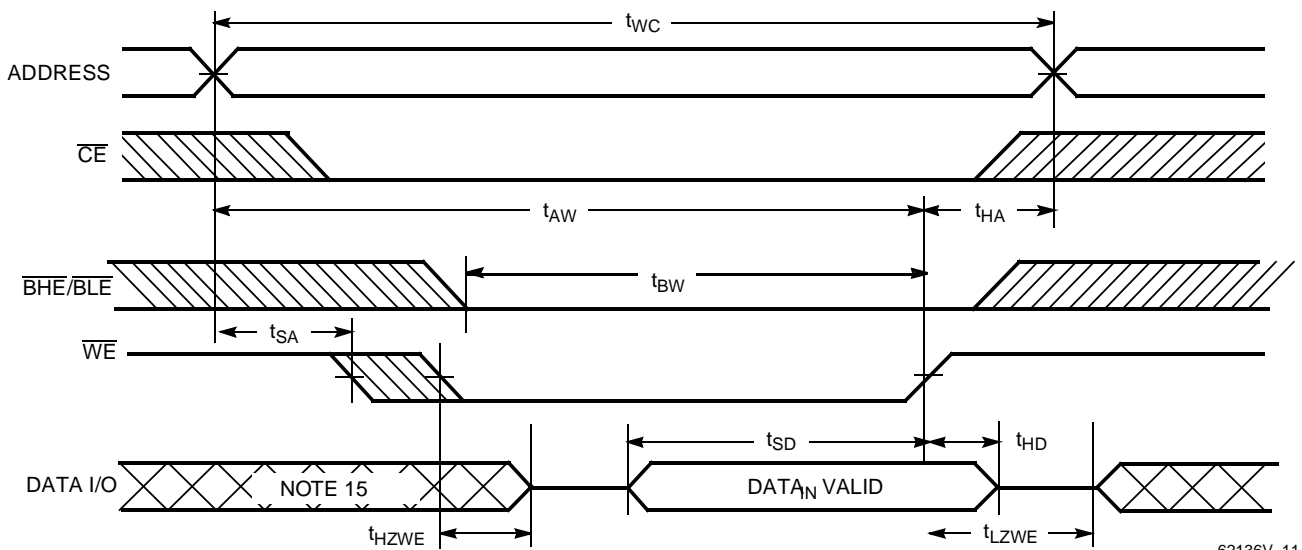
Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{\text{CE}}$ Controlled) [8, 13, 14]



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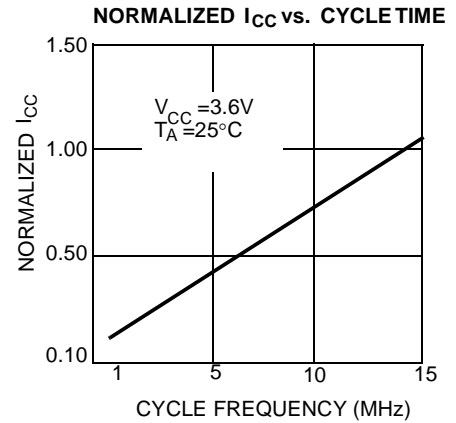
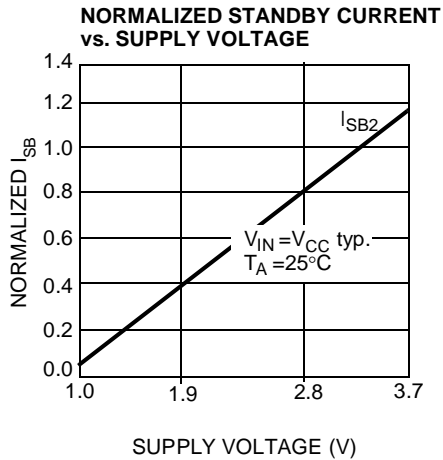
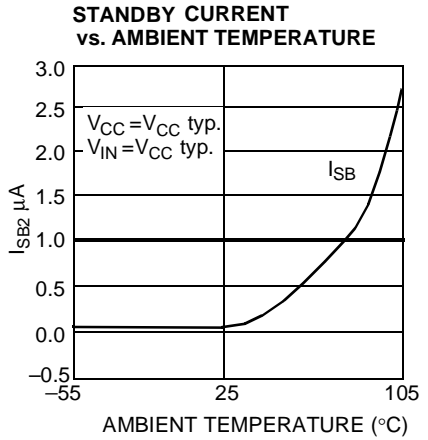
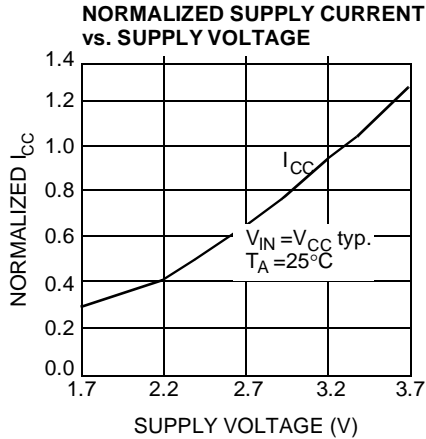
Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW) [9, 14]



62136V-11



Typical DC and AC Characteristics



Truth Table

\overline{CE}	\overline{WE}	\overline{OE}	\overline{BHE}	\overline{BLE}	Inputs/Outputs	Mode	Power
H	X	X	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	L	L	L	Data Out (I/O_0 – I/O_{15})	Read	Active (I_{CC})
L	H	L	H	L	Data Out (I/O_0 – I/O_7); I/O_8 – I/O_{15} in High Z	Read	Active (I_{CC})
L	H	L	L	H	Data Out (I/O_8 – I/O_{15}); I/O_0 – I/O_7 in High Z	Read	Active (I_{CC})
L	H	H	L	L	High Z	Deselect/Output Disabled	Active (I_{CC})
L	H	H	H	L	High Z	Deselect/Output Disabled	Active (I_{CC})
L	H	H	L	H	High Z	Deselect/Output Disabled	Active (I_{CC})
L	L	X	L	L	Data In (I/O_0 – I/O_{15})	Write	Active (I_{CC})
L	L	X	H	L	Data In (I/O_0 – I/O_7); I/O_8 – I/O_{15} in High Z	Write	Active (I_{CC})
L	L	X	L	H	Data In (I/O_8 – I/O_{15}); I/O_0 – I/O_7 in High Z	Write	Active (I_{CC})



CY62136V MoBL™ CY62136V18 MoBL2™

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	CY62136VLL-70ZI	Z44	44-Pin TSOP II	Industrial
	CY62136VLL-70BAI	BA48	48-Ball Fine Pitch BGA	
	CY62136V18LL-70BAI	BA48	48-Ball Fine Pitch BGA	

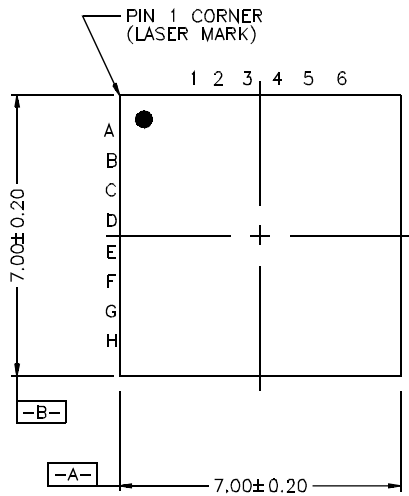
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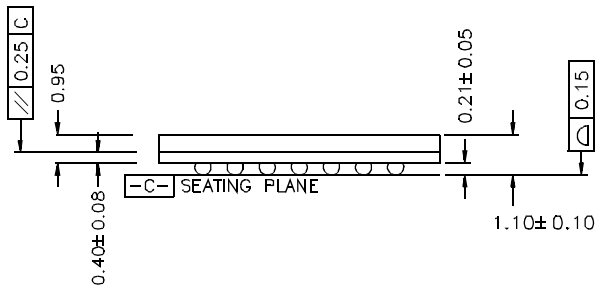
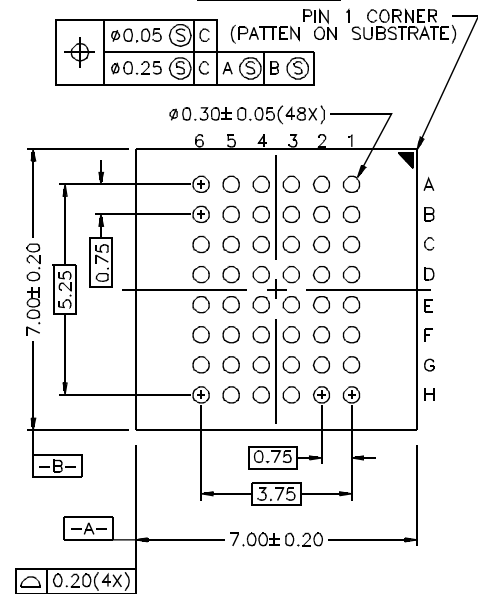
Package Diagrams

48-Ball (7.00 mm x 7.00 mm) FBGA BA48

TOP VIEW



BOTTOM VIEW



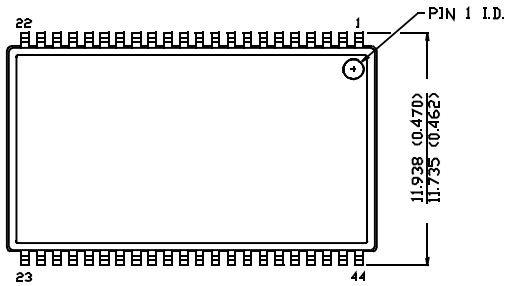


CY62136V MoBL™ CY62136V18 MoBL2™

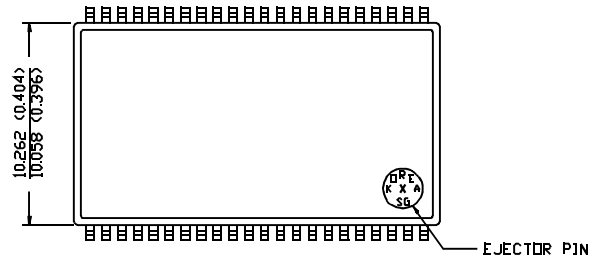
Package Diagrams (continued)

44-Pin TSOP II Z44

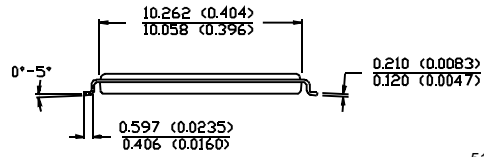
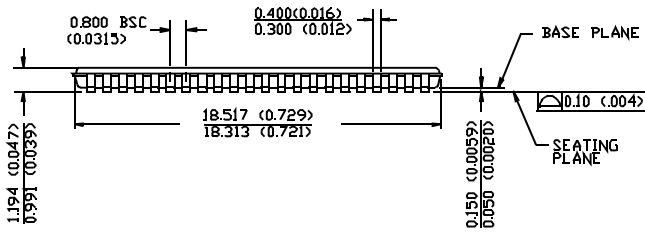
DIMENSION IN MM (INCH)
MAX
MIN.



TOP VIEW



BOTTOM VIEW



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