



CYPRESS

CY7C371i

## UltraLogic™ 32-Macrocell Flash CPLD

## Features

- 32 macrocells in two logic blocks
- 32 I/O pins
- 5 dedicated inputs including 2 clock pins
- In-System Reprogrammable (ISR™) Flash technology
  - JTAG interface
- Bus Hold capabilities on all I/Os and dedicated inputs
- No hidden delays
- High speed
  - $f_{MAX} = 143 \text{ MHz}$
  - $t_{PD} = 8.5 \text{ ns}$
  - $t_S = 5 \text{ ns}$
  - $t_{CO} = 6 \text{ ns}$
- Fully PCI compliant
- 3.3V or 5.0V I/O operation
- Available in 44-pin PLCC, and TQFP packages
- Pin compatible with the CY7C372i

## Functional Description

The CY7C371i is an In-System Reprogrammable Complex Programmable Logic Device (CPLD) and is part of the FLASH370i™ family of high-density, high-speed CPLDs. Like all members of the FLASH370i family, the CY7C371i is designed

to bring the ease of use and high performance of the 22V10, as well as PCI Local Bus Specification support, to high-density CPLDs.

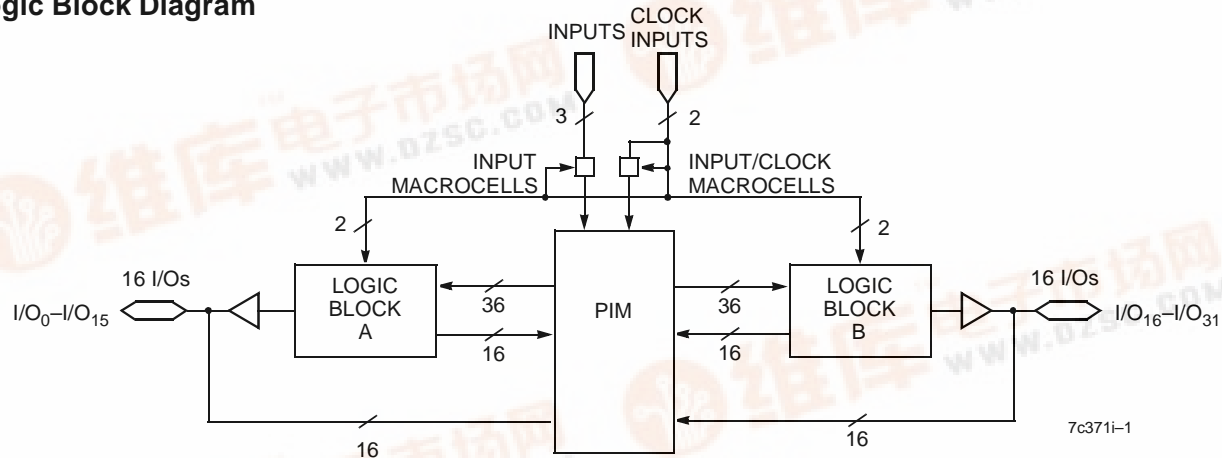
Like all of the UltraLogic™ FLASH370i devices, the CY7C371i is electrically erasable and In-System Reprogrammable (ISR), which simplifies both design and manufacturing flows, thereby reducing costs. The Cypress ISR function is implemented through a JTAG serial interface. Data is shifted in and out through the SDI and SDO pins. The ISR interface is enabled using the programming voltage pin (ISR<sub>EN</sub>). Additionally, because of the superior routability of the FLASH370i devices, ISR often allows users to change existing logic designs while simultaneously fixing pinout assignments.

The 32 macrocells in the CY7C371i are divided between two logic blocks. Each logic block includes 16 macrocells, a 72 x 86 product term array, and an intelligent product term allocator.

The logic blocks in the FLASH370i architecture are connected with an extremely fast and predictable routing resource—the Programmable Interconnect Matrix (PIM). The PIM brings flexibility, routability, speed, and a uniform delay to the interconnect.

Like all members of the FLASH370i family, the CY7C371i is rich in I/O resources. Each macrocell in the device features an associated I/O pin, resulting in 32 I/O pins on the CY7C371i. In addition, there are three dedicated inputs and two input/clock pins.

## Logic Block Diagram



## Selection Guide

	7C371i-143	7C371i-110	7C371i-83	7C371iL-83	7C371i-66	7C371iL-66
Maximum Propagation Delay <sup>[1]</sup> , $t_{PD}$ (ns)	8.5	10	12	12	15	15
Minimum Set-Up, $t_S$ (ns)	5	6	8	8	10	10
Maximum Clock to Output <sup>[1]</sup> , $t_{CO}$ (ns)	6	6.5	8	8	10	10
Typical Supply Current, $I_{CC}$ (mA)	75	75	75	45	75	45

Note: The 3.3V I/O mode timing adder,  $t_{3.3IO}$ , must be added to this specification when  $V_{CCIO} = 3.3V$ .



The FLASH370i family can be configured to operate in both 3.3V and 5.0V systems. All devices have two sets of V<sub>CC</sub> pins: one

set, VCCINT, for internal operation and input buffers, and another set, VCCIO, for I/O output drivers. VCCINT pins must always be connected to a 5.0V power supply. However, the VCCIO pins may be connected to either a 3.3V or 5.0V power supply, depending on the output requirements. When VCCIO pins are connected to a 5.0V source, the I/O voltage levels are compatible with 5.0V systems. When VCCIO pins are connected to a 3.3V source, the input voltage levels are compatible with both 5.0V and 3.3V systems, while the output voltage levels are compatible with 3.3V systems. There will be an additional timing delay on all output buffers when operating in 3.3V I/O mode. The added flexibility of 3.3V I/O capability is available in commercial and industrial temperature ranges.

#### Bus Hold Capabilities on all I/Os and Dedicated Inputs

In addition to ISR capability, a new feature called bus-hold has been added to all FLASH370i I/Os and dedicated input pins. Bus-hold, which is an improved version of the popular internal pull-up resistor, is a weak latch connected to the pin that does not degrade the device's performance. As a latch, bus-hold recalls the last state of a pin when it is three-stated, thus reducing system noise in bus-interface applications. Bus-hold additionally allows unused device pins to remain unconnected on the board, which is particularly useful during prototyping as designers can route new signals to the device without cutting trace connections to VCC or GND.

#### Operating Range

Range	Ambient Temperature	V <sub>CC</sub> V <sub>CCINT</sub>	V <sub>CCIO</sub>
Commercial	0°C to +70°C	5V ± 0.25V	5V ± 0.25V OR 3.3V ± 0.3V
Industrial	–40°C to +85°C	5V ± 0.5V	5V ± 0.5V OR 3.3V ± 0.3V

#### Design Tools

Development software for the CY7C371i is available from Cypress's *Warp2*®, *Warp2Sim*™, and *Warp3*® software packages. All of these products are based on the IEEE-standard VHDL language. Cypress also actively supports third-party design tools from companies such as Synopsys, Mentor Graphics, Cadence, and Synario. Please refer to third-party tool support for further information.

#### Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....	–65°C to +150°C
Ambient Temperature with Power Applied .....	–55°C to +125°C
Supply Voltage to Ground Potential .....	–0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State .....	–0.5V to +7.0V
DC Input Voltage .....	–0.5V to +7.0V
DC Program Voltage .....	12.5V
Output Current into Outputs (LOW) .....	16 mA
Static Discharge Voltage .....	>2001V (per MIL-STD-883, Method 3015)
Latch-Up Current .....	>200 mA

**Electrical Characteristics** Over the Operating Range<sup>[2,3]</sup>

Param.	Description	Test Conditions		Min.	Typ.	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage with Output Enabled	V <sub>CC</sub> = Min.	I <sub>OH</sub> = -3.2 mA (Com'I/Ind) <sup>[4]</sup>	2.4			V
V <sub>OHZ</sub>	Output HIGH Voltage with Output Disabled <sup>[8]</sup>	V <sub>CC</sub> = Max.	I <sub>OH</sub> = 0 $\mu$ A (Com'I/Ind) <sup>[4,5]</sup>			4.0	V
			I <sub>OH</sub> = -50 $\mu$ A (Com'I/Ind) <sup>[4,5]</sup>			3.6	V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min.	I <sub>OL</sub> = 16 mA (Com'I/Ind) <sup>[4]</sup>			0.5	V
V <sub>IH</sub>	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all inputs <sup>[6]</sup>		2.0		7.0	V
V <sub>IL</sub>	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all inputs <sup>[6]</sup>		-0.5		0.8	V
I <sub>IX</sub>	Input Load Current	V <sub>I</sub> = Internal GND, V <sub>I</sub> = V <sub>CC</sub>		-10		+10	$\mu$ A
I <sub>OZ</sub>	Output Leakage Current	V <sub>CC</sub> = Max., V <sub>O</sub> = GND or V <sub>O</sub> = V <sub>CC</sub> , Output Disabled		-50		+50	$\mu$ A
		V <sub>CC</sub> = Max., V <sub>O</sub> = 3.3V, Output Disabled <sup>[5]</sup>		0	-70	-125	$\mu$ A
I <sub>OS</sub>	Output Short Circuit Current <sup>[7,8]</sup>	V <sub>CC</sub> = Max., V <sub>OUT</sub> = 0.5V		-30		-160	mA
I <sub>CC</sub>	Power Supply Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA, f = 1 MHz, V <sub>IN</sub> = GND, V <sub>CC</sub> <sup>[9]</sup>	Com'I/Ind.		75	125	mA
			Com'I "L" -66, -83		45	75	mA
I <sub>BHL</sub>	Input Bus Hold LOW Sustaining Current	V <sub>CC</sub> = Min., V <sub>IL</sub> = 0.8V		+75			$\mu$ A
I <sub>BHH</sub>	Input Bus Hold HIGH Sustaining Current	V <sub>CC</sub> = Min., V <sub>IH</sub> = 2.0V		-75			$\mu$ A
I <sub>BHLO</sub>	Input Bus Hold LOW Overdrive Current	V <sub>CC</sub> = Max.				+500	$\mu$ A
I <sub>BHHO</sub>	Input Bus Hold HIGH Overdrive Current	V <sub>CC</sub> = Max.				-500	$\mu$ A

**Capacitance<sup>[8]</sup>**

Parameter	Description	Test Conditions	Min.	Max.	Unit
C <sub>I/O</sub> <sup>[10]</sup>	Input Capacitance	V <sub>IN</sub> = 5.0V at f=1 MHz		8	pF
C <sub>CLK</sub>	Clock Signal Capacitance	V <sub>IN</sub> = 5.0V at f = 1 MHz	5	12	pF

**Inductance<sup>[8]</sup>**

Parameter	Description	Test Conditions	44-Lead TQFP	44-Lead PLCC	Unit
L	Maximum Pin Inductance	V <sub>IN</sub> = 5.0V at f= 1 MHz	2	5	nH

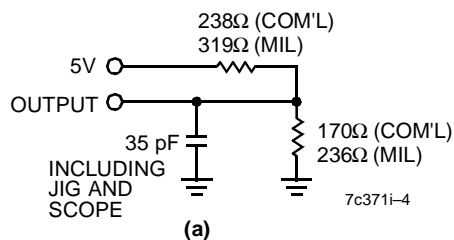
**Endurance Characteristics<sup>[8]</sup>**

Parameter	Description	Test Conditions	Max.	Unit
N	Maximum Reprogramming Cycles	Normal Programming Conditions	100	Cycles

**Notes:**

- See the last page of this specification for Group A subgroup testing information.
- If V<sub>CCIO</sub> is not specified, the device can be operating in either 3.3V or 5V I/O mode; V<sub>CC</sub>=V<sub>CCINT</sub>.
- I<sub>OH</sub> = -2 mA, I<sub>OL</sub> = 2 mA for SDO.
- When the I/O is three-stated, the bus-hold circuit can weakly pull the I/O to a maximum of 4.0V if no leakage current is allowed. This voltage is lowered significantly by a small leakage current. Note that all I/Os are three-stated during ISR programming. Refer to the application note "Understanding Bus Hold" for additional information.
- These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
- Not more than one output should be tested at a time. Duration of the short circuit should not exceed 1 second. V<sub>OUT</sub> = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
- Tested initially and after any design or process changes that may affect these parameters.
- Measured with 16-bit counter programmed into each logic block.

## AC Test Loads and Waveforms

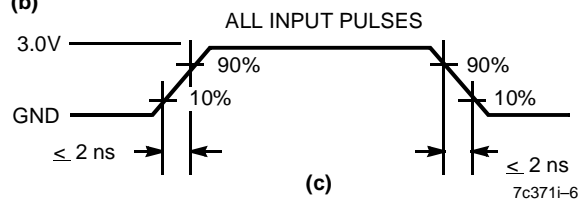
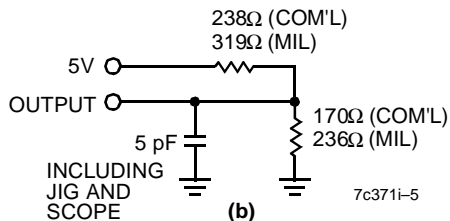



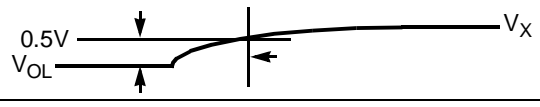
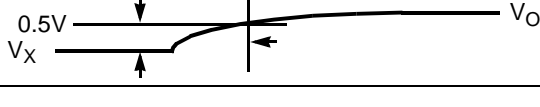
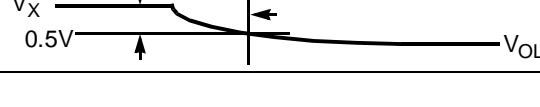
Equivalent to: THÉVENIN EQUIVALENT

99Ω (COM'L)  
136Ω (MIL)

OUTPUT

2.08V(COM'L)  
2.13V(MIL)



Parameter <sup>[11]</sup>	V <sub>x</sub>	Output Waveform Measurement Level
t <sub>ER(-)</sub>	1.5V	
t <sub>ER(+)</sub>	2.6V	
t <sub>EA(+)</sub>	1.5V	
t <sub>EA(-)</sub>	V <sub>the</sub>	

### Notes:

10. Cl/O for ISR<sub>EN</sub> is 15 pF Max.

11. t<sub>ER</sub> measured with 5-pF AC Test Load and t<sub>EA</sub> measured with 35-pF AC Test Load.

**Switching Characteristics** Over the Operating Range<sup>[12]</sup>

Parameter	Description	7C371i-143		7C371i-110		7C371i-83 7C371iL-83		7C371i-66 7C371iL-66		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Combinatorial Mode Parameters										
t <sub>PD</sub>	Input to Combinatorial Output <sup>[1]</sup>		8.5		10		12		15	ns
t <sub>PDL</sub>	Input to Output Through Transparent Input or Output Latch <sup>[1]</sup>		11.5		13		18		22	ns
t <sub>PDLL</sub>	Input to Output Through Transparent Input and Output Latches <sup>[1]</sup>		13.5		15		20		24	ns
t <sub>EA</sub>	Input to Output Enable <sup>[1]</sup>		13		14		19		24	ns
t <sub>ER</sub>	Input to Output Disable		13		14		19		24	ns
Input Registered/Latched Mode Parameters										
t <sub>WL</sub>	Clock or Latch Enable Input LOW Time <sup>[8]</sup>	2.5		3		4		5		ns
t <sub>WH</sub>	Clock or Latch Enable Input HIGH Time <sup>[8]</sup>	2.5		3		4		5		ns
t <sub>IS</sub>	Input Register or Latch Set-Up Time	2		2		3		4		ns
t <sub>IH</sub>	Input Register or Latch Hold Time	2		2		3		4		ns
t <sub>ICO</sub>	Input Register Clock or Latch Enable to Combinatorial Output <sup>[1]</sup>		12		14		19		24	ns
t <sub>ICOL</sub>	Input Register Clock or Latch Enable to Output Through Transparent Output Latch <sup>[1]</sup>		14		16		21		26	ns
Output Registered/Latched Mode Parameters										
t <sub>CO</sub>	Clock or Latch Enable to Output <sup>[1]</sup>		6		6.5		8		10	ns
t <sub>S</sub>	Set-Up Time from Input to Clock or Latch Enable	5		6		8		10		ns
t <sub>H</sub>	Register or Latch Data Hold Time	0		0		0		0		ns
t <sub>CO2</sub>	Output Clock or Latch Enable to Output Delay (Through Memory Array) <sup>[1]</sup>		12		14		19		24	ns
t <sub>SCS</sub>	Output Clock or Latch Enable to Output Clock or Latch Enable (Through Memory Array)	7		9		12		15		ns
t <sub>SL</sub>	Set-Up Time from Input Through Transparent Latch to Output Register Clock or Latch Enable	9		10		12		15		ns
t <sub>HL</sub>	Hold Time for Input Through Transparent Latch from Output Register Clock or Latch Enable	0		0		0		0		ns
f <sub>MAX1</sub>	Maximum Frequency with Internal Feedback (Least of 1/t <sub>SCS</sub> , 1/(t <sub>S</sub> + t <sub>H</sub> ), or 1/t <sub>CO</sub> ) <sup>[8]</sup>	143		111		83.3		66.6		MHz
f <sub>MAX2</sub>	Maximum Frequency Data Path in Output Registered/Latched Mode (Lesser of 1/(t <sub>WL</sub> + t <sub>WH</sub> ), 1/(t <sub>S</sub> + t <sub>H</sub> ), or 1/t <sub>CO</sub> ) <sup>[8]</sup>	166.7		153.8		100		83.3		MHz
f <sub>MAX3</sub>	Maximum Frequency with external feedback (Lesser of 1/(t <sub>CO</sub> + t <sub>S</sub> ) and 1/(t <sub>WL</sub> + t <sub>WH</sub> )) <sup>[8]</sup>	91		80		50		41.6		MHz
t <sub>OH</sub> -t <sub>IH</sub> 37x	Output Data Stable from Output clock Minus Input Register Hold Time for 7C37x <sup>[8,13]</sup>	0		0		0		0		ns

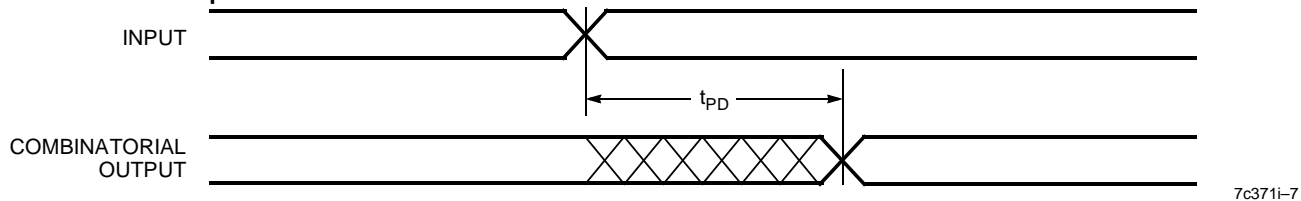
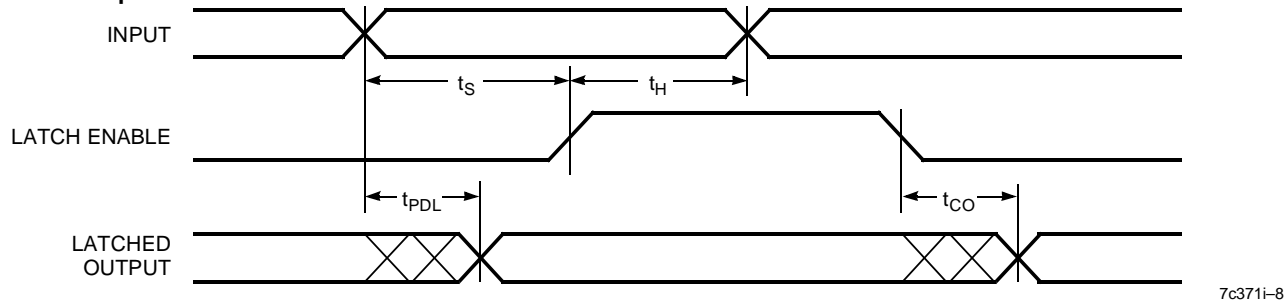
**Notes:**

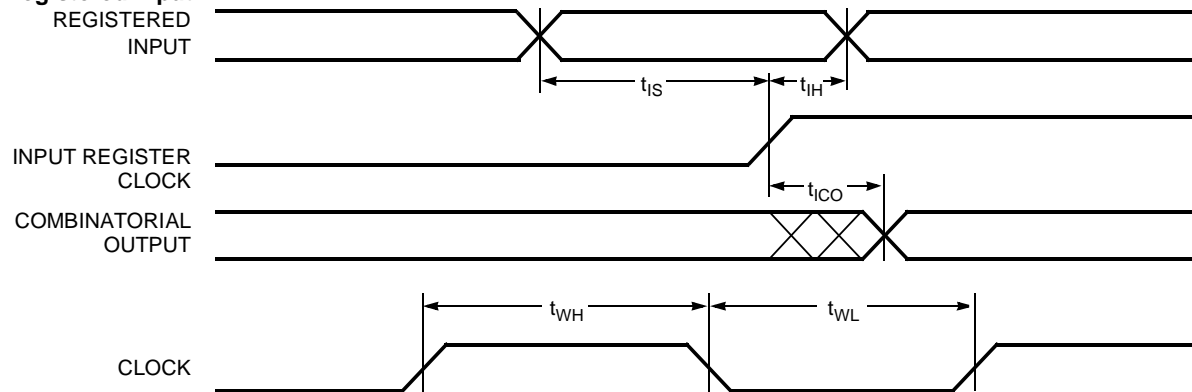
12. All AC parameters are measured with 16 outputs switching and 35-pF AC Test Load.

13. This specification is intended to guarantee interface compatibility of the other members of the CY7C370i family with the CY7C371i. This specification is met for the devices operating at the same ambient temperature and at the same power supply voltage.

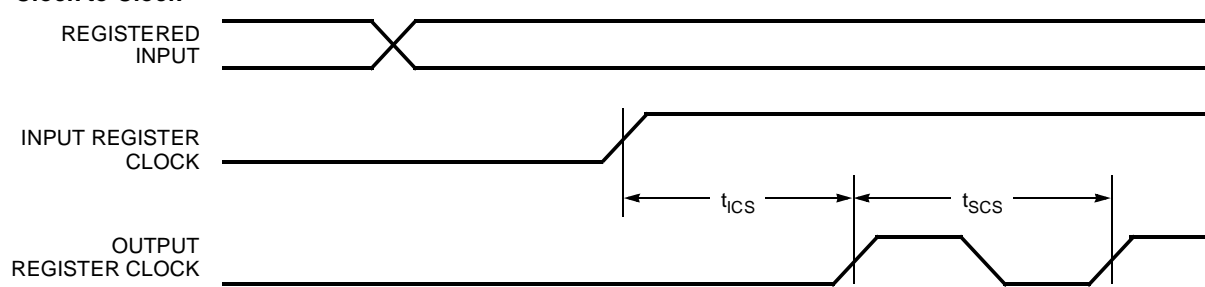
**Switching Characteristics** Over the Operating Range<sup>[12]</sup> (continued)

Parameter	Description	7C371i–143		7C371i–110		7C371i–83 7C371iL–83		7C371i–66 7C371iL–66		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Pipelined Mode Parameters										
t <sub>ICS</sub>	Input Register Clock to Output Register Clock	7		9		12		15		ns
f <sub>MAX4</sub>	Maximum Frequency in Pipelined Mode (Least of 1/(t <sub>CO</sub> + t <sub>IS</sub> ), 1/t <sub>ICS</sub> , 1/(t <sub>WL</sub> + t <sub>WH</sub> ), 1/(t <sub>IS</sub> + t <sub>IH</sub> ), or 1/t <sub>SCS</sub> )	125		111		76.9		62.5		MHz
Reset/Preset Parameters										
t <sub>RW</sub>	Asynchronous Reset Width <sup>[8]</sup>	8		10		15		20		ns
t <sub>RR</sub>	Asynchronous Reset Recovery Time <sup>[8]</sup>	10		12		17		22		ns
t <sub>RO</sub>	Asynchronous Reset to Output <sup>[1]</sup>		14		16		21		26	ns
t <sub>PW</sub>	Asynchronous Preset Width <sup>[8]</sup>	8		10		15		20		ns
t <sub>PR</sub>	Asynchronous Preset Recovery Time <sup>[8]</sup>	10		12		17		22		ns
t <sub>PO</sub>	Asynchronous Preset to Output <sup>[1]</sup>		14		16		21		26	ns
Tap Controller Parameters										
f <sub>TAP</sub>	Tap Controller Frequency	500		500		500		500		kHz
3.3V I/O Mode Parameters										
t <sub>3.3IO</sub>	3.3V I/O mode timing adder		1		1		1		1	ns

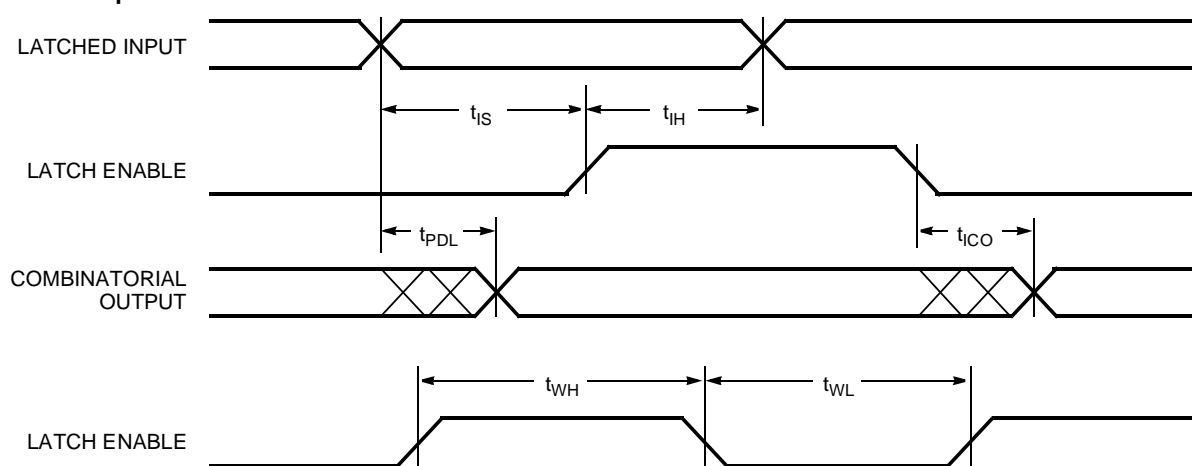
**Switching Waveforms**
**Combinatorial Output**

**Latched Output**


**Switching Waveforms (continued)**
**Registered Input**


7c371i-9

**Clock to Clock**


7c371i-10

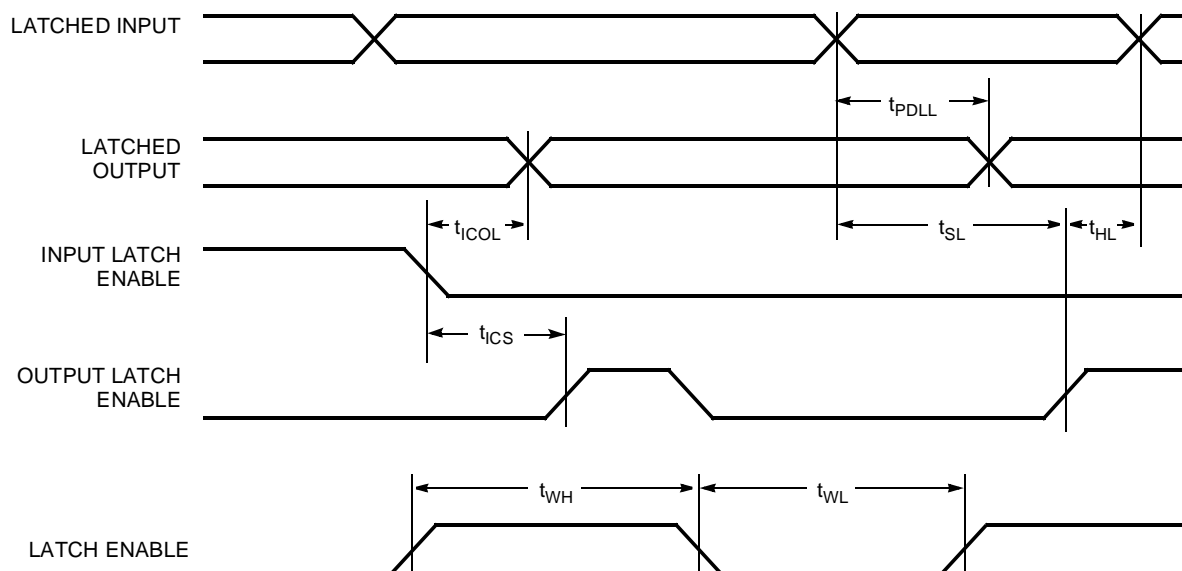
**Latched Input**


7c371i-11



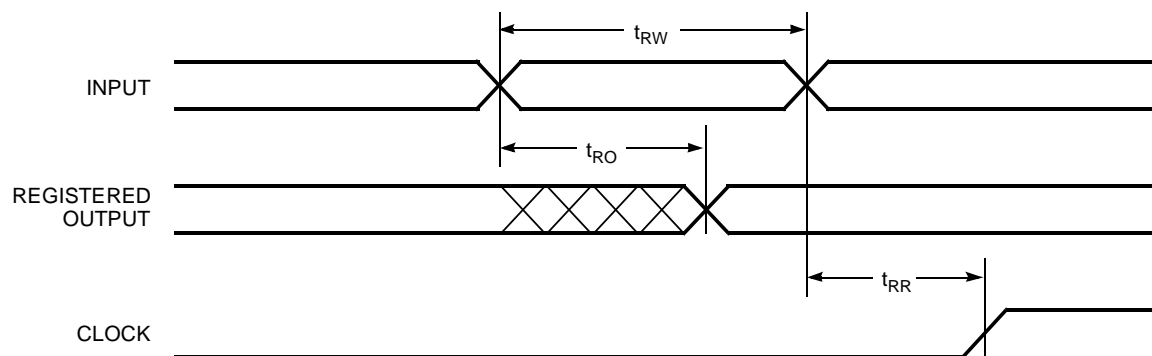
## Switching Waveforms (continued)

### Latched Input and Output



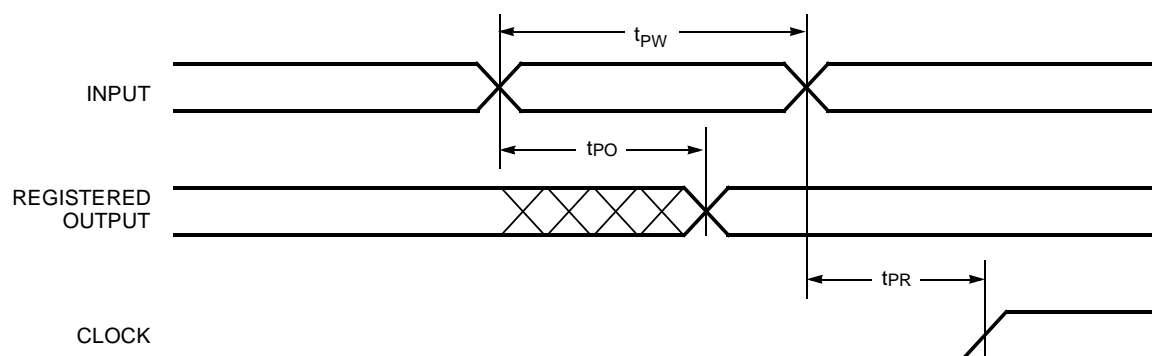
7c371i-12

### Asynchronous Reset



7c371i-13

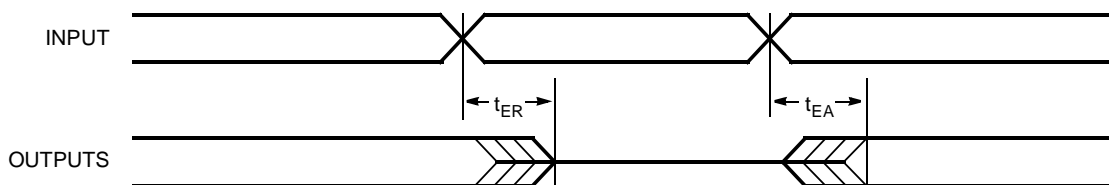
### Asynchronous Preset



7c371i-14

## Switching Waveforms (continued)

### Output Enable/Disable



7c371i-16

## Ordering Information

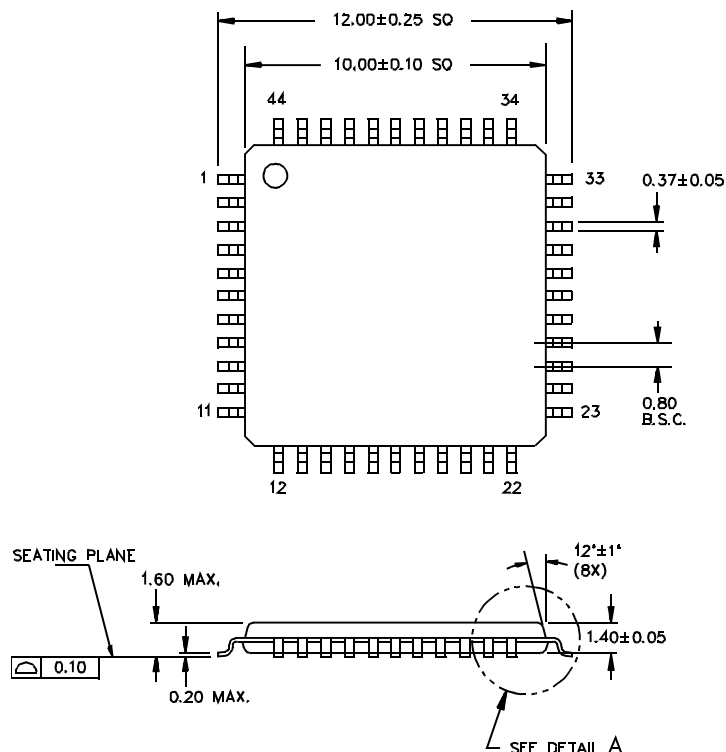
Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
143	CY7C371i-143AC	A44	44-Lead Thin Plastic Quad Flat Pack	Commercial
	CY7C371i-143JC	J67	44-Lead Plastic Leaded Chip Carrier	
110	CY7C371i-110AC	A44	44-Lead Thin Plastic Quad Flat Pack	Commercial
	CY7C371i-110JC	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C371i-110AI	A44	44-Lead Thin Plastic Quad Flat Pack	Industrial
	CY7C371i-110JI	J67	44-Lead Plastic Leaded Chip Carrier	
83	CY7C371i-83AC	A44	44-Lead Thin Plastic Quad Flat Pack	Commercial
	CY7C371i-83JC	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C371i-83AI	A44	44-Lead Thin Plastic Quad Flat Pack	Industrial
	CY7C371i-83JI	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C371iL-83AC	A44	44-Lead Thin Plastic Quad Flat Pack	Commercial
	CY7C371iL-83JC	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C371iL-83AI	A44	44-Lead Thin Plastic Quad Flat Pack	Industrial
	CY7C371iL-83JI	J67	44-Lead Plastic Leaded Chip Carrier	
66	CY7C371i-66AC	A44	44-Lead Thin Plastic Quad Flat Pack	Commercial
	CY7C371i-66JC	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C371i-66AI	A44	44-Lead Thin Plastic Quad Flat Pack	Industrial
	CY7C371i-66JI	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C371iL-66AC	A44	44-Lead Thin Plastic Quad Flat Pack	Commercial
	CY7C371iL-66JC	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C371iL-66AI	A44	44-Lead Thin Plastic Quad Flat Pack	Industrial
	CY7C371iL-66JI	J67	44-Lead Plastic Leaded Chip Carrier	

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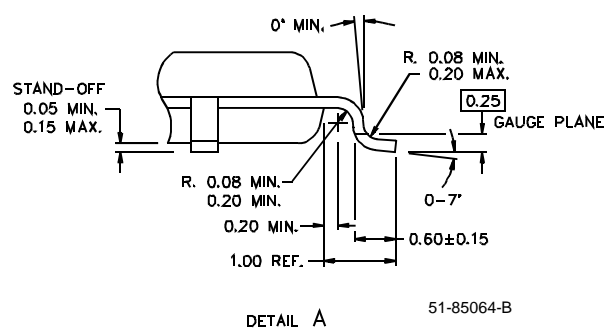
Warp2Sim, FLASH370, FLASH370i, ISR, and UltraLogic are trademarks of Cypress Semiconductor Corporation. Warp2 and Warp3 are registered trademarks of Cypress Semiconductor Corporation.

## Package Diagrams

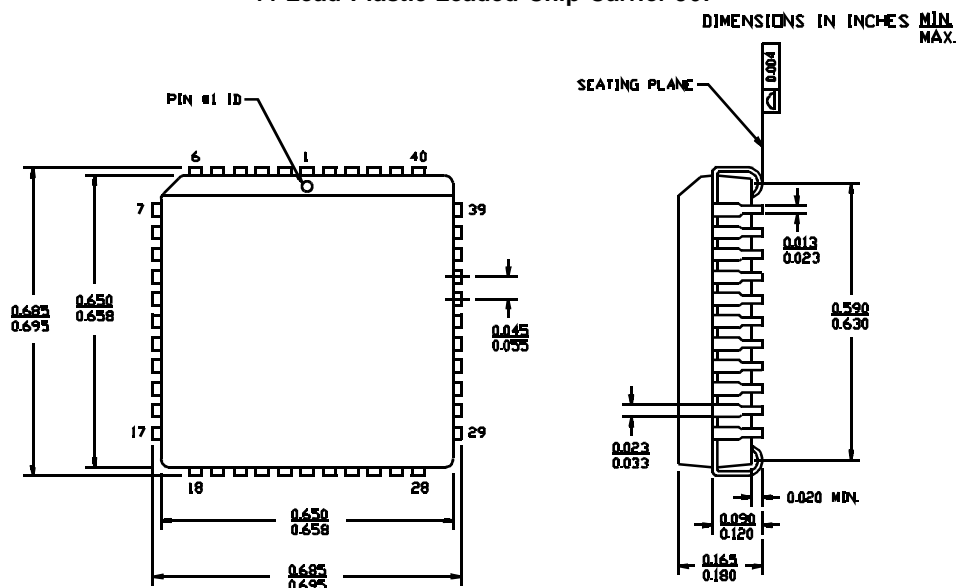
### 44-Lead Thin Plastic Quad Flat Pack A44



DIMENSIONS ARE IN MILLIMETERS



### 44-Lead Plastic Leaded Chip Carrier J67



51-85003-A