



ICD2051

Dual Programmable Clock Generator

Features

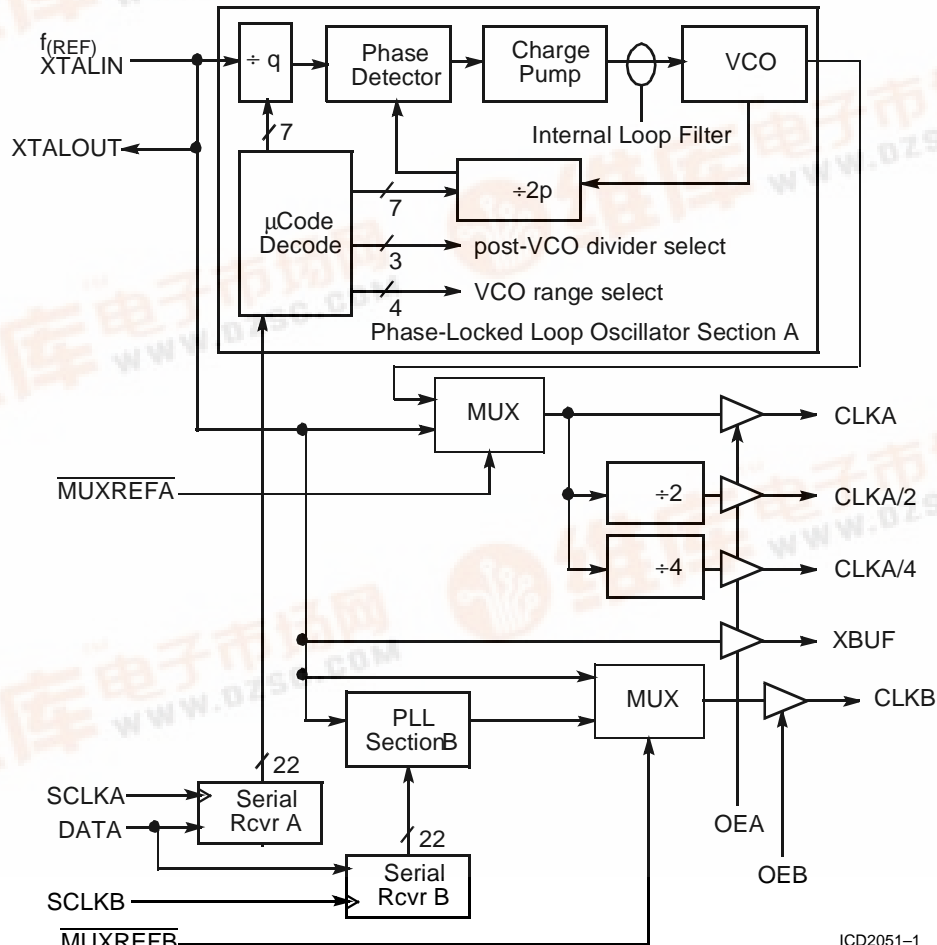
- Two independent clock outputs ranging from 320 kHz to 100 MHz
- Individually programmable PLLs use 22-bit serial word
- Low-skew $\pm 1, \pm 2,$ and ± 4 CLKA outputs
- Phase-locked loop oscillator input derived from external low-frequency reference clock (1 MHz - 25 MHz) or external crystal (2 MHz - 24 MHz)
- Sophisticated internal loop-filter requires no external components or manufacturing tweaks as commonly required with external filters
- Three-state control disables outputs for test purposes (optional)
- 5V operation
- Low-power, high-speed CMOS technology
- Available in 16-pin SOIC package

Functional Description

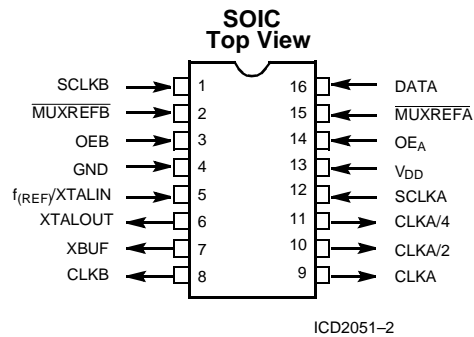
The ICD2051 Programmable Clock Generator offers two fully user-programmable phase-locked loops in a single package. The outputs may be changed "on the fly" to any desired frequency value between 320 kHz and 100 MHz. The ICD2051 is ideally suited for any design where one or more multiple or varying frequencies are required, thus replacing more expensive metal can oscillators.

The capability to dynamically change the output frequency adds a whole new degree of freedom for the electrical engineer. Some examples of the uses for this device include: laptop computers, in which slowing the speed of operation can mean less power consumption or speeding it up can mean faster operation; graphics board dot clocks to allow dynamic synchronization with different brands of monitors or display formats; and on-board test strategies where the ability to skew a system's desired frequency (for example $\pm 10\%$) allows worst case evaluations.

Logic Block Diagram



Pin Configuration



Pin Summary

| Name | Number | Description |
|-------------------------------------|--------|--|
| SCLKB | 1 | Serial clock input line for CLKB |
| MUXREFB | 2 | MUXREFB = 0, CLKB equals input reference frequency MUXREFB = 1, CLKB equals programmed frequency This is used if glitch-free frequency changes are required. |
| OEB | 3 | Three-states CLKB outputs when pulled LOW. (Internal pull-up allows for no-connect if three-state operation is not needed.) |
| GND | 4 | Ground |
| $f_{REF}/$ XTALIN ^[1] | 5 | Reference Oscillator input for all internal phase-locked loops |
| XTALOUT ^[1] | 6 | Oscillator output to a reference crystal. |
| XBUF | 7 | Buffered Crystal Oscillator Output |
| CLKB | 8 | CLKB Programmable Output |
| CLKA | 9 | CLKA Programmable Output |
| CLKA/2 | 10 | CLKA divided by 2 (low skew) |
| CLKA/4 | 11 | CLKA divided by 4 |
| SCLKA | 12 | Serial clock input line for CLKA. |
| V_{DD} | 13 | +5V |
| OE_A | 14 | Three-states CLKA outputs when pulled LOW. (Internal pull-up allows for no-connect if three-state operation is not needed.) |
| MUXREFA | 15 | MUXREFA = 0, CLKA equals input reference frequency MUXREFA = 1, CLKA equals programmed frequency This is used if glitch-free frequency changes are required. |
| DATA | 16 | Serial data input line for both programmable PLLs |

Note:

- For best accuracy, use a parallel-resonant crystal, assume $C_{LOAD} = 17$ pF.

General Considerations

Programming the ICD2051

The desired output frequency is defined via a serial interface, with a 22-bin number shifted in. The ICD2051 has two programmable PLLs (CLKA and CLKB), requiring a 22-bit programming word (W) to be loaded into each channel independently. This word contains 5 fields:

Table 1. Programming Word Bit Fields

| Field | # of bits | Notes |
|----------------------|-----------|------------------------------|
| Index (I) | 4 | MSB (Most Significant Bits) |
| P Counter value (P') | 7 | |
| Reserved (R) | 1 | normally set to logic 1 |
| Mux (M) | 3 | |
| Q Counter value (Q') | 7 | LSB (Least Significant Bits) |

The frequency of the programmable oscillator $f_{(VCO)}$ is determined by these fields as follows:

$$P' = P - 3$$

$$Q' = Q - 2$$

$$f_{(VCO)} = 2 \times f_{(REF)} \times P/Q$$

where $f_{(REF)}$ = Reference frequency (between 1 MHz – 25 MHz)

The value of $f_{(VCO)}$ must remain between 40 MHz and 120 MHz. Therefore, for output frequencies below 40 MHz, $f_{(VCO)}$ must be multiplied up into the required range. To accomplish this, a post-VCO Divisor is selected by setting the values of the Mux field (M) as follows:

Table 2. Mux Field (M)

| M | Divisor |
|-----|---------|
| 000 | 1 |
| 001 | 2 |
| 010 | 4 |
| 011 | 8 |
| 100 | 16 |
| 101 | 32 |
| 110 | 64 |
| 111 | 128 |

The Index field (I) is used to preset the VCO to an appropriate range. The value for this field should be chosen from *Table 3*. (Note that this table is referenced to the VCO frequency $f_{(VCO)}$, rather than to the desired output frequency.)

Table 3. Index Field (I)

| I | $f_{(VCO)}$ (MHz) |
|------|-------------------|
| 0000 | 40.0 – 42.5 |
| 0001 | 42.5 – 47.5 |
| 0010 | 47.5 – 53.5 |
| 0011 | 53.5 – 58.5 |
| 0100 | 58.5 – 62.5 |
| 0101 | 62.5 – 68.5 |
| 0110 | 68.5 – 69.0 |
| 0111 | 69.0 – 82.0 |
| 1000 | 82.0 – 87.0 |
| 1001 | 87.0 – 92.0 |
| 1010 | 92.0 – 92.1 |
| 1011 | 92.1 – 105.0 |
| 1100 | 105.0 – 115.0 |
| 1101 | 115.0 – 120.0 |
| 1110 | 115.0 – 120.0 |
| 1111 | 115.0 – 120.0 |

If the desired VCO frequency lies on a boundary in the table (if it is exactly the upper limit of one entry and the lower limit of the next) then either index value may be used (since both limits are tested), but we recommend using the higher one.

To assist with these calculations, Cypress/IC Designs provides *BitCalc* (Part #ICD/BCALC), a Windows™ program which automatically generates the appropriate programming words from the user's reference input and desired output frequencies. The software also assembles the program words for control and power-down registers. Contact your local Cypress representative for more information.

Programming Constraints

There are five primary programming constraints the user must be aware of:

Table 4. Programming Constraints

| Parameter | Minimum | Maximum |
|---------------|---------|---------|
| $f_{(REF)}$ | 1 MHz | 25 MHz |
| $f_{(REF)}/Q$ | 200 kHz | 1 MHz |
| $f_{(VCO)}$ | 40 MHz | 120 MHz |
| Q | 3 | 129 |
| P | 4 | 130 |

The constraints have to do with trade-offs between optimum speed and lowest noise, VCO stability and factors affecting the loop equation. The factors are listed for completeness sake; however, by using the *BitCalc* program all of these constraints become transparent.

ICD2051 Programming Example

The following is an example of the calculations *BitCalc* performs:

Derive the proper programming word for a 39.5 MHz output frequency, using 14.31818 MHz as the reference frequency:

Since 39.5 MHz < 40 MHz, double it to 79.0 MHz. Set M to 001. Set I to 0111. The result:

$$f_{(VCO)} = 79.0 = (2 \times 14.31818 \times P/Q)$$

$$P/Q = 2.7857$$

Several choices of P and Q are available:

Table 5. P and Q Value Candidates

| P | Q | f _(VCO) (MHz) | Error (PPM) |
|----|----|--------------------------|-------------|
| 69 | 25 | 79.0363 | 460 |
| 80 | 29 | 78.9969 | 40 |
| 91 | 33 | 78.9669 | 419 |

Choose (P, Q) = (80, 29) for best accuracy (40 ppm).

Therefore:

$$P' = P - 3 = 80 - 3 = 77 = 1001101 \text{ (4dH)}$$

$$Q' = Q - 2 = 29 - 2 = 27 = 0011011 \text{ (1bH)}$$

The programming word, W is generated by concatenating I=0111, P'=1001101, R=1, M=001, Q'=0011011 to obtain

$$W = 0111100110110010011011 \text{ (1e6c9bH)}$$

A LOW-to-HIGH transition on SCLKA/SCLKB (depending on appropriate channel) is used to shift the programming word W into DATA as a serial bit stream, LSB first. (See the set-up and hold timing specifications later in this datasheet.) If more than 22 shifts are performed, only the last 22 data bits received will be retained.

Glitch-Free Frequency-Modification Procedure

When changing to a new frequency, there is a period of time when the output signal will be in transition and may glitch due to changes in the post divider. For applications where it is critical that the output clock not glitch and always maintain some known value, the MUXREF_A and MUXREF_B inputs must be used. Under normal operation, MUXREF(X) is HIGH and the output clocks are at the programmed value. When MUXREF(X) is brought LOW, the reference clock is now multiplexed to the associated output clock. The output remains at this fixed frequency while the programmed frequency seeks its new value.

When programming the ICD2051, use the MUXREF inputs in the following manner:

1. Set MUXREF(X) to a LOW state. This will set the output to the reference frequency. The transition is guaranteed to be glitch-free. (See the timing specifications.)
2. Shift in the desired output frequency value via a 22-bit word (as defined above) using the appropriate SCLK and DATA lines.
3. After the last bit is shifted in, the VCO will settle to the new state (within .01% of the actual output frequency) within 10 msec.
4. Set MUXREF(X) to a HIGH state. This will set the output to the new programmed frequency. This transition is guaranteed to be

glitch-free. (See Serial Programming Timing in the Switching Waveforms section of this datasheet.)

Skew-Controlled ±2 on CLKA

The CLKA output is available concurrently as +1, +2, and +4 values of the desired output. The +1 and +2 outputs are also closely matched in order to minimize the phase differences between the two outputs. Typical phase coherence is less than 2 ns of skew between the two outputs, with 1 ns or less available as an order option.

Output Frequency Accuracy

The accuracy of the ICD2051 output frequencies depends on the target output frequency. As stated previously, the output frequencies of the ICD2051 are integrally related to the input reference frequency:

$$f_{(OUT)} = 2 \times f_{(REF)} \times P/Q$$

Only certain output frequencies are possible for a particular reference frequency. However, the ICD2051 normally produces an output frequency within 0.1% of the desired output frequency. Specifics regarding accuracy (ppm) are given for any desired output frequency as part of the *BitCalc* program output.

Three-State Output Operation

The OEA or OEB signal, when pulled LOW, will three-state the clock output line (CLKA or CLKB respectively). This supports wired-OR connections between external clock lines, and allows for procedures such as automated testing where the clock must be disabled. The OE signals contain internal pull-ups; they can be left unconnected if three-state operation is not required.

Estimating Total Current Drain

Actual current drain is a function of frequency and of circuit loading. The operating current of a given output is given by the equation: $I = C \cdot V \cdot f$, where I=current, C=load capacitance (max. 25 pF), V=output voltage (usually 5V), and f=output frequency (in MHz).

To calculate total operating current, sum the following:

| | | |
|----------|---|--------------------------------|
| XBUF | ⇒ | $C \cdot V \cdot f_{(REF)}$ |
| CLKA | ⇒ | $C \cdot V \cdot f_{(CLKA)}$ |
| CLKA/2 | ⇒ | $C \cdot V \cdot f_{(CLKA/2)}$ |
| CLKA/4 | ⇒ | $C \cdot V \cdot f_{(CLKA/4)}$ |
| CLKB | ⇒ | $C \cdot V \cdot f_{(CLKB)}$ |
| Internal | ⇒ | 12 mA |

This gives an approximation of the actual operating current. For unconnected output pins, one can assume 5–10 pF loading, depending on package type.

Typical values:

Table 6. Typical Load Current Values

| Frequency | Load | Current (mA) |
|-----------|------|--------------|
| low | none | 15 |
| high | none | 40 |
| high | high | 100 |



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage to Ground Potential -0.5V to +7.0V
 DC Input Voltage -0.5V to $V_{DD} + 0.5V$
 Storage Temperature -65°C to +150°C
 Max soldering temperature (10 sec) 260°C
 Junction temperature 125°C

Package power dissipation..... 525 mWatts

Operating Range

| Ambient Temperature | V_{DD} & AV_{DD} |
|----------------------------------|----------------------|
| 0°C $\leq T_{AMBIENT} \leq$ 70°C | 5V \pm 5% |

Operating Conditions

| Parameter | Description | Min. | Max. | Unit |
|-----------|-------------------------------|------|------|------|
| V_{DD} | Supply Voltage | 4.75 | 5.25 | V |
| T_A | Ambient Operating Temperature | 0 | 70 | °C |
| C_L | Load Capacitance | | 25 | pF |

Electrical Characteristics Over the Operating Range

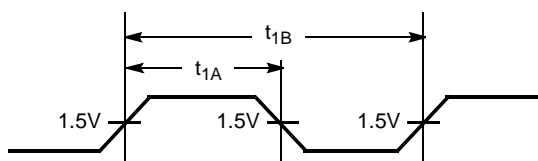
| Parameter | Description | Test Conditions | Min. | Max. | Unit |
|-----------|------------------------|---|------|------|---------|
| V_{OH} | Output HIGH Voltage | $I_{OH} = -4.0mA$ | 2.4 | | V |
| V_{OL} | Output LOW Voltage | $I_{OL} = 4.0 mA$ | | 0.4 | V |
| V_{IH} | Input HIGH Voltage | Except XTALIN pins | 2.0 | | V |
| V_{IL} | Input LOW Voltage | Except XTALIN pins | | 0.8 | V |
| I_{IH} | Input HIGH Current | $V_{IN} = 5.25V$ | | 150 | μA |
| I_{IL} | Input LOW Current | $V_{IN} = 0V$ | | -250 | μA |
| I_{OZ} | Output Leakage Current | Three-state outputs | | 10 | μA |
| I_{DD} | Power Supply Current | $V_{DD} = V_{DD} \text{ max.}, 100 \text{ MHz}, V_{IN} = V_{DD} \text{ or } 0V$ | 15 | 100 | mA |

Switching Characteristics Over the Operating Range^[2]

| Parameter | Name | Description | Min. | Max. | Unit |
|-------------|--------------------------|---|---------------------|------------------|------|
| | Output Frequency | | 0.320 | 100 | MHz |
| $f_{(REF)}$ | Reference Frequency | Reference Oscillator nominal value | 1 | 25 | MHz |
| $t_{(REF)}$ | Reference Clock Period | $t_{(REF)} = 1/f_{(REF)}$ | 40 | 1000 | ns |
| | Duty Cycle | Duty cycle for the output oscillators defined as $t_{1A} \div t_{1B}$ | 40% | 60% | |
| t_2 | Output Rise Time | Rise time for the outputs into a 25-pF load | | 3 | ns |
| t_3 | Output Fall Time | Fall time for the outputs into a 25-pF load | | 3 | ns |
| t_4 | CLKA/2/4 skew | Skew delay between the CLKA output and the CLKA/2 and CLKA/4 outputs | | 2 | ns |
| t_5 | MUXREF Set-Up Time | Delay required after MUXREF goes LOW prior to starting the SCLK clock line | t_{freq1} | | ns |
| t_6 | SCLK Cycle Time | Minimum cycle time for the SCLK clock | $2 \cdot t_{(REF)}$ | | ns |
| t_{6H} | SCLK HIGH Time | Minimum HIGH time for the SCLK clock | $t_{(REF)}$ | | ns |
| t_{6L} | SCLK LOW Time | Minimum LOW time for the SCLK clock | $t_{(REF)}$ | | ns |
| t_7 | Output Clock Stable Time | Time required for CLKA or CLKB output to become valid after last SCLK clock | | 10 | msec |
| t_8 | Data Set-Up Time | Time required for the data to be valid prior to the rising edge of SCLK | 10 | | ns |
| t_9 | Data Hold Time | Time required for the data to remain valid after the rising edge of SCLK | 5 | | ns |
| t_{10} | Transition Time | Time for CLKA or CLKB to go HIGH after assertion of MUXREF | 0 | t_{freq1} | ns |
| t_{11} | Transition Time | Delay of CLKA or CLKB prior to valid $t_{(REF)}$ signal at output | $t_{(REF)}/2$ | $3(t_{(REF)}/2)$ | ns |
| t_{12} | Transition Time | Time for CLKA or CLKB to go HIGH after release of MUXREF | 0 | $t_{(REF)}$ | ns |
| t_{13} | Transition Time | Delay of CLKA or CLKB prior to valid new frequency at output | $t_{freq2}/2$ | $3(t_{freq2}/2)$ | ns |
| t_{14} | Output Disable Time | Time for the outputs to go into three-state mode after OE signal assertion | | 12 | ns |
| t_{15} | Output Enable Time | Time for the outputs to recover from three-state mode after OE signal goes HIGH | | 12 | ns |

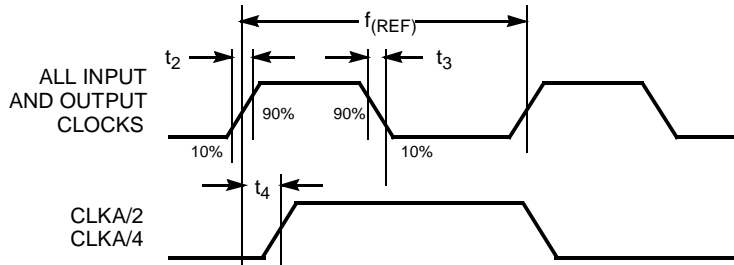
Note:

- Input capacitance is typically 10 pF, except for the crystal pads.

Switching Waveforms
Duty Cycle Timing


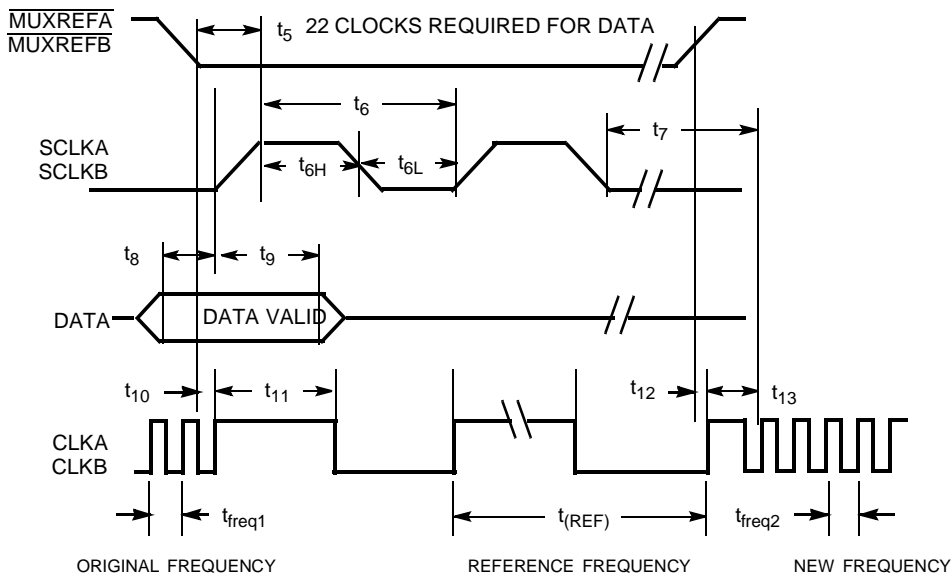
Switching Waveforms (continued)

Rise and Fall Times



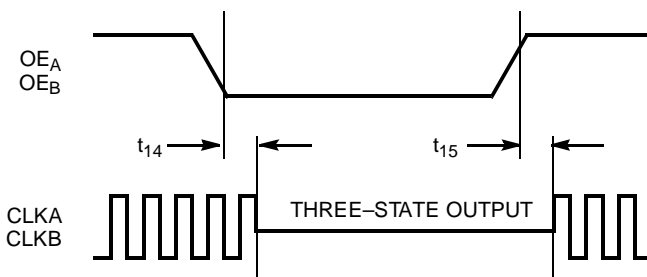
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Serial Programming Timing



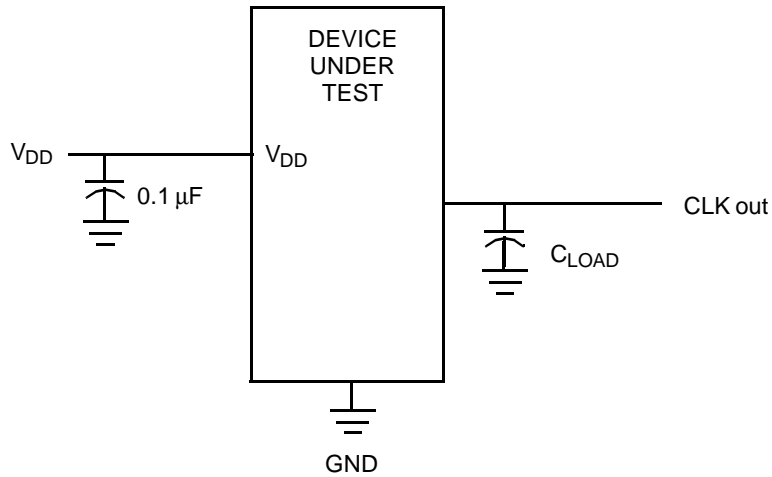
ICD2051-5

Three-State Timing



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Test Circuit



Ordering Information

| Ordering Code | Package Name | Package Type | Operating Range |
|---------------|--------------|--------------|---------------------------|
| ICD2051 | S1 | 16-Pin SOIC | Commercial ^[3] |

Note:

3. 0°C to +70°C

Document #: 38-00402

Package Diagram

16-Lead Molded SOIC S1

