PRELIMINARY

W237

440BX/MX Spread Spectrum Frequency Synthesizer

Features

- **Maximized EMI suppression using Cypress's Spread Spectrum technology**
- **Single-chip system frequency synthesizer for Mobile Intel® 440BX**
- **Two copies of CPU output**
- **I²C™ interface for programming**
- **Seven copies of PCI output**
- **Two 48/24MHz outputs for USB and SIO**
- **Three buffered reference outputs**
- **Eight buffered SDRAM outputs provide support for 2 DIMMs**
- **Spread Spectrum feature enabled through I²C interface and pin option**
- **Power management control inputs**

Key Specifications

CPU Cycle-to-Cycle Jitter:.....250 ps

CPU to CPU Output Skew:.....175 ps

PCI to PCI Output Skew:.....500 ps

VDDQ3:.....3.3V±5%

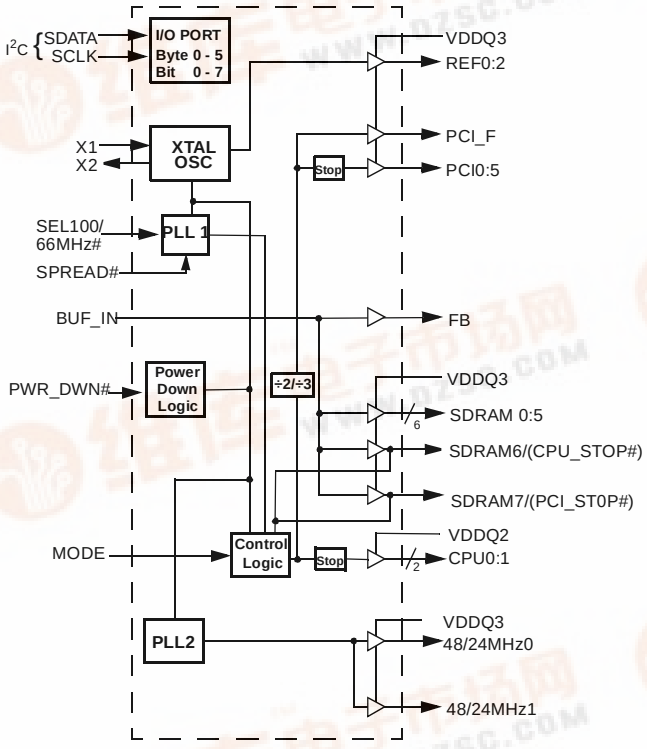
VDDQ2:.....2.5V±5%

SDRAM0:7 Delay:.....+3.7 ns typ.

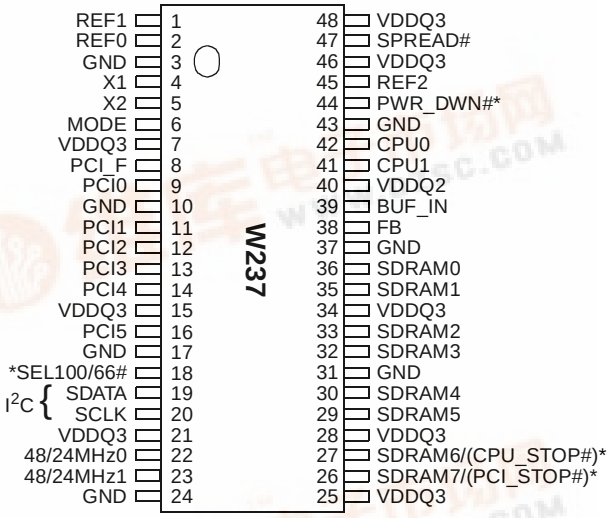
Table 1. Clock Select Table[1]

SEL100/66 (MHz)	CPU,SDRAM (MHz)	PCI (MHz)
0	66.6	33.3
1	100	33.3

Block Diagram



Pin Configuration[2]



Notes:

1. Mode input latched at power-up.
2. Pin function with parentheses determined by MODE pin logic state. Internal 250-kΩ pull-up resistors present on inputs marked with *. Design should not rely solely on internal resistor to set I/O pins HIGH.

Pin Definitions

Pin Name	Pin No.	Pin Type	Pin Description
CPU0:1	42, 41	O	***CPU Clock Outputs:*** See *Table 1* for detailed frequency information. Output voltage swing is controlled by voltage applied to VDDQ2.
PCI0:5	9, 11, 12, 13, 14, 16	O	***PCI Clock Outputs 0 through 5:*** These six PCI clock outputs are controlled by the PCI_STOP# control pin. Output voltage swing is controlled by voltage applied to VDDQ3.
PCI_F	8	O	***Fixed PCI Clock Output:*** Unlike PCI0:5 outputs, this output is not controlled by the PCI_STOP# control pin. Output voltage swing is controlled by voltage applied to VDDQ3.
MODE	6	I	***Mode Control:*** This input selects the function of device pin 26 (SDRAM7/PCI_STOP#) and pin 27 (SDRAM6/CPU_STOP#). Refer to description for those pins.
PWR_DWN#	44	I	***Power-Down Control:*** When this input is LOW, device goes into a low-power condition. All outputs are held LOW while in power-down, CPU and PCI clock outputs are stopped LOW after completing a full clock cycle (2–3 CPU clock cycle latency). When brought HIGH, CPU, SDRAM, and PCI outputs start with a full clock cycle at full operating frequency (3 ms maximum latency).
FB	38	O	***Feedback out***
SPREAD#	47	I	***Spread#:*** When LOW, enables spread spectrum clocking.
SEL100/66#	18	I	***SEL 66- or 100-MHz Input Selection:*** Selects power-up default CPU clock frequency as shown in *Table 1* on page 1 (also determines SDRAM and PCI clock frequency selections).
BUF_IN	39	I	***Clock Input:*** This clock input has an input threshold voltage of 1.5V (typ.).
48/24MHz0:1	22,23	O	***48-/24-MHz Output:*** 48/24MHz is provided in normal operation. In standard systems, this output can be used as the reference for the Universal Serial Bus. This output does not have the Spread Spectrum feature.
REF0:2	2, 1,45	O	***Reference Clock Outputs 0 through 2:*** This pin provides a fixed clock signal equal in frequency to the reference signal provided at the X1/X2 pins.
SDRAM7/ PCI_STOP#	26	I/O	***SDRAM Clock Output 7 or PCI Clock Output Stop Control:*** This pin has dual functions, selectable by the MODE input pin. When MODE = 0, this pin becomes the PCI_STOP# input. When MODE = 1, this pin becomes SDRAM clock output 7. PCI_STOP# input: When brought LOW, clock outputs PCI0:5 are stopped LOW after completing a full clock cycle. When brought HIGH, clock outputs PCI0:5 are started beginning with a full clock cycle. Clock latency provides one PCI_F rising edge of PCI clock following PCI_STOP# state change. Regarding use as a SDRAM clock: Output voltage swing is controlled by voltage applied to VDDQ3.
SDRAM6/CPU_ STOP#	27	I/O	***SDRAM Clock Output 6 or CPU Clock Output Stop Control:*** This pin has dual functions, selectable by the MODE input pin. When MODE = 0, this pin becomes the CPU_STOP# input. When MODE = 1, this pin becomes SDRAM clock output 6. Regarding use as a CPU_STOP# input: When brought LOW, clock outputs CPU0:1 are stopped LOW after completing a full clock cycle (2–3 CPU clock latency). When brought HIGH, clock outputs CPU0:1 are started beginning with a full clock cycle (2–3 CPU clock latency). Regarding use as a SDRAM clock: Output voltage swing is controlled by voltage applied to VDDQ3.
SDRAM0:5	36, 35, 33, 32, 30, 29	O	**Buffered Outputs:** These six dedicated outputs provide copies of the signal provided at the BUF_IN input. The swing is set by VDDQ3.
SCLK	20	I	Clock pin for I^2C circuitry.
SDATA	19	I/O	Data pin for I^2C circuitry.
X1	4	I	***Crystal Connection or External Reference Frequency Input:*** This pin has dual functions. It can be used as an external 14.318-MHz crystal connection or as an external reference frequency input.

Pin Definitions (continued)

Pin Name	Pin No.	Pin Type	Pin Description
X2	5	I	***Crystal Connection:*** An input connection for an external 14.318-MHz crystal. If using an external reference, this pin must be left unconnected.
VDDQ3	7, 15, 21, 25, 28, 34, 46, 48	P	***Power Connection:*** Power supply for core logic, PLL circuitry, SDRAM outputs, PCI outputs, reference outputs, 48-MHz output, and 24-MHz output. Connect to 3.3V supply.
VDDQ2	40	P	***Power Connection:*** Power supply for CPU0:1 output buffers. Connect to 2.5V supply.
GND	3, 10, 17, 24, 31, 37, 43	G	***Ground Connections:*** Connect all ground pins to the common system ground plane.

Overview

The W237 was developed as a single-chip device to meet the clocking needs of the Intel 440BX. In addition to the typical outputs provided by standard 100-MHz 440BX FTGs, the W237 adds eight SDRAM output buffers supporting 2 DIMM modules in conjunction with the chipset.

Cypress's proprietary spread spectrum frequency synthesis technique is a feature of the CPU and PCI outputs. This feature reduces the peak EMI measurements of not only the output signals and their harmonics, but also of any other clock signals that are properly synchronized to them.

Spread Spectrum Frequency Timing Generator

The device generates a clock that is frequency modulated in order to increase the bandwidth that it occupies. By increasing the bandwidth of the fundamental and its harmonics, the amplitudes of the radiated electromagnetic emissions are reduced. This effect is depicted in *Figure 1*.

As shown in *Figure 1*, a harmonic of a modulated clock has a much lower amplitude than that of an unmodulated signal. The reduction in amplitude is dependent on the harmonic number and the frequency deviation or spread. The equation for the reduction is:

$dB = 6.5 + 9*\log_{10}(P) + 9*\log_{10}(F)$

Where P is the percentage of deviation and F is the frequency in MHz where the reduction is measured.

The output clock is modulated with a waveform depicted in *Figure 2*. This waveform, as discussed in "Spread Spectrum Clock Generation for the Reduction of Radiated Emissions" by Bush, Fessler, and Hardin produces the maximum reduction in the amplitude of radiated electromagnetic emissions. The deviation selected for this chip is either –0.25% or ±0.5% of the selected frequency. *Figure 2* details the Cypress spreading pattern. Cypress does offer options with more spread and greater EMI reduction. Contact your local Sales representative for details on these devices.

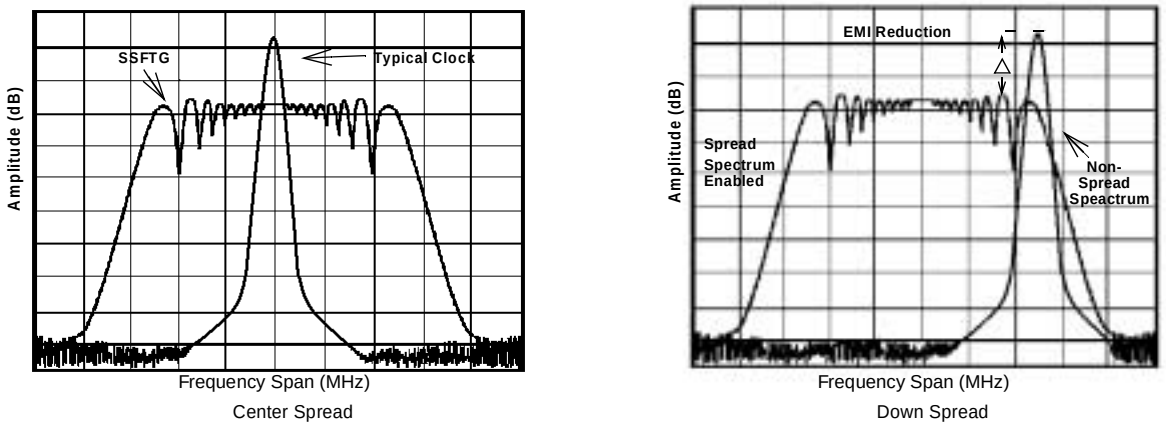


Figure 1. Clock Harmonic with and without SSCG Modulation Frequency Domain Representation

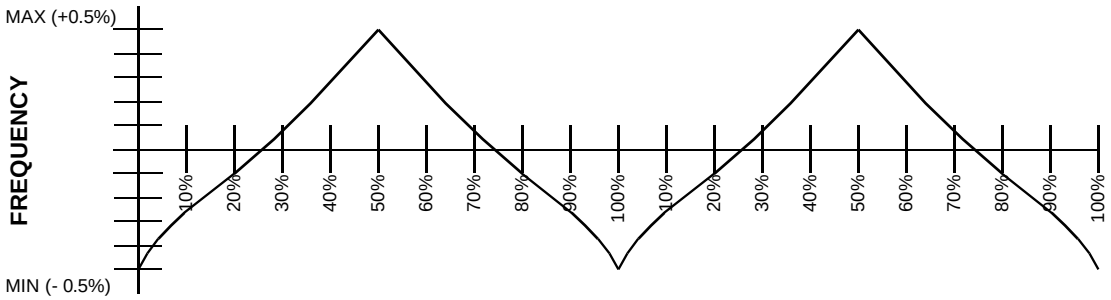


Figure 2. Modulation Waveform Profile

Serial Data Interface

The W237 features a two-pin, serial data interface that can be used to configure internal register settings that control particular device functions. Upon power-up, the W237 initializes with default register settings, therefore the use of this serial data interface is optional. The serial interface is write-only (to the clock chip) and is the dedicated function of device pins SDATA and SCLK. In motherboard applications, SDATA and SCLK are typically driven by two logic outputs of the chipset. Clock device register changes are normally made upon system initialization, if any are required. The interface can also be used during system operation for power management functions. *Table 2* summarizes the control functions of the serial data interface.

Operation

Data is written to the W237 in ten bytes of eight bits each. Bytes are written in the order shown in *Table 3*.

Table 2. Serial Data Interface Control Functions Summary

Control Function	Description	Common Application
Clock Output Disable	Any individual clock output(s) can be disabled. Disabled outputs are actively held LOW.	Unused outputs are disabled to reduce EMI and system power. Examples are clock outputs to unused PCI slots.
CPU Clock Frequency Selection	Provides CPU/PCI frequency selections through software. Frequency is changed in a smooth and controlled fashion.	For alternate microprocessors and power management options. Smooth frequency transition allows CPU frequency change under normal system operation.
Spread Spectrum Enabling	Enables or disables spread spectrum clocking.	For EMI reduction.
Output Three-state	Puts clock output into a high-impedance state.	Production PCB testing.
(Reserved)	Reserved function for future device revision or production device testing.	No user application. Register bit must be written as 0.

Table 3. Byte Writing Sequence

Byte Sequence	Byte Name	Bit Sequence	Byte Description
1	Slave Address	11010010	Commands the W237 to accept the bits in Data Bytes 0–6 for internal register configuration. Since other devices may exist on the same common serial data bus, it is necessary to have a specific slave address for each potential receiver. The slave receiver address for the W237 is 11010010. Register setting will not be made if the Slave Address is not correct (or is for an alternate slave receiver).
2	Command Code	Don't Care	Unused by the W237, therefore bit values are ignored ("don't care"). This byte must be included in the data write sequence to maintain proper byte allocation. The Command Code Byte is part of the standard serial communication protocol and may be used when writing to another addressed slave receiver on the serial data bus.
3	Byte Count	Don't Care	Unused by the W237, therefore bit values are ignored ("don't care"). This byte must be included in the data write sequence to maintain proper byte allocation. The Byte Count Byte is part of the standard serial communication protocol and may be used when writing to another addressed slave receiver on the serial data bus.
4	Data Byte 0	Refer to *Table 4*	The data bits in Data Bytes 0–7 set internal W237 registers that control device operation. The data bits are only accepted when the Address Byte bit sequence is 11010010, as noted above. For description of bit control functions, refer to *Table 4*, Data Byte Serial Configuration Map.
5	Data Byte 1		
6	Data Byte 2		
7	Data Byte 3		
8	Data Byte 4		
9	Data Byte 5		
10	Data Byte 6		

Writing Data Bytes

Each bit in Data Bytes 0–7 controls a particular device function except for the “reserved” bits, which must be written as a logic 0. Bits are written MSB (most significant bit) first, which is bit 7. *Table 4* gives the bit formats for registers located in Data Bytes 0-7.

Table 5 details the select functions for Byte 0, bits 1 and 0.

Table 4. Data Bytes 0-7 Serial Configuration Map

Bit(s)	Affected Pin		Control Function	Bit Control		Default
	Pin No.	Pin Name		0	1	
Data Byte 0						
7	--	--	(Reserved)	--	--	0
6	--	--	(Reserved)			0
5	47	SPREAD#	Spread Spectrum Control	Center Spread	Down Spread	1
4			Spread Spectrum Control Spreading	±0.5%	–0.25%	0
3	23	48/24MHZ1	48/24MHZ1 Frequency Select	24 MHz	48 MHz	1
2	22	48/24MHZ0	48/24MHZ0 Frequency Select	24 MHz	48 MHz	1
1–0	--	--	**Bit 1 Bit 0 Function (See *Table 5* for function details)** 0 0 Normal Operation 0 1 Test Mode 1 0 Spread Spectrum Enable 1 1 All Outputs Three-stated			00
Data Byte 1						
7	23	48/24MHZ1	Clock Output Disable	Low	Active	1
6	22	48/24MHZ0	Clock Output Disable	Low	Active	1
5	--	--	(Reserved)	--	--	0
4	--	--	(Reserved)	--	--	0
3	--	--	(Reserved)	--	--	0
2	--	--	(Reserved)	--	--	0
1	41	CPU1	Clock Output Disable	Low	Active	1
0	42	CPU0	Clock Output Disable	Low	Active	1
Data Byte 2						
7	--	--	(Reserved)	--	--	0
6	8	PCI_F	Clock Output Disable	Low	Active	1
5	16	PCI5	Clock Output Disable	Low	Active	1
4	14	PCI4	Clock Output Disable	Low	Active	1
3	13	PCI3	Clock Output Disable	Low	Active	1
2	12	PCI2	Clock Output Disable	Low	Active	1
1	11	PCI1	Clock Output Disable	Low	Active	1
0	9	PCI0	Clock Output Disable	Low	Active	1
Data Byte 3						
7	26	SDRAM7	Clock Output Disable	Low	Active	1
6	27	SDRAM6	Clock Output Disable	Low	Active	1
5	29	SDRAM5	Clock Output Disable	Low	Active	1
4	30	SDRAM4	Clock Output Disable	Low	Active	1
3	32	SDRAM3	Clock Output Disable	Low	Active	1
2	33	SDRAM2	Clock Output Disable	Low	Active	1

Table 4. Data Bytes 0-7 Serial Configuration Map (continued)

Bit(s)	Affected Pin		Control Function	Bit Control		Default
	Pin No.	Pin Name		0	1	
1	35	SDRAM1	Clock Output Disable	Low	Active	1
0	36	SDRAM0	Clock Output Disable	Low	Active	1
Data Byte 4						
7	--	--	(Reserved)	--	--	0
6	--	--	(Reserved)	--	--	0
5	--	--	(Reserved)	--	--	0
4	--	--	(Reserved)	--	--	0
3	--	--	(Reserved)	--	--	0
2	--	--	(Reserved)	--	--	0
1	--	--	(Reserved)	--	--	0
0	--	--	(Reserved)	--	--	0
Data Byte 5						
7	--	--	(Reserved)	--	--	0
6	--	--	(Reserved)	--	--	0
5	--	--	(Reserved)	--	--	0
4	--	--	(Reserved)	--	--	0
3	--	--	(Reserved)	--	--	0
2	45	REF2	Clock Output Disable	Low	Active	1
1	1	REF1	Clock Output Disable	Low	Active	1
0	2	REF0	Clock Output Disable	Low	Active	1
Data Byte 6						
7	--	--	(Reserved)	--	--	0
6	--	--	(Reserved)	--	--	0
5	--	--	(Reserved)	--	--	0
4	--	--	(Reserved)	--	--	0
3	--	--	(Reserved)	--	--	0
2	--	--	(Reserved)	--	--	0
1	--	--	(Reserved)	--	--	0
0	--	--	(Reserved)	--	--	0

Table 5. Select Function for Data Byte 0, Bits 0:1

Function	Input Conditions		Output Conditions					
	Data Byte 0							
	Bit 1	Bit 0	CPU0:1	PCI_F, PCI1:5	SDRAM	REF0:1,	24MHZ	48MHZ
Three-state	1	1	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z
Testmode	0	1	TCLK/2[3]	TCLK/4[3]	TCLK/2[3]	TCLK[3]	TCLK/4[3]	TCLK/2[3]

Note:
3. TCLK is a test clock driven on the X1 (crystal) input during test mode.

Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

Parameter	Description	Rating	Unit
V_{DD}, V_{IN}	Voltage on any pin with respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
T_B	Ambient Temperature under Bias	–55 to +125	°C
T_A	Operating Temperature	0 to +70	°C
ESD_{PROT}	Input ESD Protection	2 (min.)	kV

DC Electrical Characteristics: T_A = 0°C to +70°C, V_{DDQ3} = 3.3V±5%, V_{DDQ2} = 2.5V±5%

Parameter	Description		Test Condition	Min.	Typ.	Max.	Unit
Supply Current							
I_{DD}	3.3V Supply Current		CPU0:1 =100 MHz[4]		260		mA
I_{DD}	2.5V Supply Current		CPU0:1 =100 MHz[4]		25		mA
Logic Inputs (All referenced to V_{DDQ3} = 3.3V)							
V_{IL}	Input Low Voltage			GND – 0.3		0.8	V
V_{IH}	Input High Voltage			2.0		V_{DD} + 0.3	V
I_{IL}	Input Low Current[5]					–25	µA
I_{IH}	Input High Current[5]					10	µA
Clock Outputs							
V_{OL}	Output Low Voltage		I_{OL} = 1 mA			50	mV
V_{OH}	Output High Voltage		I_{OH} = –1 mA	3.1			V
V_{OH}	Output High Voltage	CPU0:1, IOAPIC	I_{OH} = –1 mA	2.2			V
I_{OL}	Output Low Current:	CPU0:1	V_{OL} = 1.25V	27	57	97	mA
		PCI_F, PCI1:5	V_{OL} = 1.5V	20.5	53	139	mA
		IOAPIC	V_{OL} = 1.25V	40	85	140	mA
		REF0:1	V_{OL} = 1.5V	25	37	76	mA
		48MHz	V_{OL} = 1.5V	25	37	76	mA
		24MHz	V_{OL} = 1.5V	25	37	76	mA
I_{OH}	Output High Current	CPU0:1	V_{OH} = 1.25V	25	55	97	mA
		PCI_F, PCI1:5	V_{OH} = 1.5V	31	55	139	mA
		IOAPIC	V_{OH} = 1.25V	40	87	155	mA
		REF0:1	V_{OH} = 1.5V	27	44	94	mA
		48MHz	V_{OH} = 1.5V	27	44	94	mA
		24MHz	V_{OH} = 1.5V	25	37	76	mA

Notes:

4. All clock outputs loaded with 6" 60Ω transmission lines with 22-pF capacitors.
5. W237 logic inputs have internal pull-up devices (pull-ups not full CMOS level).

DC Electrical Characteristics: T_A = 0°C to +70°C, V_{DDQ3} = 3.3V±5%, V_{DDQ2} = 2.5V±5% (continued)

Parameter	Description	Test Condition	Min.	Typ.	Max.	Unit
Crystal Oscillator						
V_{TH}	X1 Input Threshold Voltage[6]	V_{DDQ3} = 3.3V		1.65		V
C_{LOAD}	Load Capacitance, Imposed on External Crystal[7]			14		pF
$C_{IN,X1}$	X1 Input Capacitance[8]	Pin X2 unconnected		28		pF
Pin Capacitance/Inductance						
C_{IN}	Input Pin Capacitance	Except X1 and X2			5	pF
C_{OUT}	Output Pin Capacitance				6	pF
L_{IN}	Input Pin Inductance				7	nH

AC Electrical Characteristics

T_A = 0°C to +70°C, V_{DDQ3} = 3.3V±5%, V_{DDQ2} = 2.5V± 5%, f_{XTL} = 14.31818 MHz

AC clock parameters are tested and guaranteed over stated operating conditions using the stated lump capacitive load at the clock output; Spread Spectrum clocking is disabled.

CPU Clock Outputs, CPU0:1 (Lump Capacitance Test Load = 20 pF)

Parameter	Description	Test Condition/Comments	CPU = 66.6 MHz			CPU = 100 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
t_P	Period	Measured on rising edge at 1.25V	15		15.5	10		10.5	ns
t_H	High Time	Duration of clock cycle above 2.0V	5.6			3			ns
t_L	Low Time	Duration of clock cycle below 0.4V	5.3			2.8			ns
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.0V	1		4	1		4	V/ns
t_F	Output Fall Edge Rate	Measured from 2.0V to 0.4V	1		4	1		4	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.25V	45		55	45		55	%
t_{JC}	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.25V. Maximum difference of cycle time between two adjacent cycles.			250			250	ps
t_{SK}	Output Skew	Measured on rising edge at 1.25V			175			175	ps
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		20			20		Ω

Notes:

6. X1 input threshold voltage (typical) is $V_{DD}/2$.
7. The W237 contains an internal crystal load capacitor between pin X1 and ground and another between pin X2 and ground. Total load placed on crystal is 14 pF; this includes typical stray capacitance of short PCB traces to crystal.
8. X1 input capacitance is applicable when driving X1 with an external clock source (X2 is left unconnected).

SDRAM Clock Outputs, SDRAM, SDRAM0:7 (Lump Capacitance Test Load = 30 pF)

Parameter	Description	Test Condition/Comments	CPU = 66.6 MHz			CPU = 100 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
t_P	Period	Measured on rising edge at 1.5V	15		15.5	10		15.5	ns
t_H	High Time	Duration of clock cycle above 2.4V, at min. edge rate (1.5 V/ns)	5.6			3.3			ns
t_L	Low Time	Duration of clock cycle below 0.4V, at min. edge rate (1.5 V/ns)	5.3			3.1			ns
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V	1.5		4	1.5		4	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V	1.5		4	1.5		4	V/ns
t_{PLH}	Prop Delay LH	Input edge rate faster than 1 V/ns	1		5	1		5	ns
t_{PHL}	Prop Delay HL	Input edge rate faster than 1 V/ns	1		5	1		5	ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V, at min. edge rate (1.5 V/ns)	45		55	45		55	%
t_{SK}	Output Skew	Measured on rising edge at 1.5V			250			250	ps
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		30			30		Ω

PCI Clock Outputs, PCI_F and PCI0:5 (Lump Capacitance Test Load = 30 pF)

Parameter	Description	Test Condition/Comments	CPU = 66.6/100 MHz			Unit
			Min.	Typ.	Max.	
t_P	Period	Measured on rising edge at 1.5V	30			ns
t_H	High Time	Duration of clock cycle above 2.4V	12			ns
t_L	Low Time	Duration of clock cycle below 0.4V	12			ns
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V	1		4	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V	1		4	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	%
t_{JC}	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.			250	ps
t_{SK}	Output Skew	Measured on rising edge at 1.5V			500	ps
t_O	CPU to PCI Clock Skew	Covers all CPU/PCI outputs. Measured on rising edge at 1.5V. CPU leads PCI output.	1.5		4	ns
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		30		Ω

REF0:1 Clock Output (Lump Capacitance Test Load = 20 pF)

Parameter	Description	Test Condition/Comments	CPU = 66.6/100 MHz			Unit
			Min.	Typ.	Max.	
f	Frequency, Actual	Frequency generated by crystal oscillator		14.318		MHz
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V	0.5		2	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V	0.5		2	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	%
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		40		Ω

48-MHZ Clock Output (Lump Capacitance Test Load = 20 pF)

Parameter	Description	Test Condition/Comments	CPU = 66.6/100 MHz			Unit
			Min.	Typ.	Max.	
f	Frequency, Actual	Determined by PLL divider ratio (see m/n below)		48.008		MHz
f_D	Deviation from 48 MHz	(48.008 – 48)/48		+167		ppm
m/n	PLL Ratio	(14.31818 MHz x 57/17 = 48.008 MHz)		57/17		
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V	0.5		2	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V	0.5		2	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	%
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		40		Ω

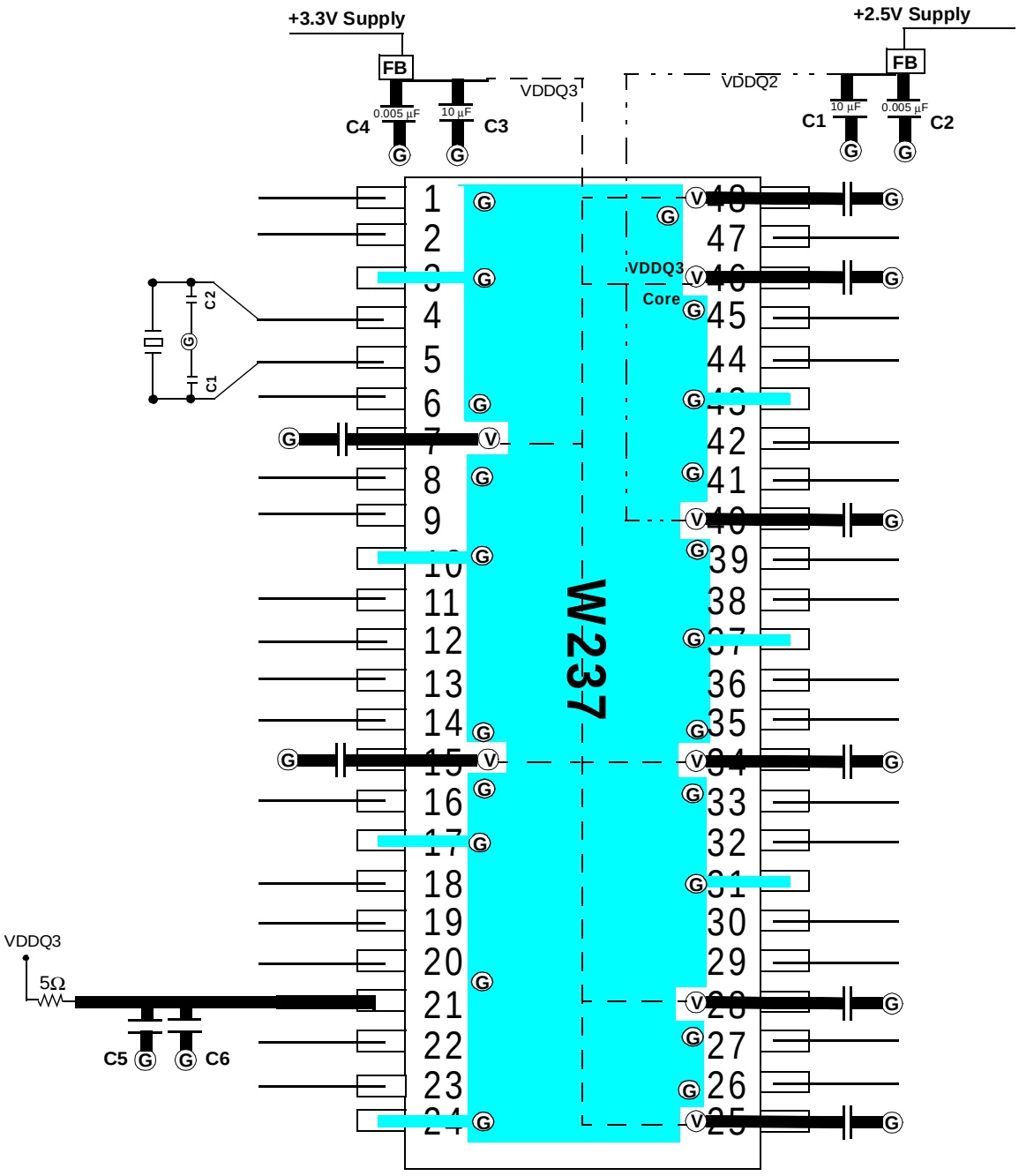
24-MHZ Clock Output (Lump Capacitance Test Load = 20 pF)

Parameter	Description	Test Condition/Comments	CPU = 66.6/100 MHz			Unit
			Min.	Typ.	Max.	
f	Frequency, Actual	Determined by PLL divider ratio (see m/n below)		24.004		MHz
f_D	Deviation from 24 MHz	(24.004 – 24)/24		+167		ppm
m/n	PLL Ratio	(14.31818 MHz x 57/34 = 24.004 MHz)		57/34		
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V	0.5		2	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V	0.5		2	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	%
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		40		Ω

Ordering Information

Ordering Code	Package Name	Package Type
W237	X	48-pin TSSOP (240 mils)

Layout Example



FB = Dale ILB1206 - 300 (300Ω @ 100 MHz)

C1 & C3 = 10–22 µF C2 & C4 = 0.005 µF C5 = 47 µF C6 = 0.1 µF

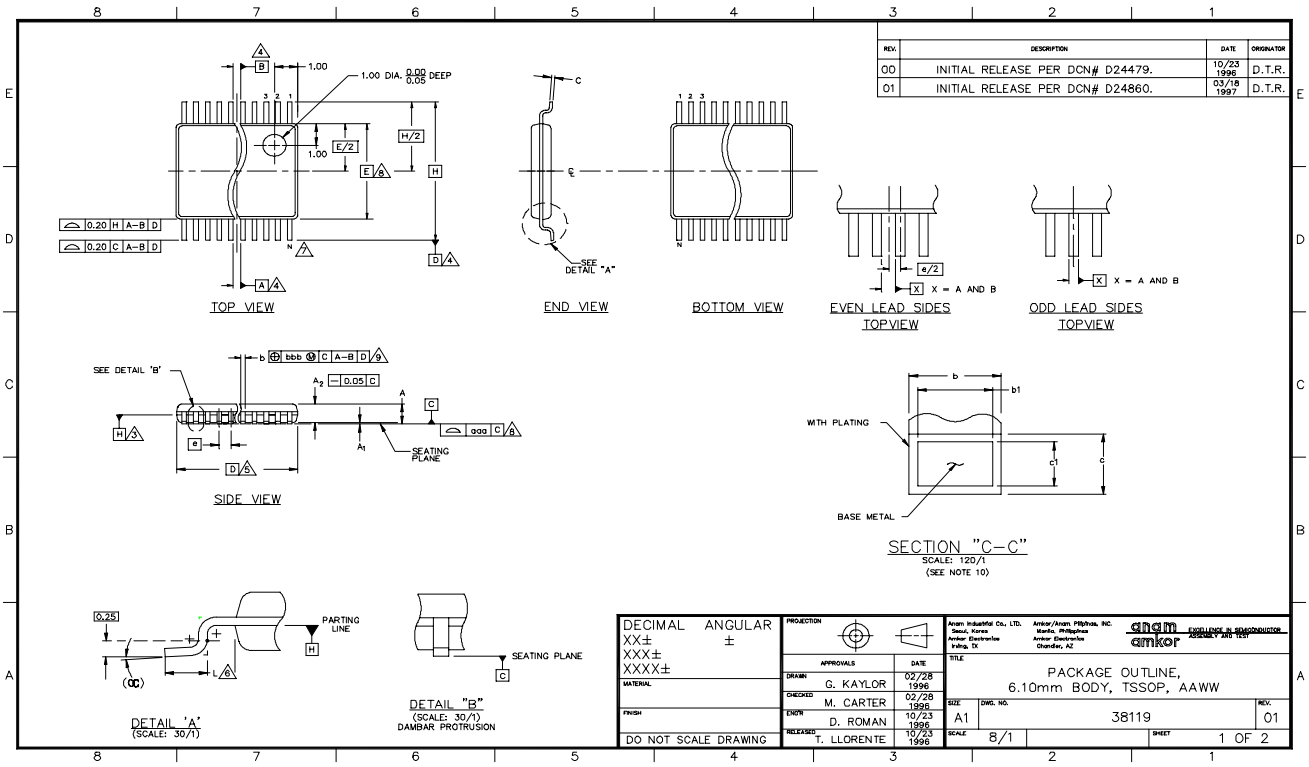
Ⓖ = VIA to GND plane layer Ⓥ =VIA to respective supply plane trace

Note: Each supply plane or strip should have a ferrite bead and capacitors

All V_{DD} by pass capacitors = 0.1 µF

Package Diagram

48-Pin Thin Shrink Small Outline Package (TSSOP, 240 mils)



THIS TABLE FOR 0.65mm PITCH

	COMMON DIMENSIONS			NOTE	VARIATIONS	5			7 N
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
A	—	—	1.10		DB	9.60	9.70	9.80	28
A_1	0.05	—	0.15		DC	10.90	11.00	11.10	32
A_2	0.80	1.00	1.05		* DF	12.40	12.50	12.60	38
aaa		0.10			DE	13.90	14.00	14.10	40
b	0.19	-	0.30	9					
b1	0.19	0.22	0.25						
bbb		0.10							
c	0.09	-	0.20						
c1	0.09	-	0.16						
D	SEE VARIATIONS			5					
E	6.00	6.10	6.20	5					
e		0.65 BSC							
H		8.10 BSC							
L	0.50	0.60	0.75	6					
N	SEE VARIATIONS			7					
⌀	0°	—	8°						

* - THIS VARIATION NOT REGISTERED WITH JEDEC.

THIS TABLE FOR 0.50mm PITCH

	COMMON DIMENSIONS			NOTE	VARIATIONS	5			7 N
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
A	—	—	1.10		ED	12.40	12.50	12.60	48
A_1	0.05	—	0.15		EE	13.90	14.00	14.10	56
A_2	0.80	1.00	1.05		EF*	16.90	17.00	17.10	64
aaa		0.10							
b	0.17	-	0.27	9	*DESIGNED BUT NOT TOOLED				
b1	0.17	0.20	0.23						
bbb		0.08							
c	0.09	-	0.20						
c1	0.09	0.127	0.16						
D	SEE VARIATIONS			5					
E	6.00	6.10	6.20	5					
e		0.50 BSC							
H		8.10 BSC							
L	0.50	0.60	0.75	6					
N	SEE VARIATIONS			7					
⌀	0°	—	8°						

THIS TABLE FOR 0.40mm PITCH

	COMMON DIMENSIONS			NOTE	VARIATIONS	5			7 N
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
A	—	—	1.10		FF	16.90	17.00	17.10	80
A_1	0.05	—	0.15						
A_2	0.80	1.00	1.05						
aaa		0.08							
b	0.13	-	0.23	9					
b1	0.13	0.16	0.23						
bbb		0.07							
c	0.09	-	0.20						
c1	0.09	0.127	0.16						
D	SEE VARIATIONS			5					
E	6.00	6.10	6.20	5					
e		0.40 BSC							
H		8.10 BSC							
L	0.50	0.60	0.75	6					
N	SEE VARIATIONS			7					
⌀	0°	—	8°						

NOTES:
1. DIE THICKNESS ALLOWABLE IS 0.279±0.0127 (.0110±.0005 INCHES)
2. DIMENSIONING & TOLERANCES PER ASME. Y14.5M-1994.
3. DATUM PLANE H LOCATED AT MOLD PARTING LINE AND CONCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
4. DATUMS A-B AND D TO BE DETERMINED WHERE CENTERLINE BETWEEN LEADS EXITS PLASTIC BODY AT DATUM PLANE H.
5. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, AND ARE MEASURED AT THE BOTTOM PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm ON D AND 0.25mm ON E PER SIDE.
6. DIMENSION IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
7. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
8. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN 0.076mm AT SEATING PLANE.
9. THE LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND AN ADJACENT LEAD TO BE 0.10MM FOR 0.65MM PITCH, 0.08MM FOR 0.50MM PITCH AND 0.07MM FOR 0.40MM PITCH PACKAGES.
10. SEE DETAIL 'B' AND SECTION "C-C". SECTION "C-C" TO BE DETERMINED AT 0.10 TO 0.25 MM FROM THE LEAD TIP.
11. CONTROLLING DIMENSION: MILLIMETERS.
12. THIS PART IS COMPLIANT WITH JEDEC SPECIFICATION MO-153, VARIATIONS DB, DC, DE, ED, EE, AND FE.

ALL DIMENSIONS IN MILLIMETERS