

intersil

ICL7106, ICL7107, ICL7106S, ICL7107S

January 1998

**3¹/₂ Digit,
LCD/LED Display, A/D Converters**

Features

- Guaranteed Zero Reading for 0V Input on All Scales
- True Polarity at Zero for Precise Null Detection
- 1pA Typical Input Current
- True Differential Input and Reference, Direct Display Drive
 - LCD ICL7106, LED ICL7107
- Low Noise - Less Than 15μV_{p-p}
- On Chip Clock and Reference
- Low Power Dissipation - Typically Less Than 10mW
- No Additional Active Circuits Required
- Enhanced Display Stability (ICL7106S, ICL7107S)

Ordering Information

PART NO.	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
ICL7106CPL	0 to 70	40 Ld PDIP	E40.6
ICL7106RCPL	0 to 70	40 Ld PDIP (Note)	E40.6
ICL7106CM44	0 to 70	44 Ld MQFP	Q44.10x10
ICL7106SCPL	0 to 70	40 Ld PDIP	E40.6
ICL7107SCPL	0 to 70	40 Ld PDIP	E40.6
ICL7107CPL	0 to 70	40 Ld PDIP	E40.6
ICL7107RCPL	0 to 70	40 Ld PDIP (Note)	E40.6
ICL7107CM44	0 to 70	44 Ld MQFP	Q44.10x10

NOTE: "R" indicates device with reversed leads for mounting to PC board underside. "S" indicates enhanced stability.

Description

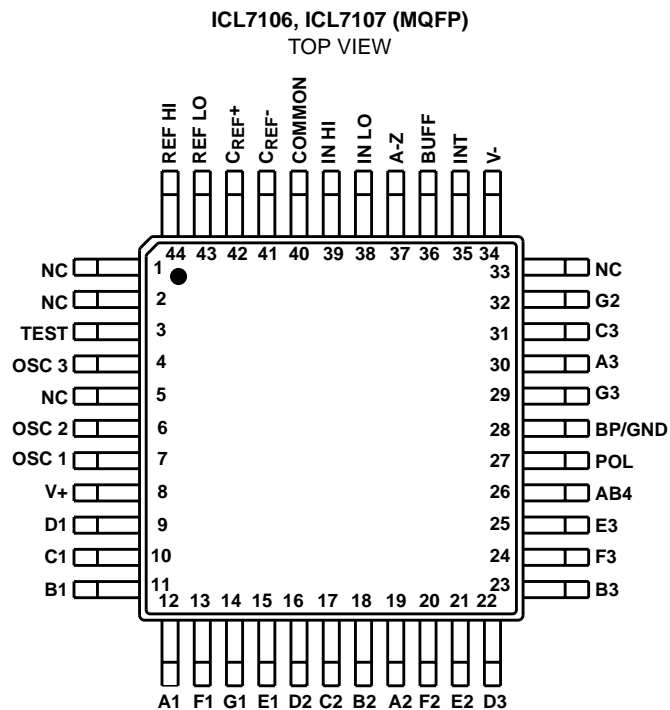
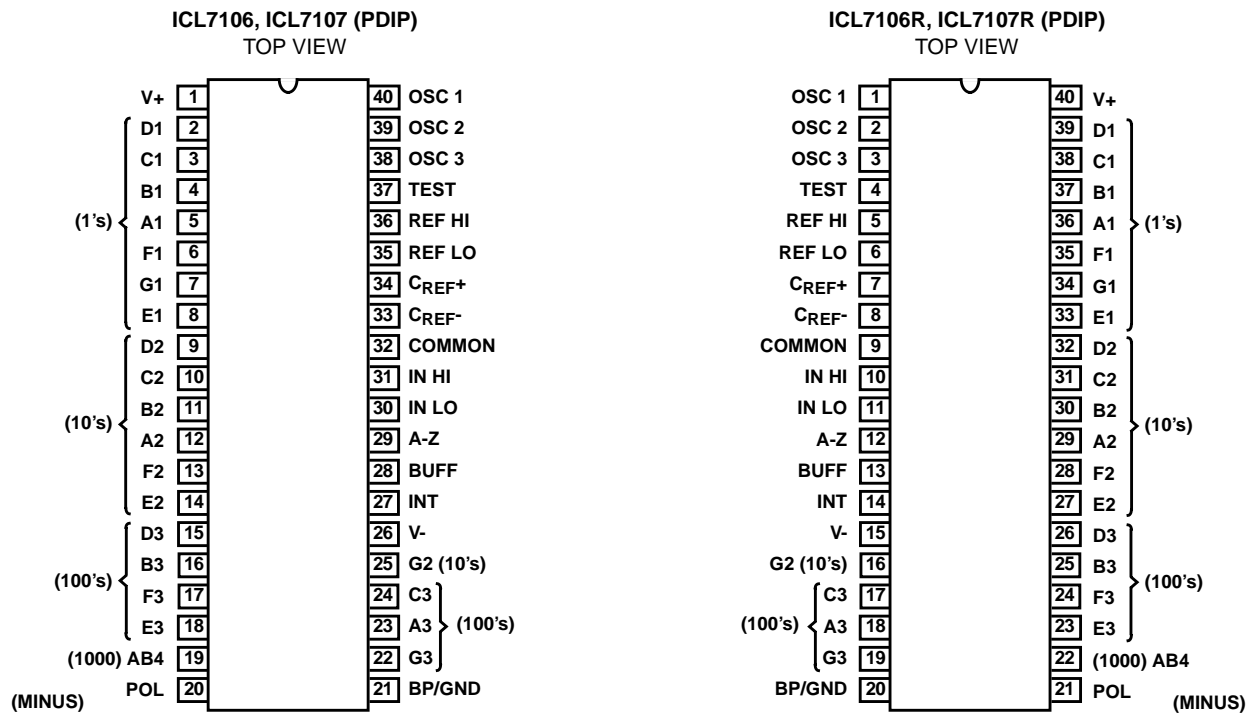
The Intersil ICL7106 and ICL7107 are high performance, low power, 3¹/₂ digit A/D converters. Included are seven segment decoders, display drivers, a reference, and a clock. The ICL7106 is designed to interface with a liquid crystal display (LCD) and includes a multiplexed backplane drive; the ICL7107 will directly drive an instrument size light emitting diode (LED) display.

The ICL7106 and ICL7107 bring together a combination of high accuracy, versatility, and true economy. It features auto-zero to less than 10μV, zero drift of less than 1μV/°C, input bias current of 10pA (Max), and rollover error of less than one count. True differential inputs and reference are useful in all systems, but give the designer an uncommon advantage when measuring load cells, strain gauges and other bridge type transducers. Finally, the true economy of single power supply operation (ICL7106), enables a high performance panel meter to be built with the addition of only 10 passive components and a display.



ICL7106, ICL7107, ICL7106S, ICL7107S

Pinouts



ICL7106, ICL7107, ICL7106S, ICL7107S

Absolute Maximum Ratings

Supply Voltage	
ICL7106, V+ to V-	15V
ICL7107, V+ to GND	6V
ICL7107, V- to GND	-9V
Analog Input Voltage (Either Input) (Note 1)	V+ to V-
Reference Input Voltage (Either Input)	V+ to V-
Clock Input	
ICL7106	TEST to V+
ICL7107	GND to V+

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
PDIP Package	50
MQFP Package	80
Maximum Junction Temperature	150°C
Maximum Storage Temperature Range	-65°C to 150°C
Maximum Lead Temperature (Soldering 10s)	300°C
(MQFP - Lead Tips Only)	

Operating Conditions

Temperature Range 0°C to 70°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Input voltages may exceed the supply voltages provided the input current is limited to $\pm 100\mu\text{A}$.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications (Note 3)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYSTEM PERFORMANCE					
Zero Input Reading	$V_{IN} = 0.0\text{V}$, Full Scale = 200mV	-000.0	± 000.0	+000.0	Digital Reading
Stability (Last Digit) (ICL7106S, ICL7107S Only)	Fixed Input Voltage (Note 7)	-000.0	± 000.0	+000.0	Digital Reading
Ratiometric Reading	$V_{IN} = V_{REF}$, $V_{REF} = 100\text{mV}$	999	999/1000	1000	Digital Reading
Rollover Error	$-V_{IN} = +V_{IN} \cong 200\text{mV}$ Difference in Reading for Equal Positive and Negative Inputs Near Full Scale	-	± 0.2	± 1	Counts
Linearity	Full Scale = 200mV or Full Scale = 2V Maximum Deviation from Best Straight Line Fit (Note 6)	-	± 0.2	± 1	Counts
Common Mode Rejection Ratio	$V_{CM} = 1\text{V}$, $V_{IN} = 0\text{V}$, Full Scale = 200mV (Note 6)	-	50	-	$\mu\text{V/V}$
Noise	$V_{IN} = 0\text{V}$, Full Scale = 200mV (Peak-To-Peak Value Not Exceeded 95% of Time)	-	15	-	μV
Leakage Current Input	$V_{IN} = 0$ (Note 6)	-	1	10	pA
Zero Reading Drift	$V_{IN} = 0$, 0°C To 70°C (Note 6)	-	0.2	1	$\mu\text{V}/^\circ\text{C}$
Scale Factor Temperature Coefficient	$V_{IN} = 199\text{mV}$, 0°C To 70°C, (Ext. Ref. 0ppm/°C) (Note 6)	-	1	5	ppm/°C
End Power Supply Character V+ Supply Current	$V_{IN} = 0$ (Does Not Include LED Current for ICL7107)	-	1.0	1.8	mA
End Power Supply Character V- Supply Current	ICL7107 Only	-	0.6	1.8	mA
COMMON Pin Analog Common Voltage	25k Ω Between Common and Positive Supply (With Respect to + Supply)	2.4	3.0	3.2	V
Temperature Coefficient of Analog Common	25k Ω Between Common and Positive Supply (With Respect to + Supply)	-	80	-	ppm/°C
DISPLAY DRIVER ICL7106 ONLY					
Peak-To-Peak Segment Drive Voltage	V+ = to V- = 9V (Note 5)	4	5.5	6	V
Peak-To-Peak Backplane Drive Voltage					

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Electrical Specifications (Note 3) (Continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DISPLAY DRIVER ICL7107 ONLY					
Segment Sinking Current (Except Pins 19 and 20)	V+ = 5V, Segment Voltage = 3V	5	8	-	mA
Pin 19 Only		10	16	-	mA
Pin 20 Only		4	7	-	mA

NOTES:

- Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
- Unless otherwise noted, specifications apply to both the ICL7106 and ICL7107 at $T_A = 25^\circ\text{C}$, $f_{\text{CLOCK}} = 48\text{kHz}$. ICL7106 is tested in the circuit of Figure 1. ICL7107 is tested in the circuit of Figure 2.
- Back plane drive is in phase with segment drive for 'off' segment, 180 degrees out of phase for 'on' segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV.
- Not tested, guaranteed by design.
- Sample Tested.

Typical Applications and Test Circuits

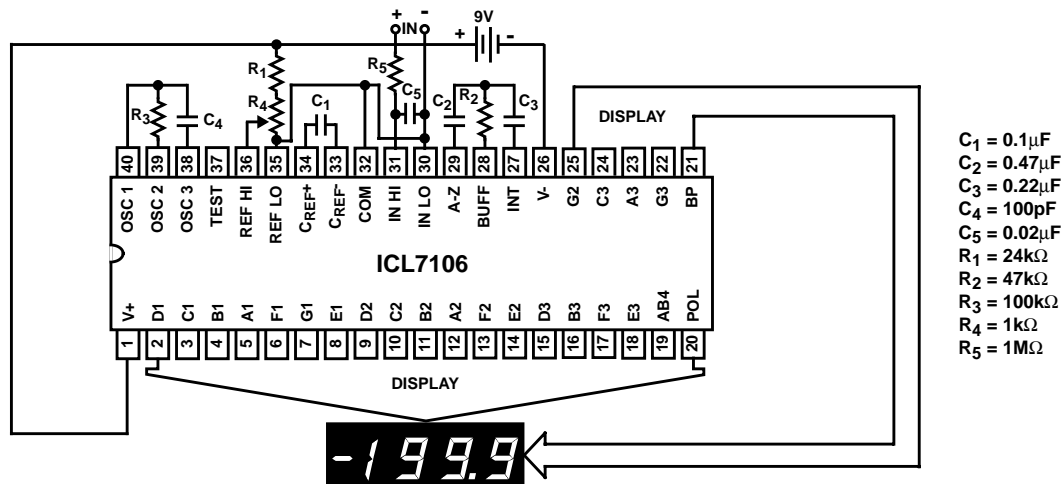


FIGURE 1. ICL7106 TEST CIRCUIT AND TYPICAL APPLICATION WITH LCD DISPLAY COMPONENTS SELECTED FOR 200mV FULL SCALE

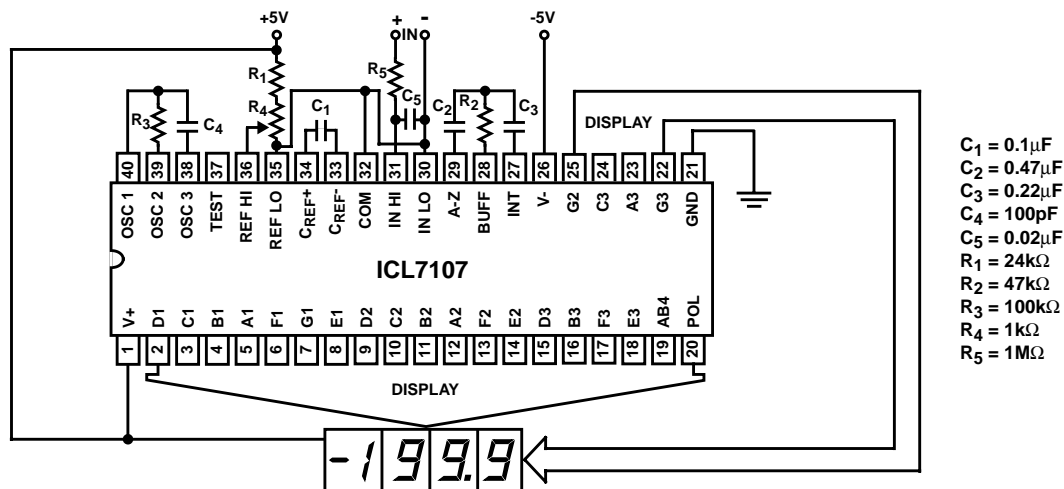


FIGURE 2. ICL7107 TEST CIRCUIT AND TYPICAL APPLICATION WITH LED DISPLAY COMPONENTS SELECTED FOR 200mV FULL SCALE

ICL7106, ICL7107, ICL7106S, ICL7107S

Design Information Summary Sheet

- **OSCILLATOR FREQUENCY**

$$f_{OSC} = 0.45/RC$$

$$C_{OSC} > 50pF; R_{OSC} > 50k\Omega$$

$$f_{OSC} (Typ) = 48kHz$$

- **OSCILLATOR PERIOD**

$$t_{OSC} = RC/0.45$$

- **INTEGRATION CLOCK FREQUENCY**

$$f_{CLOCK} = f_{OSC}/4$$

- **INTEGRATION PERIOD**

$$t_{INT} = 1000 \times (4/f_{OSC})$$

- **60/50Hz REJECTION CRITERION**

$$t_{INT}/t_{60Hz} \text{ or } t_{INT}/t_{50Hz} = \text{Integer}$$

- **OPTIMUM INTEGRATION CURRENT**

$$I_{INT} = 4\mu A$$

- **FULL SCALE ANALOG INPUT VOLTAGE**

$$V_{INFS} (Typ) = 200mV \text{ or } 2V$$

- **INTEGRATE RESISTOR**

$$R_{INT} = \frac{V_{INFS}}{I_{INT}}$$

- **INTEGRATE CAPACITOR**

$$C_{INT} = \frac{(t_{INT})(I_{INT})}{V_{INT}}$$

- **INTEGRATOR OUTPUT VOLTAGE SWING**

$$V_{INT} = \frac{(t_{INT})(I_{INT})}{C_{INT}}$$

- **V_{INT} MAXIMUM SWING:**

$$(V- + 0.5V) < V_{INT} < (V+ - 0.5V), V_{INT} (Typ) = 2V$$

- **DISPLAY COUNT**

$$COUNT = 1000 \times \frac{V_{IN}}{V_{REF}}$$

- **CONVERSION CYCLE**

$$t_{CYC} = t_{CLOCK} \times 4000$$

$$t_{CYC} = t_{OSC} \times 16,000$$

when $f_{OSC} = 48kHz$; $t_{CYC} = 333ms$

- **COMMON MODE INPUT VOLTAGE**

$$(V- + 1V) < V_{IN} < (V+ - 0.5V)$$

- **AUTO-ZERO CAPACITOR**

$$0.01\mu F < C_{AZ} < 1\mu F$$

- **REFERENCE CAPACITOR**

$$0.1\mu F < C_{REF} < 1\mu F$$

- **V_{COM}**

Biased between V_i and V_- .

- **V_{COM} \cong V₊ - 2.8V**

Regulation lost when V_+ to $V_- < \cong 6.8V$
If V_{COM} is externally pulled down to $(V_+ \text{ to } V_-)/2$, the V_{COM} circuit will turn off.

- **ICL7106 POWER SUPPLY: SINGLE 9V**

$V_+ - V_- = 9V$
Digital supply is generated internally
 $V_{GND} \cong V_+ - 4.5V$

- **ICL7106 DISPLAY: LCD**

Type: Direct drive with digital logic supply amplitude.

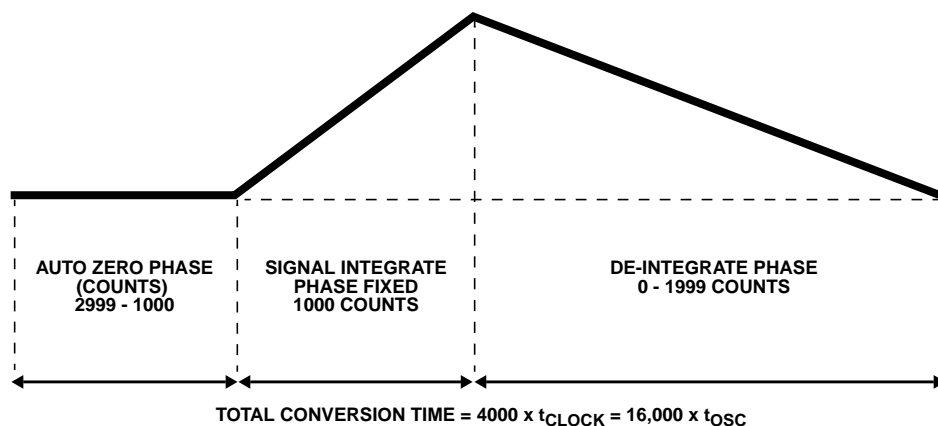
- **ICL7107 POWER SUPPLY: DUAL $\pm 5.0V$**

$V_+ = +5V$ to GND
 $V_- = -5V$ to GND
Digital Logic and LED driver supply V_+ to GND

- **ICL7107 DISPLAY: LED**

Type: Non-Multiplexed Common Anode

Typical Integrator Amplifier Output Waveform (INT Pin)



ICL7106, ICL7107, ICL7106S, ICL7107S

Detailed Description

Analog Section

Figure 3 shows the Analog Section for the ICL7106 and ICL7107. Each measurement cycle is divided into three phases. They are (1) auto-zero (A-Z), (2) signal integrate (INT) and (3) de-integrate (DE).

Auto-Zero Phase

During auto-zero three things happen. First, input high and low are disconnected from the pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than $10\mu\text{V}$.

Signal Integrate Phase

During signal integrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide common mode range: up to 1V from either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, IN LO can be tied to analog COMMON to establish the correct common mode voltage. At

the end of this phase, the polarity of the integrated signal is determined.

De-Integrate Phase

The final phase is de-integrate, or reference integrate. Input low is internally connected to analog COMMON and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. Specifically the digital reading displayed is:

$$\text{DISPLAY COUNT} = 1000 \left(\frac{V_{\text{IN}}}{V_{\text{REF}}} \right).$$

Differential Input

The input can accept differential voltages anywhere within the common mode range of the input amplifier, or specifically from 0.5V below the positive supply to 1V above the negative supply. In this range, the system has a CMRR of 86dB typical. However, care must be exercised to assure the integrator output does not saturate. A worst case condition would be a large positive common mode voltage with a near full scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator output swing can be reduced to less than the recommended 2V full scale swing with little loss of accuracy. The integrator output can swing to within 0.3V of either supply without loss of linearity.

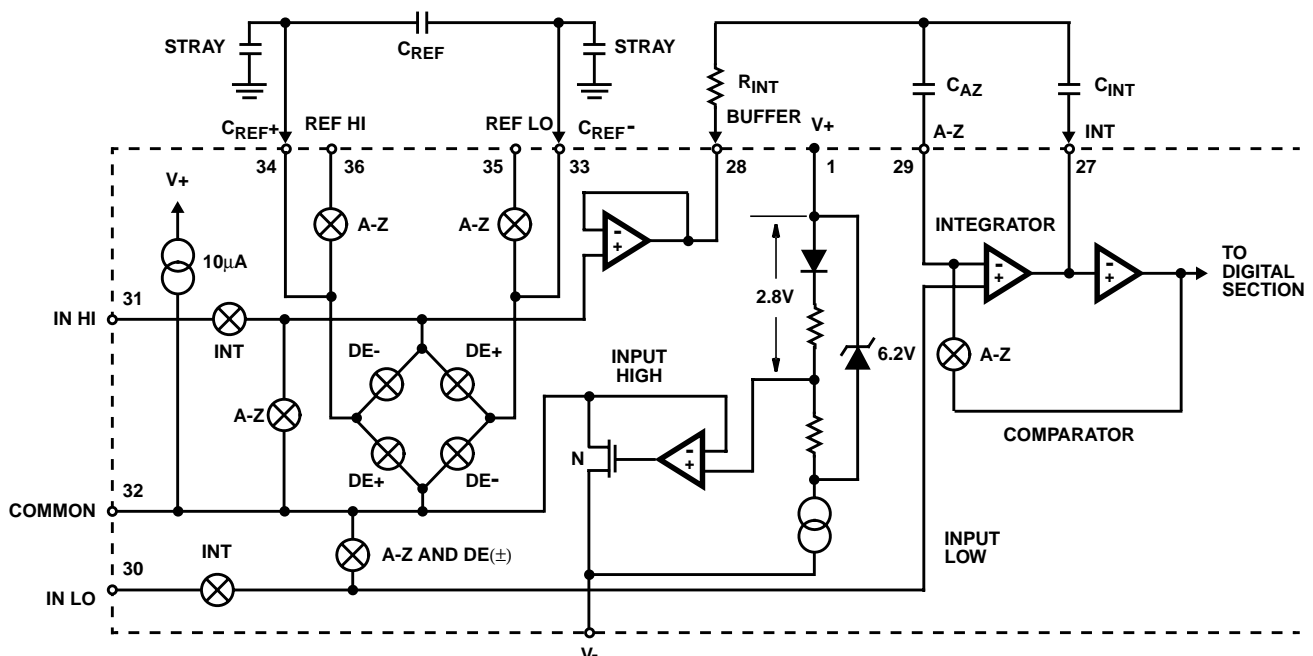


FIGURE 3. ANALOG SECTION OF ICL7106 AND ICL7107

ICL7106, ICL7107, ICL7106S, ICL7107S

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common mode error is a roll-over voltage caused by the reference capacitor losing or gaining charge to stray capacity on its nodes. If there is a large common mode voltage, the reference capacitor can gain charge (increase voltage) when called up to de-integrate a positive signal but lose charge (decrease voltage) when called up to de-integrate a negative input signal. This difference in reference for positive or negative input voltage will give a roll-over error. However, by selecting the reference capacitor such that it is large enough in comparison to the stray capacitance, this error can be held to less than 0.5 count worst case. (See Component Value Selection.)

Analog COMMON

This pin is included primarily to set the common mode voltage for battery operation (ICL7106) or for any system where the input signals are floating with respect to the power supply. The COMMON pin sets a voltage that is approximately 2.8V more negative than the positive supply. This is selected to give a minimum end-of-life battery voltage of about 6V. However, analog COMMON has some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate ($>7V$), the COMMON voltage will have a low voltage coefficient ($0.001\%/V$), low output impedance ($\approx 15\Omega$), and a temperature coefficient typically less than $80\text{ppm}/^\circ\text{C}$.

The limitations of the on chip reference should also be recognized, however. With the ICL7107, the internal heating which results from the LED drivers can cause some degradation in performance. Due to their higher thermal resistance, plastic parts are poorer in this respect than ceramic. The combination of reference Temperature Coefficient (TC), internal chip dissipation, and package thermal resistance can increase noise near full scale from $25\mu V$ to $80\mu V_{P-P}$. Also the linearity in going from a high dissipation count such as 1000 (20 segments on) to a low dissipation count such as 1111 (8 segments on) can suffer by a count or more. Devices with a positive TC reference may require several counts to pull out of an over-range condition. This is because over-range is a low dissipation mode, with the three least significant digits blanked. Similarly, units with a negative TC may cycle between over-range and a non-over-range count as the die alternately heats and cools. All these problems are of course eliminated if an external reference is used.

The ICL7106, with its negligible dissipation, suffers from none of these problems. In either case, an external reference can easily be added, as shown in Figure 4.

Analog COMMON is also used as the input low return during auto-zero and de-integrate. If IN LO is different from analog COMMON, a common mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications IN LO will be set at a fixed known voltage (power supply common for instance). In this application, analog COMMON should be tied to the same point, thus removing the common mode voltage from the converter. The same holds true for the reference voltage. If reference can be conveniently tied to analog COMMON, it

should be since this removes the common mode voltage from the reference system.

Within the IC, analog COMMON is tied to an N-Channel FET that can sink approximately 30mA of current to hold the voltage 2.8V below the positive supply (when a load is trying to pull the common line positive). However, there is only $10\mu A$ of source current, so COMMON may easily be tied to a more negative voltage thus overriding the internal reference.

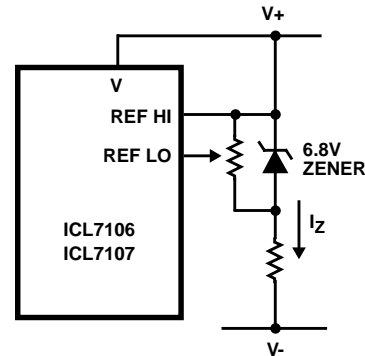


FIGURE 4A.

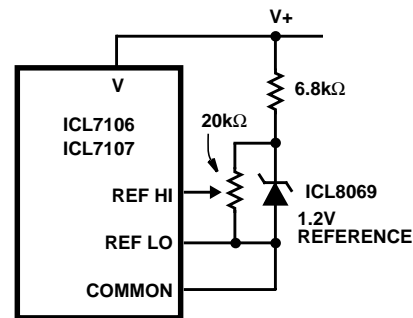


FIGURE 4B.

FIGURE 4. USING AN EXTERNAL REFERENCE

TEST

The TEST pin serves two functions. On the ICL7106 it is coupled to the internally generated digital supply through a 500Ω resistor. Thus it can be used as the negative supply for externally generated segment drivers such as decimal points or any other presentation the user may want to include on the LCD display. Figures 5 and 6 show such an application. No more than a 1mA load should be applied.

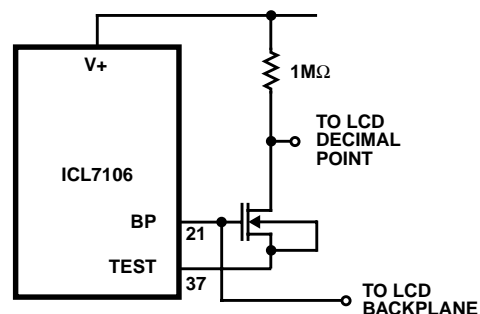


FIGURE 5. SIMPLE INVERTER FOR FIXED DECIMAL POINT

ICL7106, ICL7107, ICL7106S, ICL7107S

The second function is a “lamp test”. When TEST is pulled high (to V+) all segments will be turned on and the display should read “1888”. The TEST pin will sink about 15mA under these conditions.

CAUTION: In the lamp test mode, the segments have a constant DC voltage (no square-wave). This may burn the LCD display if maintained for extended periods.

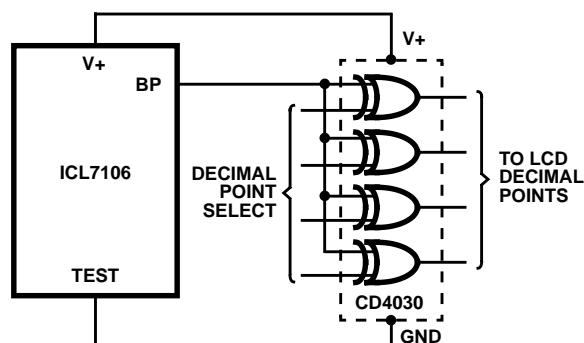


FIGURE 6. EXCLUSIVE 'OR' GATE FOR DECIMAL POINT DRIVE

Digital Section

Figures 7 and 8 show the digital section for the ICL7106 and ICL7107, respectively. In the ICL7106, an internal digital ground is generated from a 6V Zener diode and a large P-Channel source follower. This supply is made stiff to absorb the relative large capacitive currents when the back plane (BP) voltage is switched. The BP frequency is the clock frequency divided by 800. For three readings/sec., this is a 60Hz square wave with a nominal amplitude of 5V. The segments are driven at the same frequency and amplitude and are in phase with BP when OFF, but out of phase when ON. In all cases negligible DC voltage exists across the segments.

Figure 8 is the Digital Section of the ICL7107. It is identical to the ICL7106 except that the regulated supply and back plane drive have been eliminated and the segment drive has been increased from 2mA to 8mA, typical for instrument size common anode LED displays. Since the 1000 output (pin 19) must sink current from two LED segments, it has twice the drive capability or 16mA.

In both devices, the polarity indication is “on” for negative analog inputs. If IN LO and IN HI are reversed, this indication can be reversed also, if desired.

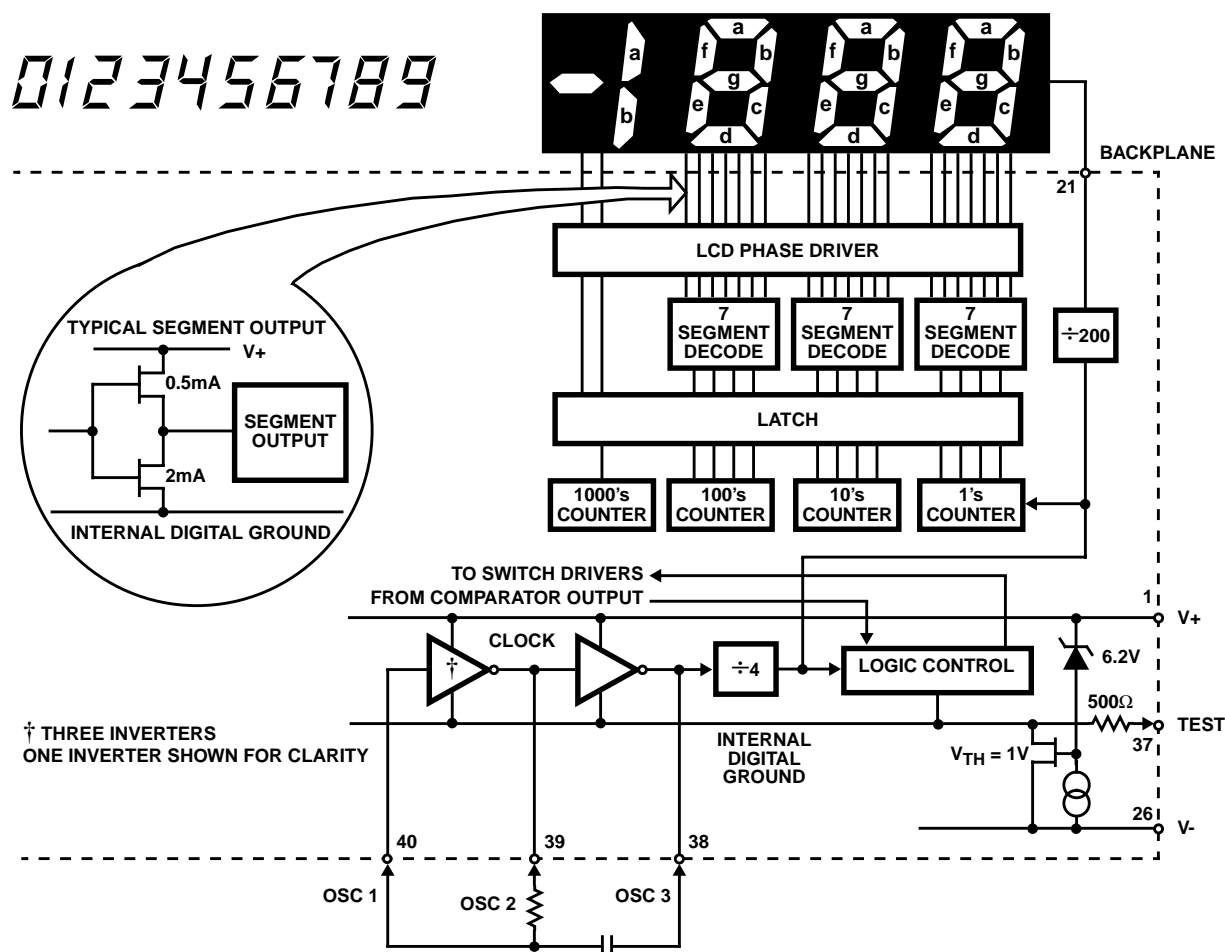


FIGURE 7. ICL7106 DIGITAL SECTION

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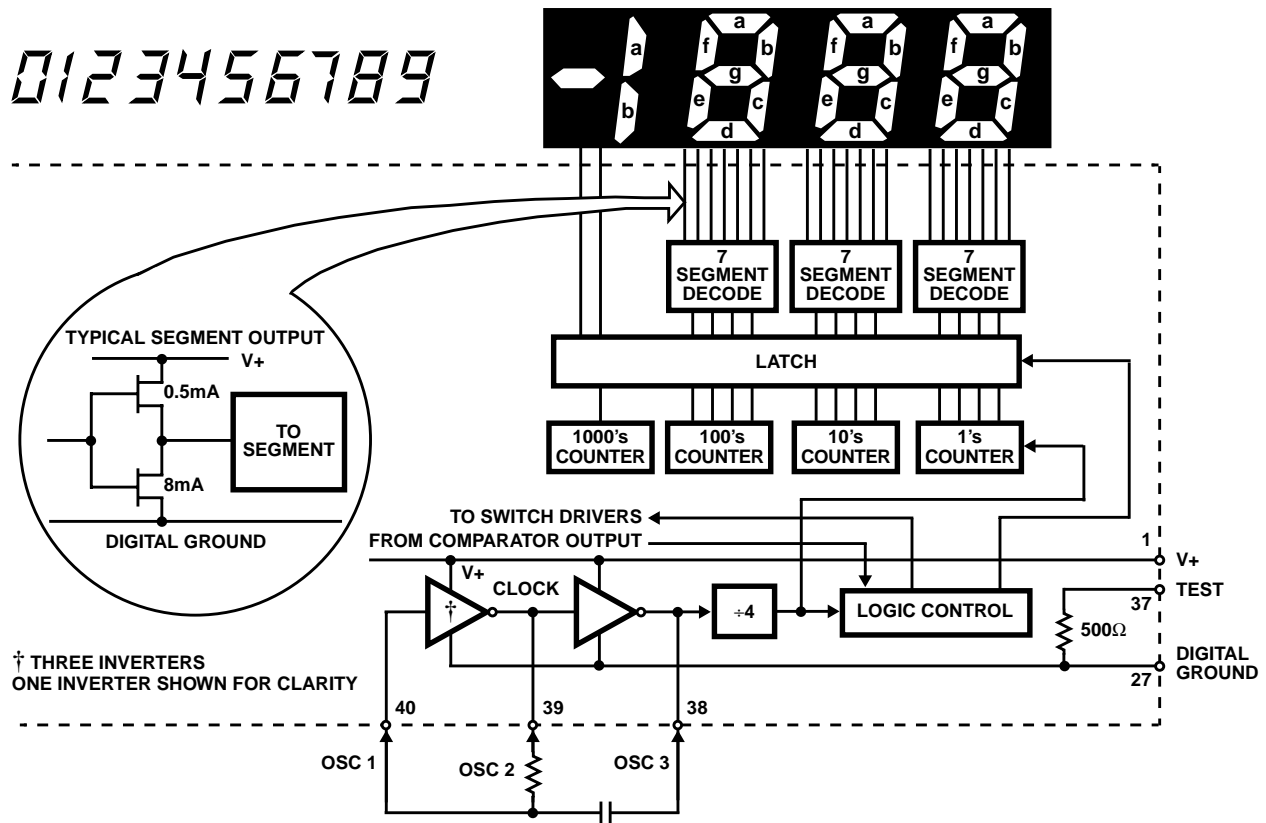


FIGURE 8. ICL7107 DIGITAL SECTION

System Timing

Figure 9 shows the clocking arrangement used in the ICL7106 and ICL7107. Two basic clocking arrangements can be used:

1. Figure 9A. An external oscillator connected to pin 40.
2. Figure 9B. An R-C oscillator using all three pins.

The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the three convert-cycle phases. These are signal integrate (1000 counts), reference de-integrate (0 to 2000 counts) and auto-zero (1000 to 3000 counts). For signals less than full scale, auto-zero gets the unused portion of reference de-integrate. This makes a complete measure cycle of 4,000 counts (16,000 clock pulses) independent of input voltage. For three readings/second, an oscillator frequency of 48kHz would be used.

To achieve maximum rejection of 60Hz pickup, the signal integrate cycle should be a multiple of 60Hz. Oscillator frequencies of 240kHz, 120kHz, 80kHz, 60kHz, 48kHz, 40kHz, $33\frac{1}{3}$ kHz, etc. should be selected. For 50Hz rejection, Oscillator frequencies of 200kHz, 100kHz, $66\frac{2}{3}$ kHz, 50kHz, 40kHz, etc. would be suitable. Note that 40kHz (2.5 readings/second) will reject both 50Hz and 60Hz (also 400Hz and 440Hz).

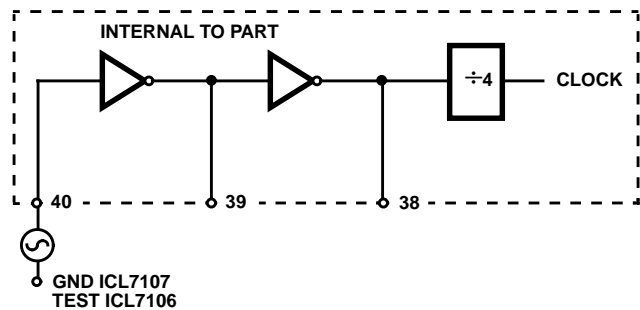


FIGURE 9A.

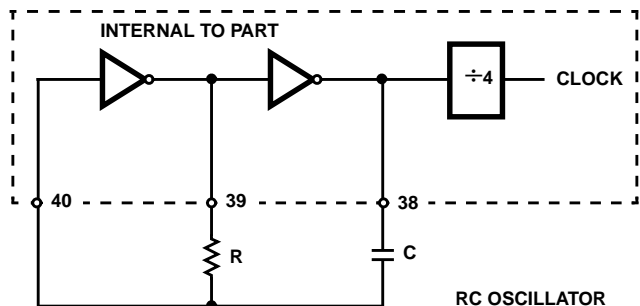


FIGURE 9B.

FIGURE 9. CLOCK CIRCUITS

FIGURE 10. GENERATING NEGATIVE SUPPLY FROM +5V

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Typical Applications

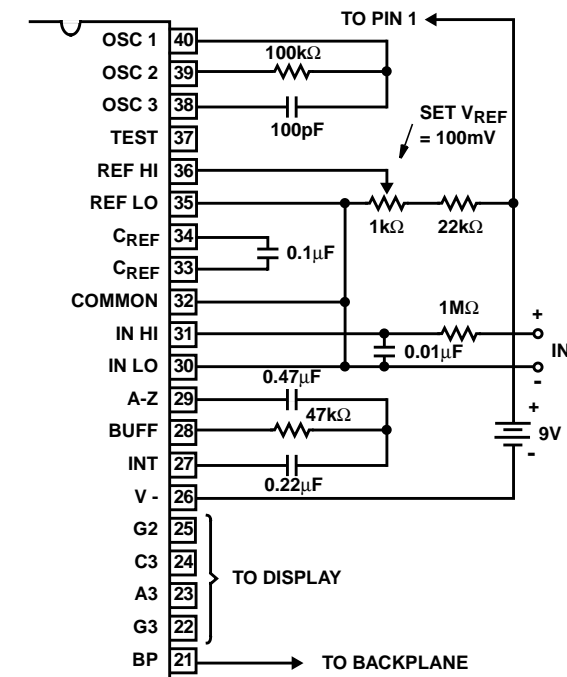
The ICL7106 and ICL7107 may be used in a wide variety of configurations. The circuits which follow show some of the possibilities, and serve to illustrate the exceptional versatility of these A/D converters.

The following application notes contain very useful information on understanding and applying this part and are available from Intersil Corporation.

Application Notes

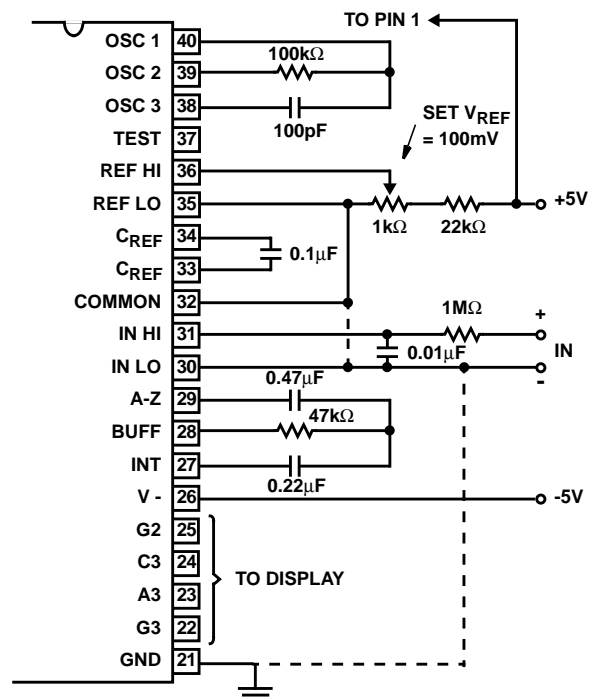
NOTE #	DESCRIPTION	AnswerFAX DOC. #
AN016	"Selecting A/D Converters"	9016
AN017	"The Integrating A/D Converter"	9017
AN018	"Do's and Don'ts of Applying A/D Converters"	9018
AN023	"Low Cost Digital Panel Meter Designs"	9023
AN032	"Understanding the Auto-Zero and Common Mode Performance of the ICL7136/7/9 Family"	9032
AN046	"Building a Battery-Operated Auto Ranging DVM with the ICL7106"	9046
AN052	"Tips for Using Single Chip $3\frac{1}{2}$ Digit A/D Converters"	9052

Typical Applications



Values shown are for 200mV full scale, 3 readings/sec., floating supply voltage (9V battery).

FIGURE 11. ICL7106 USING THE INTERNAL REFERENCE

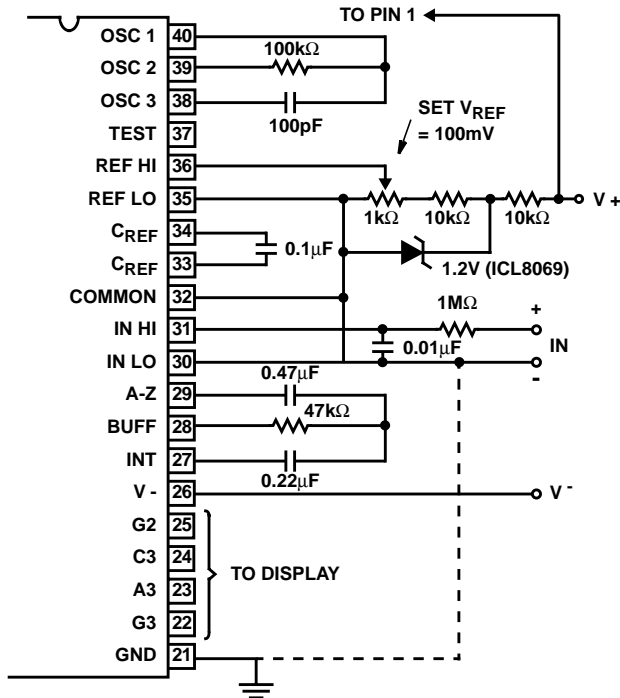


Values shown are for 200mV full scale, 3 readings/sec. IN LO may be tied to either COMMON for inputs floating with respect to supplies, or GND for single ended inputs. (See discussion under Analog COMMON.)

FIGURE 12. ICL7107 USING THE INTERNAL REFERENCE

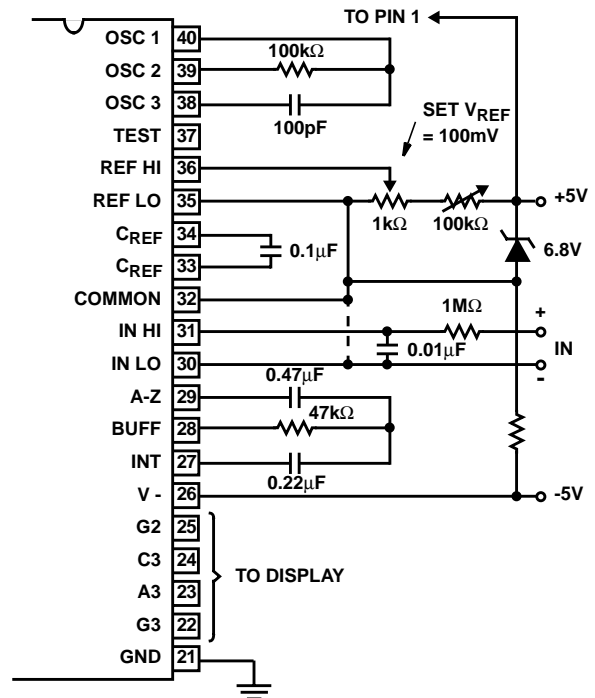
ICL7106, ICL7107, ICL7106S, ICL7107S

Typical Applications (Continued)



IN LO is tied to supply COMMON establishing the correct common mode voltage. If COMMON is not shorted to GND, the input voltage may float with respect to the power supply and COMMON acts as a pre-regulator for the reference. If COMMON is shorted to GND, the input is single ended (referred to supply GND) and the pre-regulator is overridden.

FIGURE 13. ICL7107 WITH AN EXTERNAL BAND-GAP REFERENCE (1.2V TYPE)



Since low TC zeners have breakdown voltages ~ 6.8V, diode must be placed across the total supply (10V). As in the case of Figure 14, IN LO may be tied to either COMMON or GND.

FIGURE 14. ICL7107 WITH ZENER DIODE REFERENCE

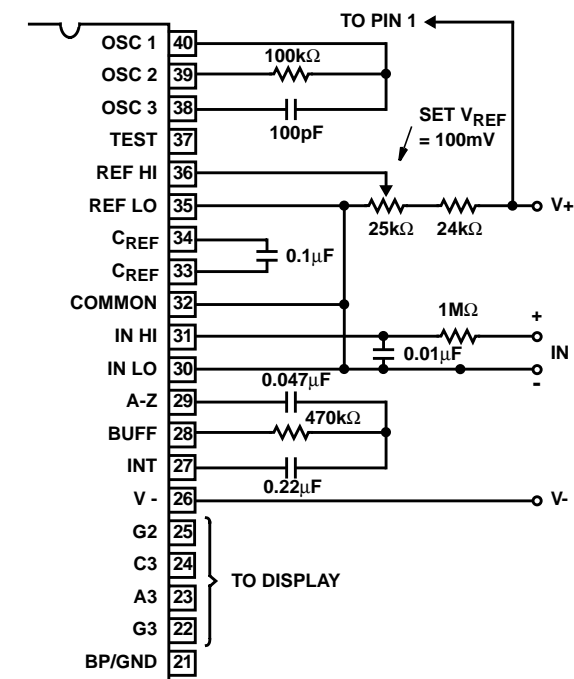
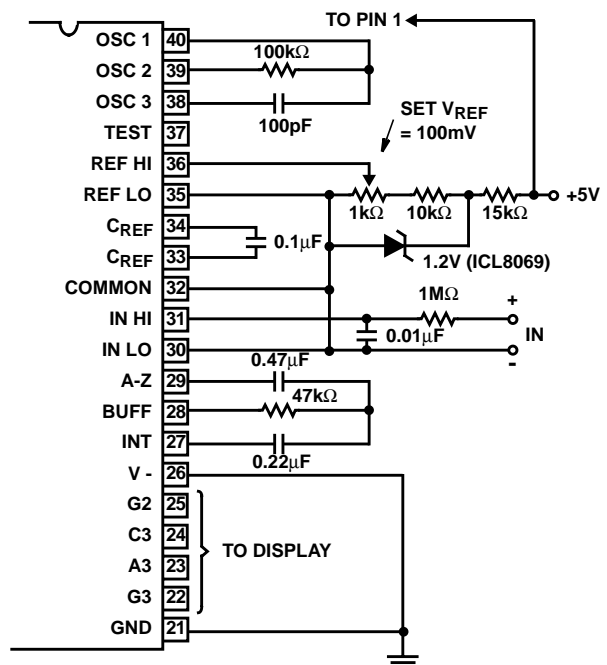


FIGURE 15. ICL7106 AND ICL7107: RECOMMENDED COMPONENT VALUES FOR 2V FULL SCALE

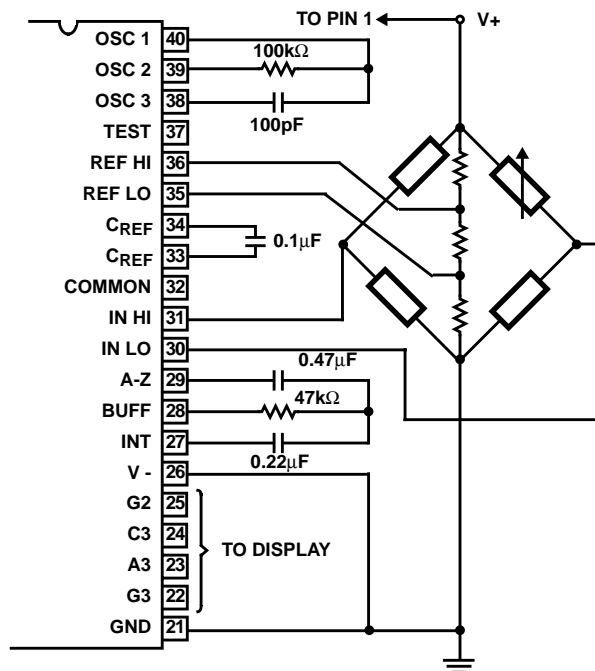


An external reference must be used in this application, since the voltage between V+ and V- is insufficient for correct operation of the internal reference.

FIGURE 16. ICL7107 OPERATED FROM SINGLE +5V

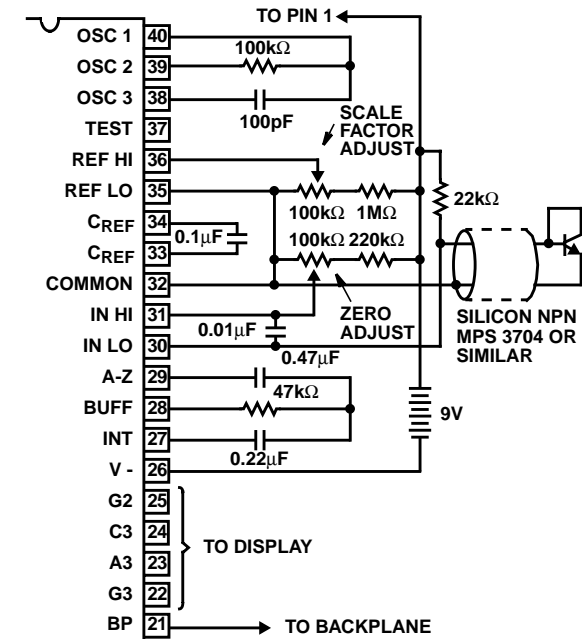
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Typical Applications (Continued)



The resistor values within the bridge are determined by the desired sensitivity.

FIGURE 17. ICL7107 MEASURING RATIOMETRIC VALUES OF QUAD LOAD CELL



A silicon diode-connected transistor has a temperature coefficient of about $-2\text{mV}/^\circ\text{C}$. Calibration is achieved by placing the sensing transistor in ice water and adjusting the zeroing potentiometer for a 000.0 reading. The sensor should then be placed in boiling water and the scale-factor potentiometer adjusted for a 100.0 reading.

FIGURE 18. ICL7106 USED AS A DIGITAL CENTIGRADE THERMOMETER

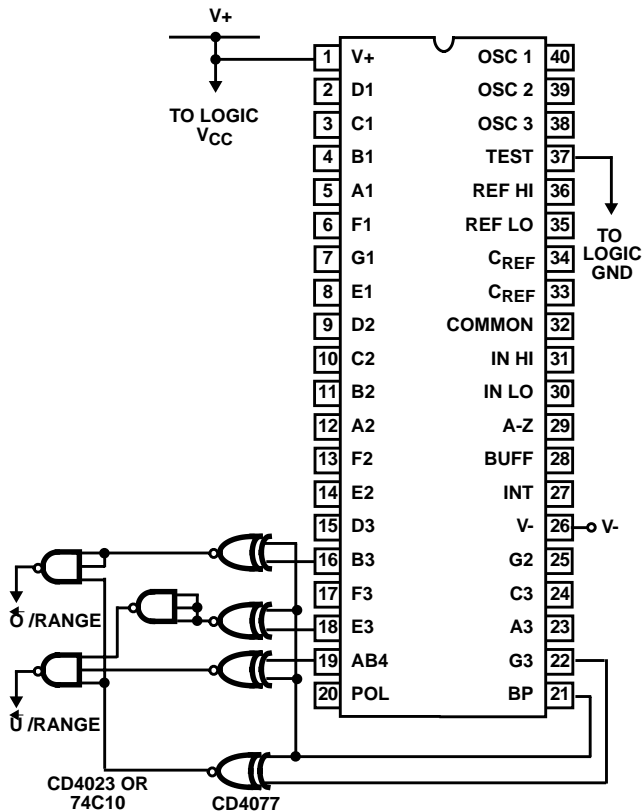


FIGURE 19. CIRCUIT FOR DEVELOPING UNDERRANGE AND OVERRANGE SIGNAL FROM ICL7106 OUTPUTS

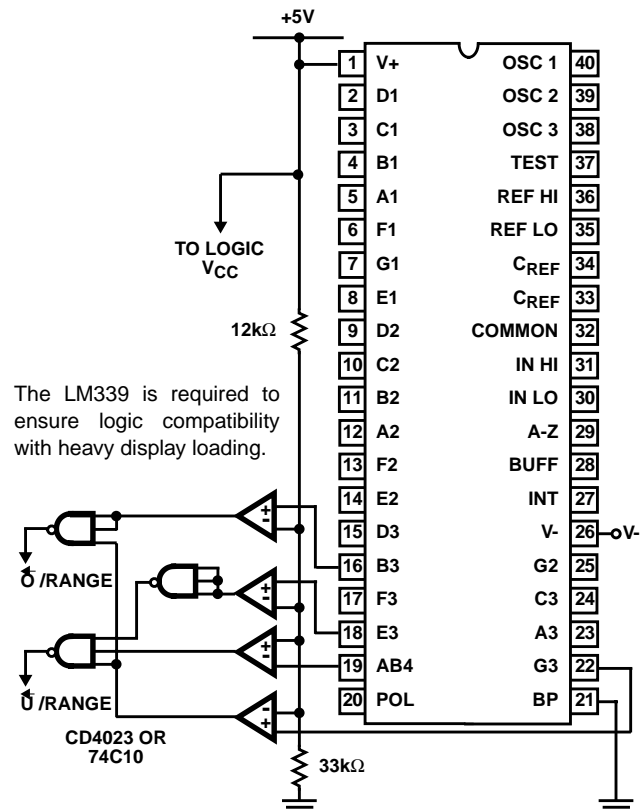
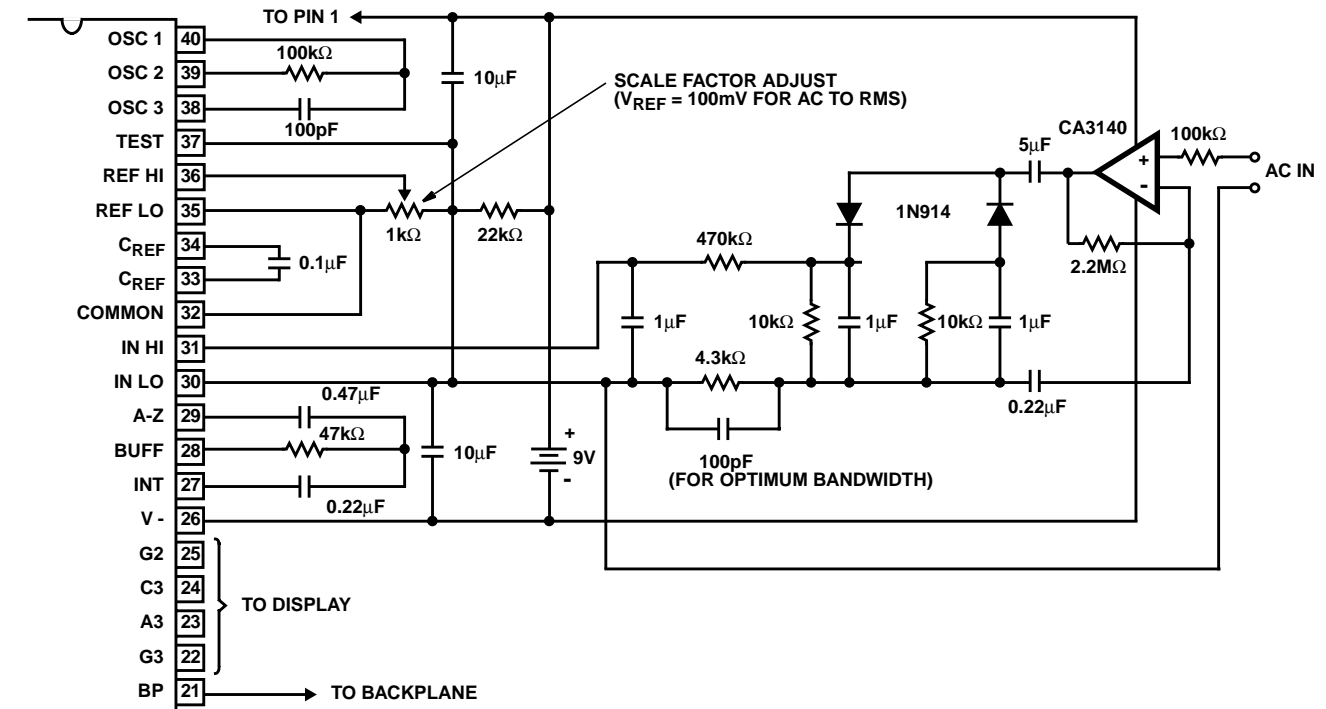


FIGURE 20. CIRCUIT FOR DEVELOPING UNDERRANGE AND OVERRANGE SIGNALS FROM ICL7107 OUTPUT

ICL7106, ICL7107, ICL7106S, ICL7107S

Typical Applications (Continued)



Test is used as a common-mode reference level to ensure compatibility with most op amps.

FIGURE 21. AC TO DC CONVERTER WITH ICL7106

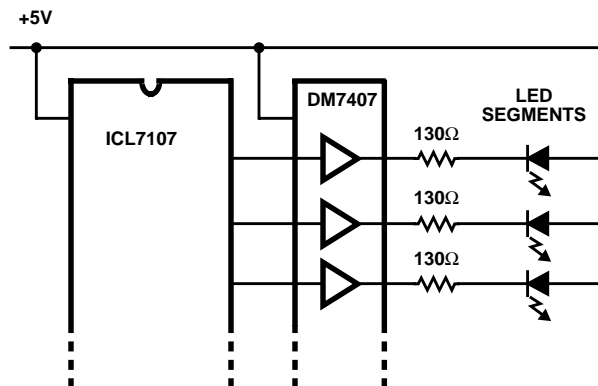
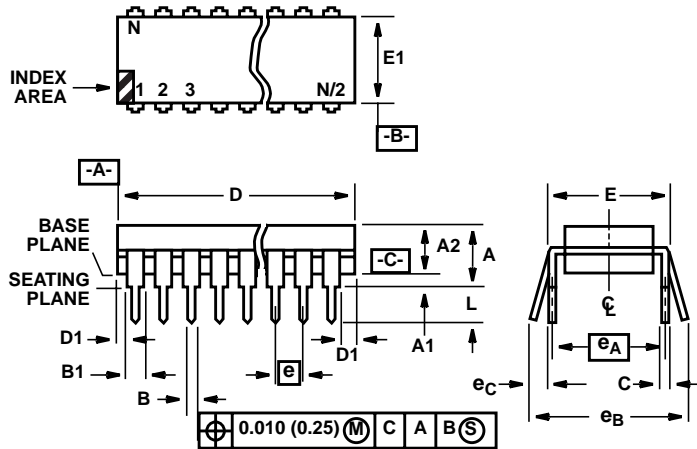


FIGURE 22. DISPLAY BUFFERING FOR INCREASED DRIVE CURRENT

ICL7106, ICL7107, ICL7106S, ICL7107S

Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E40.6 (JEDEC MS-011-AC ISSUE B)

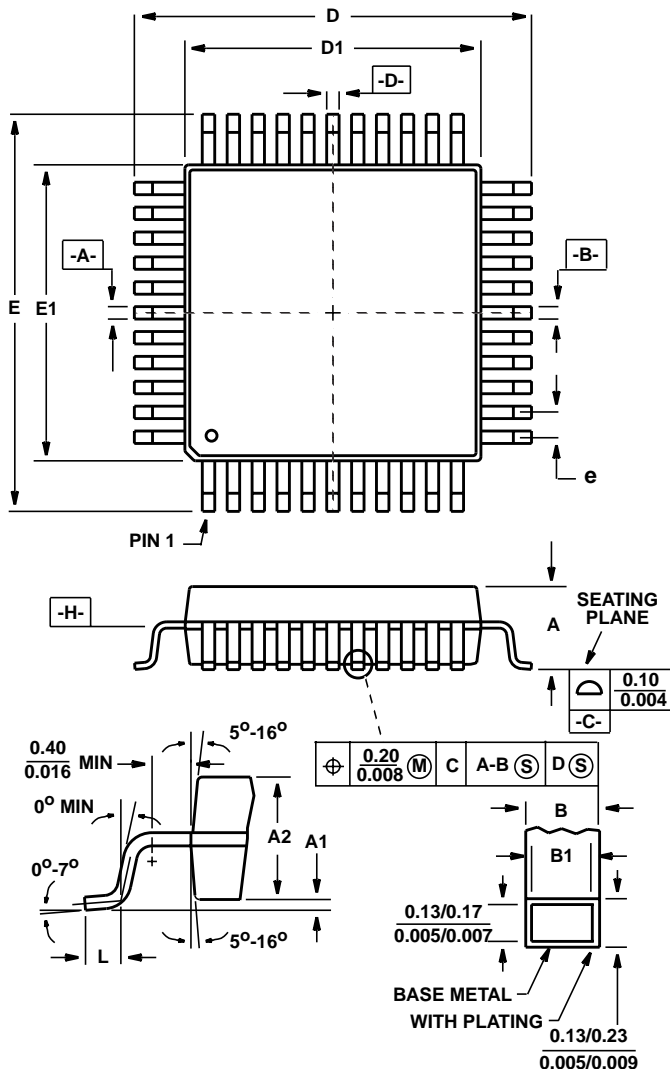
40 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.250	-	6.35	4
A1	0.015	-	0.39	-	4
A2	0.125	0.195	3.18	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.030	0.070	0.77	1.77	8
C	0.008	0.015	0.204	0.381	-
D	1.980	2.095	50.3	53.2	5
D1	0.005	-	0.13	-	5
E	0.600	0.625	15.24	15.87	6
E1	0.485	0.580	12.32	14.73	5
e	0.100 BSC		2.54 BSC		-
e_A	0.600 BSC		15.24 BSC		6
e_B	-	0.700	-	17.78	7
L	0.115	0.200	2.93	5.08	4
N	40		40		9

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ICL7106, ICL7107, ICL7106S, ICL7107S

Metric Plastic Quad Flatpack Packages (MQFP/PQFP)



Q44.10x10 (JEDEC MO-108AA-2 ISSUE A) 44 LEAD METRIC PLASTIC QUAD FLATPACK PACKAGE

SYM-BOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.093	-	2.35	-
A1	0.004	0.010	0.10	0.25	-
A2	0.077	0.083	1.95	2.10	-
B	0.012	0.018	0.30	0.45	6
B1	0.012	0.016	0.30	0.40	-
D	0.510	0.530	12.95	13.45	3
D1	0.390	0.398	9.90	10.10	4, 5
E	0.510	0.530	12.95	13.45	3
E1	0.390	0.398	9.90	10.10	4, 5
L	0.026	0.037	0.65	0.95	-
N	44		44		7
e	0.032 BSC		0.80 BSC		-

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NOTES:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. All dimensions and tolerances per ANSI Y14.5M-1982.
3. Dimensions D and E to be determined at seating plane **-C-**.
4. Dimensions D1 and E1 to be determined at datum plane **-H-**.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm (0.010 inch) per side.
6. Dimension B does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total.
7. "N" is the number of terminal positions.

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