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SEMICONDUCTOR TECHNICAL DATA

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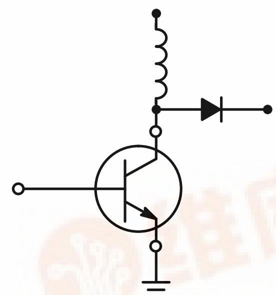
2N6836

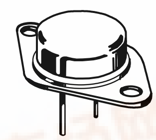
15 AMPERE
NPN SILICON
POWER TRANSISTOR
450 VOLTS
175 WATTS

Designer's™ Data Sheet
Switchmode Series Ultra-Fast NPN Silicon Power Transistors

These transistors are designed for high–voltage, high–speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line–operated switchmode applications.

- Switching Regulators
- Inverters
- Motor Controls
- Deflection Circuits
- Fast Turn–Off Times
  - 30 ns Inductive Fall Time — 75°C (Typ)
  - 50 ns Inductive Crossover Time — 75°C (Typ)
  - 600 ns Inductive Storage Time — 75°C (Typ)
- Operating Temperature Range –65 to +200°C
- 100°C Performance Specified for:
  - Reverse–Biased SOA with Inductive Loads
  - Switching Times with Inductive Loads
  - Saturation Voltages
  - Leakage Currents





CASE 1–07
TO–204AA
(TO–3)

MAXIMUM RATINGS (2)

Rating	Symbol	Max	Unit
Collector–Emitter Voltage	$V_{CEO(sus)}$	450	Vdc
Collector–Emitter Voltage	V_{CEV}	850	Vdc
Emitter Base Voltage	V_{EB}	6.0	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	15 20	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	10 15	Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	175 100 1.0	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200	°C

THERMAL CHARACTERISTICS (2)

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5.0 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.
(2) Indicate JEDEC Registered Data.

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Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector–Emitter Sustaining Voltage (Table 2) (I_C = 100 mA, I_B = 0)	$V_{CEO(sus)}$	450*	—	—	Vdc
Collector Cutoff Current (V_{CEV} = 850 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = 850 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)	I_{CEV}	 — —	 — —	 0.25* 1.5*	mAdc
Collector Cutoff Current (V_{CE} = 850 Vdc, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	—	—	2.5	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)	I_{EBO}	—	—	1.0*	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 15*			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 16			
ON CHARACTERISTICS (1)					
Collector–Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 0.7 Adc) (I_C = 10 Adc, I_B = 1.0 Adc) (I_C = 10 Adc, I_B = 1.0 Adc, T_C = 100°C)	$V_{CE(sat)}$	 — — —	 — — —	 1.2 2.5* 3.0*	Vdc
Base–Emitter Saturation Voltage (I_C = 10 Adc, I_B = 1.0 Adc) (I_C = 10 Adc, I_B = 1.0 Adc, T_C = 100°C)	$V_{BE(sat)}$	 — —	 — —	 1.5* 1.5	Vdc
DC Current Gain (I_C = 10 Adc, V_{CE} = 5.0 Vdc) (I_C = 15 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	 8.0* 5.0	 — —	 30* —	—
DYNAMIC CHARACTERISTICS (2)					
Current Gain — Bandwidth Product (V_{CE} = 10 Vdc, I_C = 0.25 Adc, f_{test} = 10 MHz)	f_T	10*	—	75*	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)	C_{ob}	50*	—	400*	pF

SWITCHING CHARACTERISTICS

Characteristic	Conditions		Symbol	Min	Typ	Max	Unit
Resistive Load (Table 1)							
Delay Time	(I_C = 10 Adc, V_{CC} = 250 Vdc, I_{B1} = 1.0 Adc, PW = 30 µs, Duty Cycle ≤ 2.0%)	(I_{B2} = 2.6 Adc, R_{B2} = 1.6 Ω)	t_d	—	20	100*	ns
Rise Time			t_r	—	200	500*	
Storage Time			t_s	—	1200	3000*	
Fall Time			t_f	—	200	250*	
Storage Time		($V_{BE(off)}$ = 5.0 Vdc)	t_s	—	650	—	
Fall Time			t_f	—	80	—	
Inductive Load (Table 2)							
Storage Time	(I_C = 10 Adc, I_{B1} = 1.0 Adc, $V_{BE(off)}$ = 5.0 Vdc, $V_{CE(pk)}$ = 400 Vdc)	(T_C = 100°C)	t_{sv}	—	800	1500*	ns
Fall Time			t_{fi}	—	50	150*	
Crossover Time			t_c	—	90	200*	
Storage Time		(T_C = 150°C)	t_{sv}	—	1050	—	
Fall Time			t_{fi}	—	70	—	
Crossover Time			t_c	—	120	—	

(1) Pulse Test: PW ± 300 µs, Duty Cycle ≤ 2%.
(2) f_T = |she| f_{test}.
* Indicates JEDEC Registered Limit.

TYPICAL STATIC CHARACTERISTICS

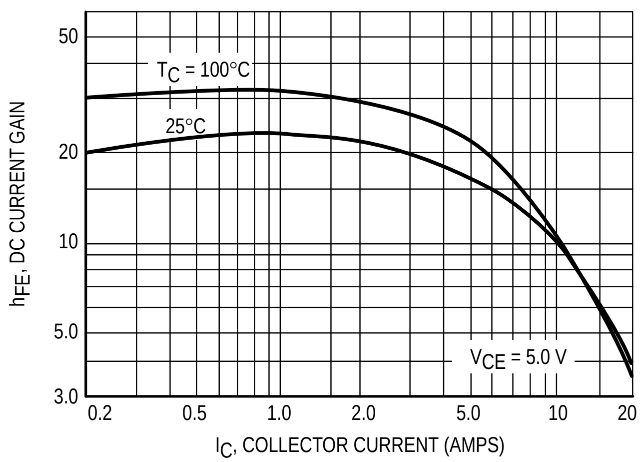


Figure 1. DC Current Gain

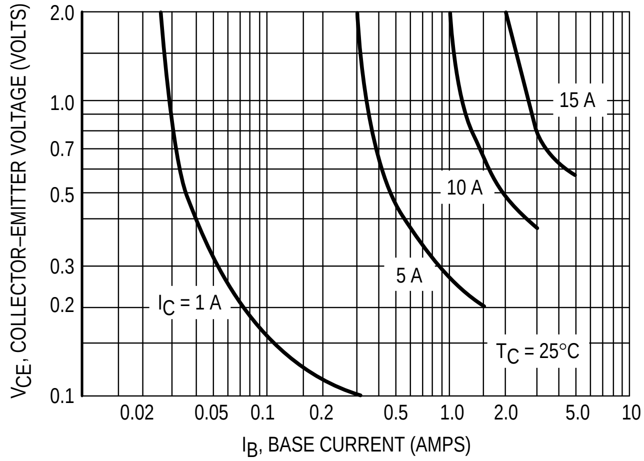


Figure 2. Collector Saturation Region

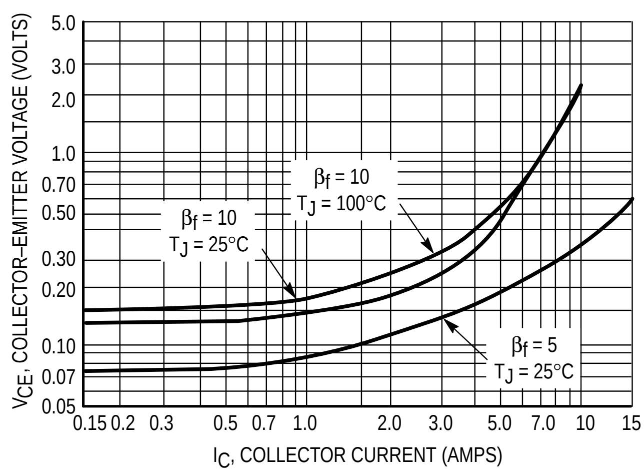


Figure 3. Collector–Emitter Saturation Voltage

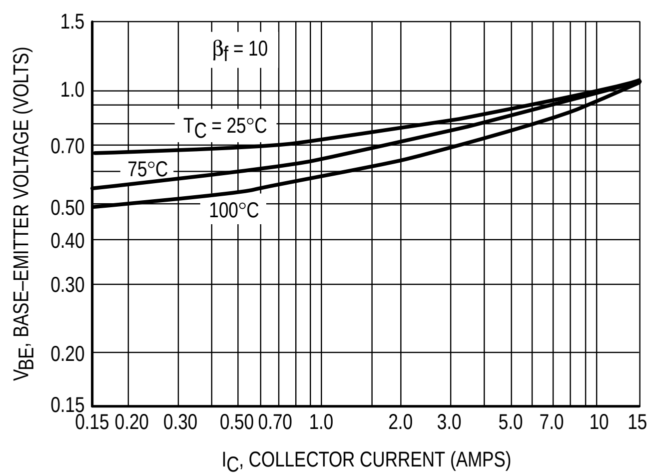


Figure 4. Base–Emitter Voltage

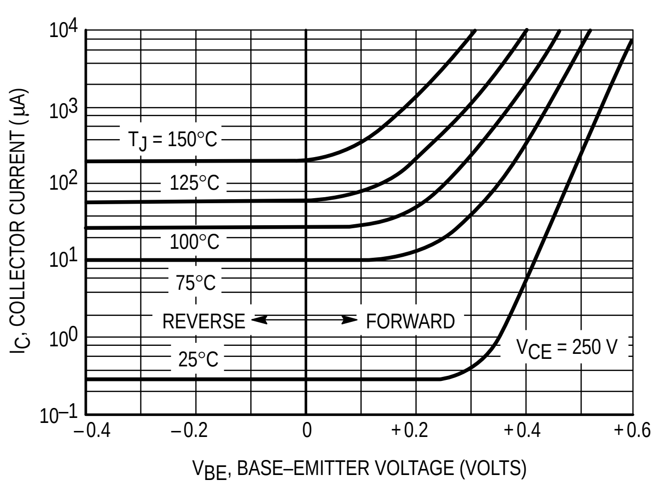


Figure 5. Collector Cutoff Region

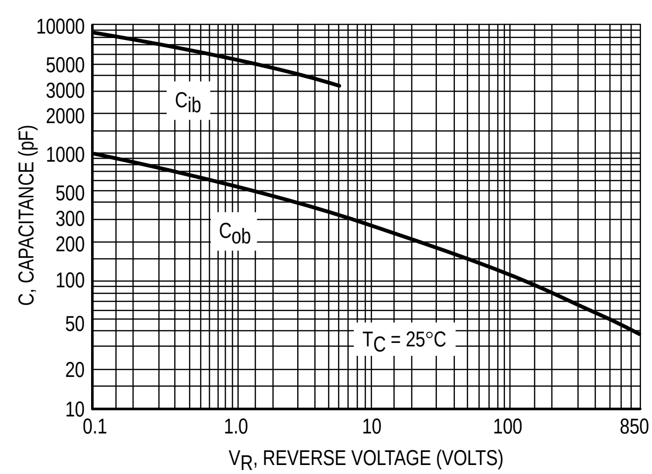


Figure 6. Capacitance

TYPICAL DYNAMIC CHARACTERISTICS

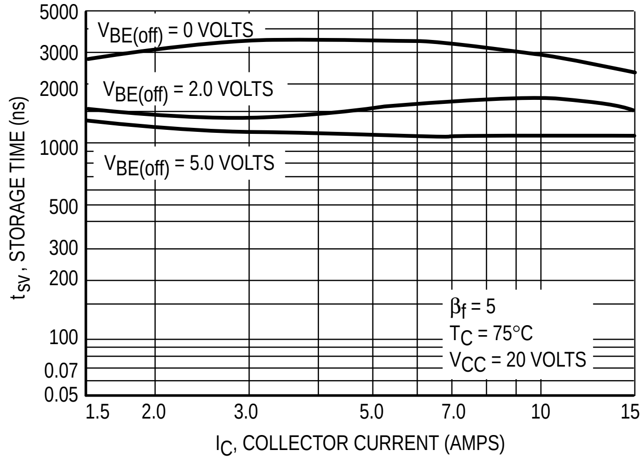


Figure 7. Storage Time

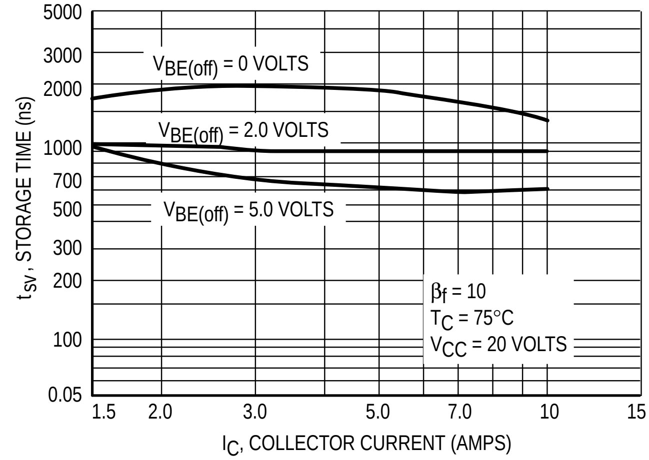


Figure 8. Storage Time

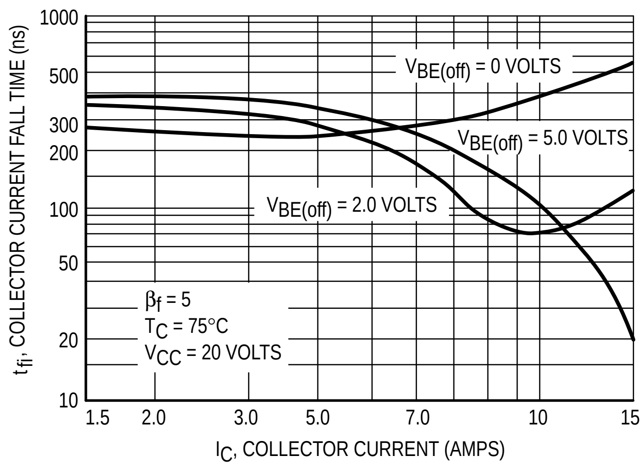


Figure 9. Collector Current Fall Time

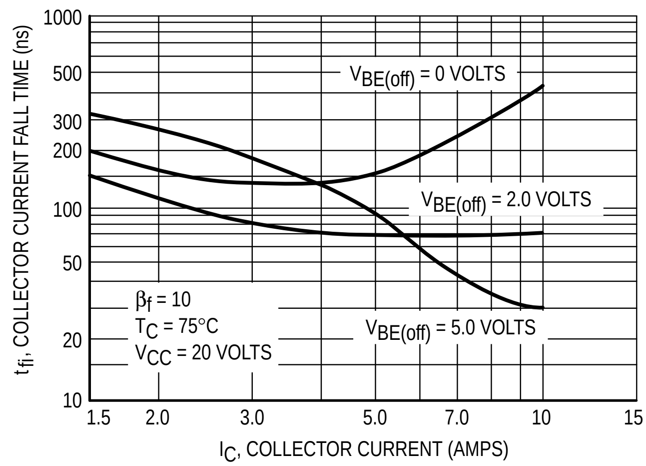


Figure 10. Collector Current Fall Time

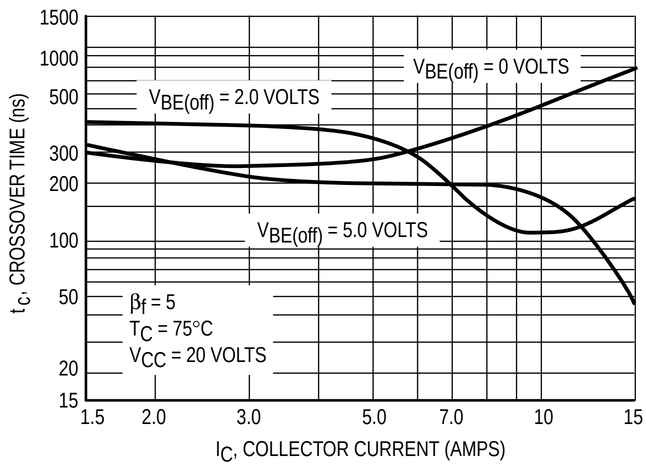


Figure 11. Crossover Time

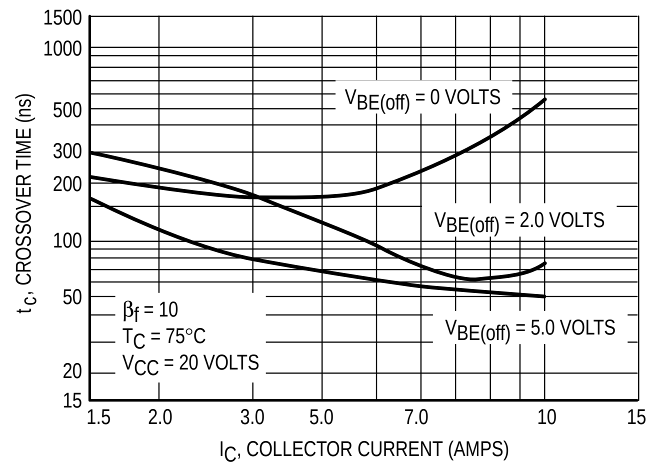


Figure 12. Crossover Time

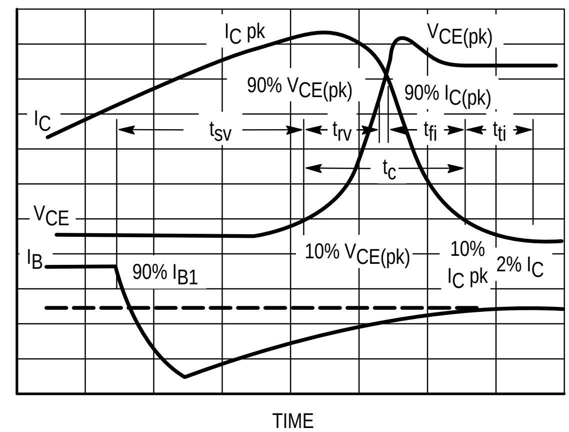


Figure 13. Inductive Switching Measurements

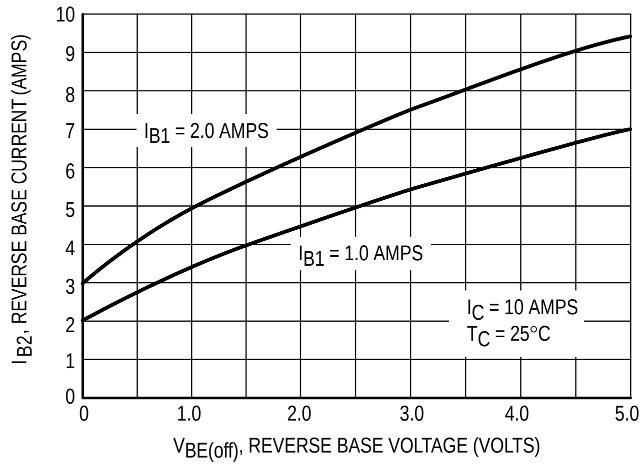


Figure 14. Peak Reverse Base Current

GUARANTEED SAFE OPERATING AREA LIMITS

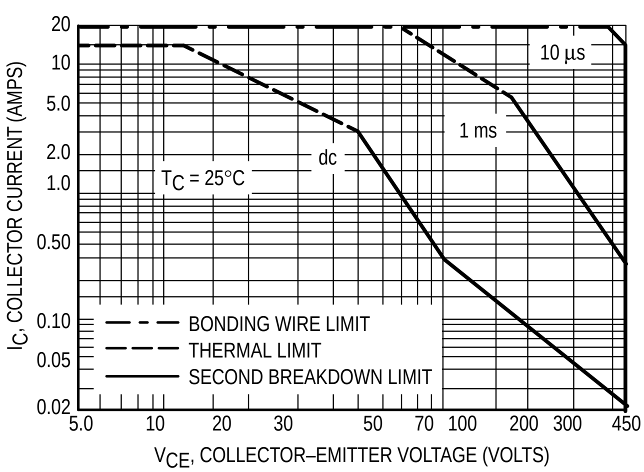


Figure 15. Maximum Forward Bias Safe Operating Area

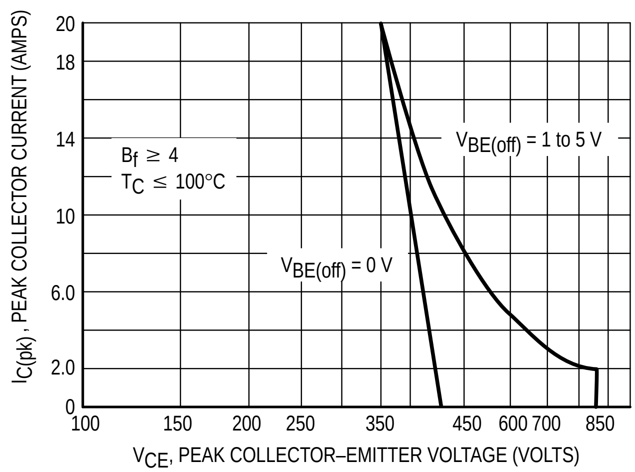


Figure 16. Maximum Reverse Bias Safe Operating Area

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C – V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 15 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 15 may be found at any case temperature by using the appropriate curve on Figure 18.

$T_{J(pk)}$ may be calculated from the data in Figure 17. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn–off, in most cases, with the base–to–emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, R_C snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage–current condition allowable during reverse biased turn–off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 16 gives the RBSOA characteristics.

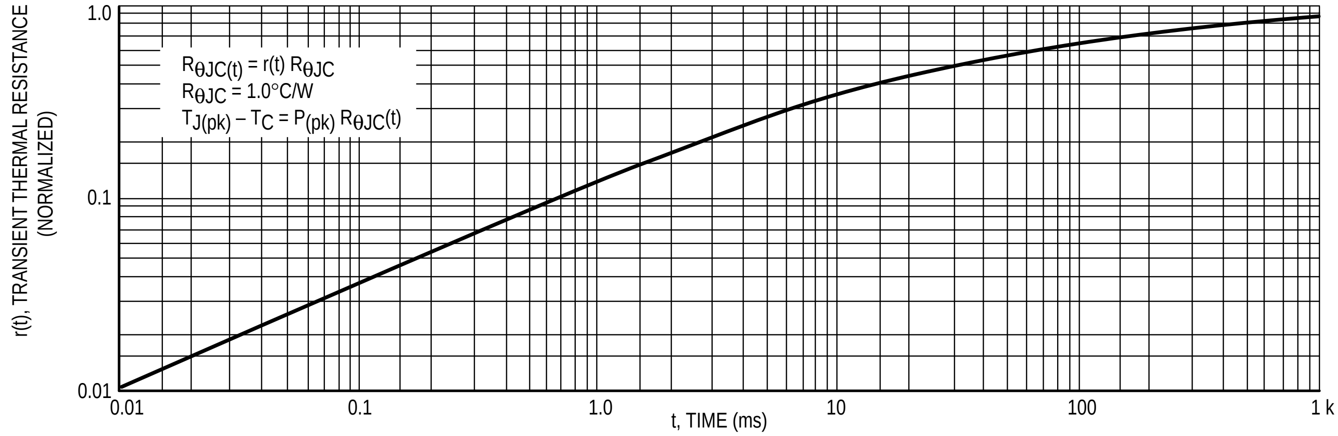


Figure 17. Thermal Response

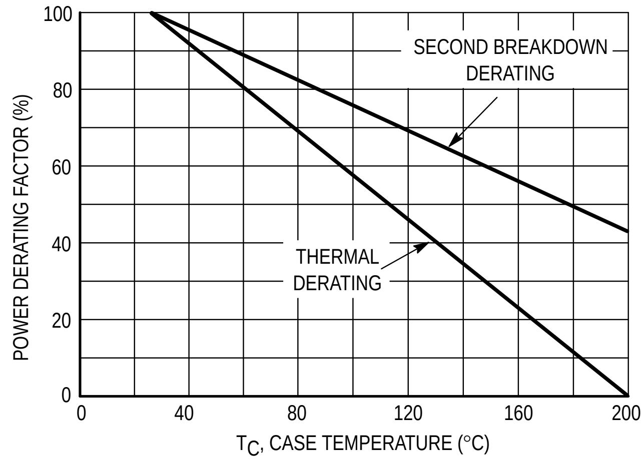
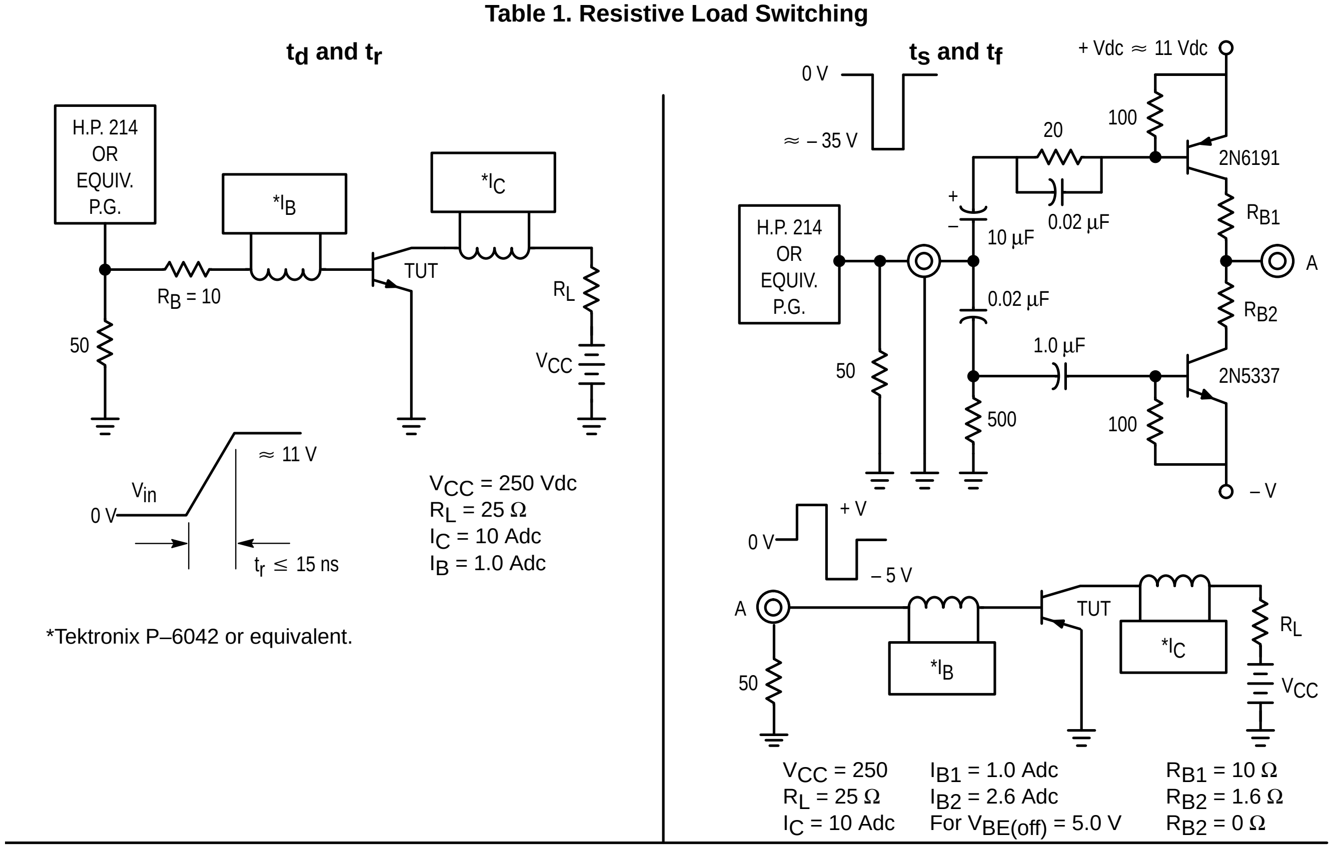


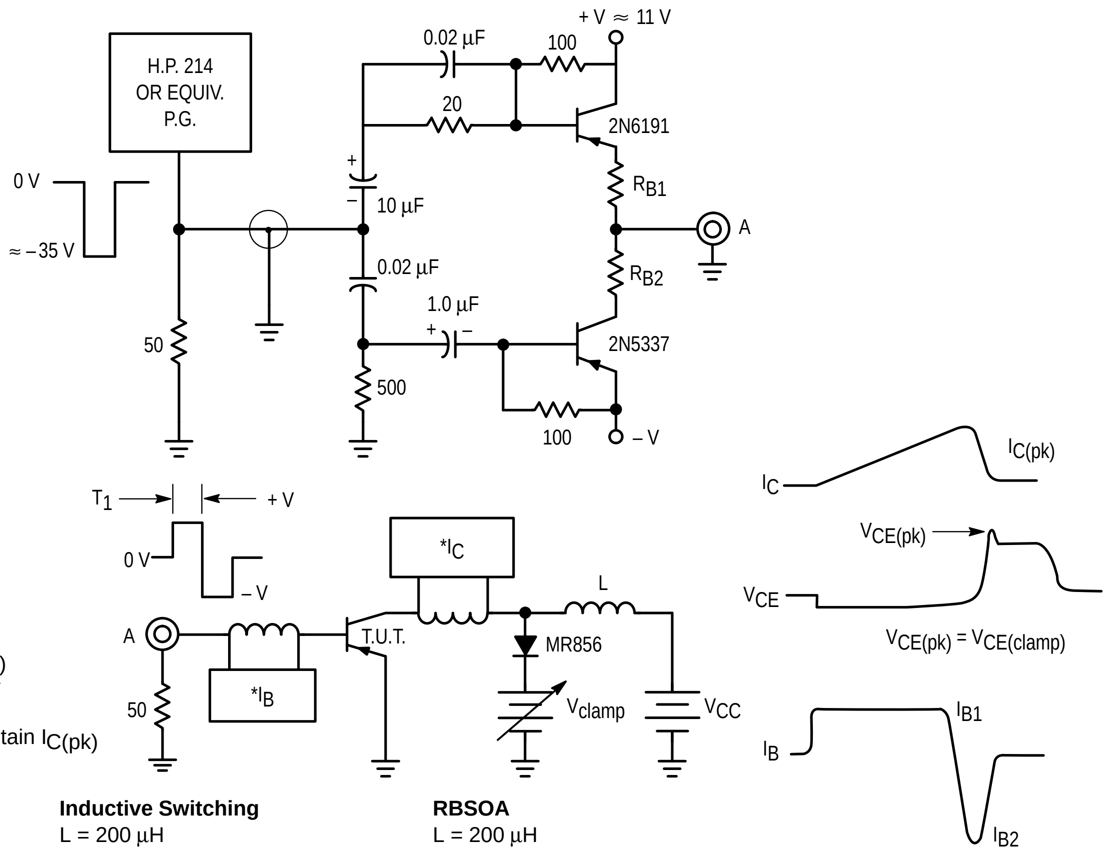
Figure 18. Power Derating

Table 1. Resistive Load Switching



*NOTE: Adjust – V to obtain desired $V_{BE(off)}$ at Point A.

Table 2. Inductive Load Switching



$T_1 \approx \frac{L_{coil}\,(I_{Cpk})}{V_{CC}}$

T_1 adjusted to obtain $I_{C(pk)}$

$V_{(BR)CEO}$	Inductive Switching	RBSOA
L = 10 mH	L = 200 µH	L = 200 µH
$R_{B2} = \infty$	$R_{B2} = 0$	$R_{B2} = 0$
V_{CC} = 20 Volts	V_{CC} = 20 Volts	V_{CC} = 20 Volts
	R_{B1} selected for desired I_{B1}	R_{B1} selected for desired I_{B1}

*Tektronix P–6042 or Equivalent

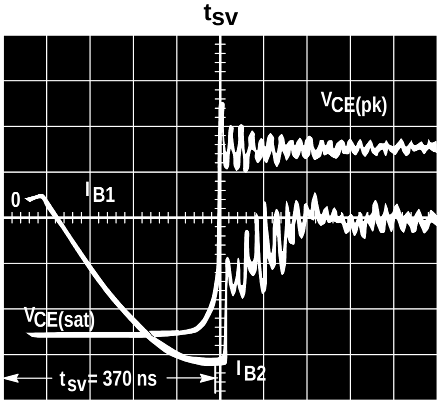
Scope — Tektronix 7403 or Equivalent

Note: Adjust –V to obtain desired $V_{BE(off)}$ at Point A.

TYPICAL INDUCTIVE SWITCHING WAVEFORMS

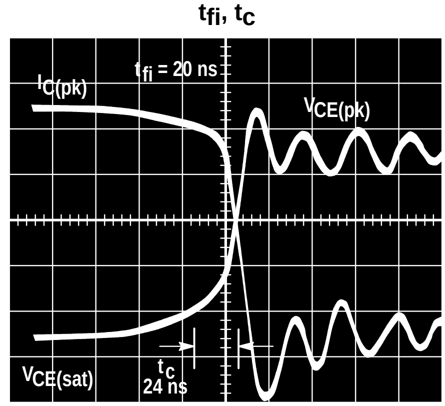
$I_{C(pk)}$ = 10 Amps
I_{B1} = 1.0 Amp
$V_{BE(off)}$ = 5.0 Volts
$V_{CE(pk)}$ = 400 Volts
T_C = 25°C
Time Base = 100 ns/cm

t_{sv}

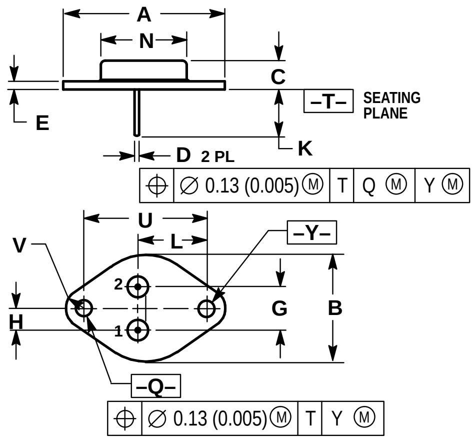


$I_{C(pk)}$ = 10 Amps
I_{B1} = 1.0 Amp
$V_{BE(off)}$ = 5.0 Volts
$V_{CE(pk)}$ = 400 Volts
T_C = 25°C
Time Base = 20 ns/cm

t_{fi}, t_c



PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO–204AA OUTLINE SHALL APPLY.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.550 REF		39.37 REF	
B	—	1.050	—	26.67
C	0.250	0.335	6.35	8.51
D	0.038	0.043	0.97	1.09
E	0.055	0.070	1.40	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N	—	0.830	—	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

CASE 1–07
TO–204AA (TO–3)
ISSUE Z

How to reach us:
USA / EUROPE: Motorola Literature Distribution;
P.O. Box 20912; Phoenix, Arizona 85036. 1–800–441–2447

MFAX: RMFAX0@email.sps.mot.com – TOUCHTONE (602) 244–6609
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JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, Toshikatsu Otsuki,
6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 03–3521–8315

HONG KONG: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298