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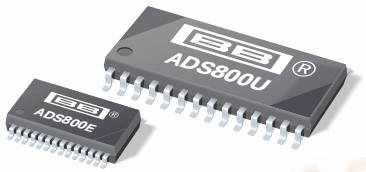



# ADS800

## SpeedPLUS™ 12-Bit, 40MHz Sampling ANALOG-TO-DIGITAL CONVERTER

## FEATURES

- LOW POWER: 390mW
- INTERNAL REFERENCE
- WIDEBAND TRACK/HOLD: 65MHz
- SINGLE +5V SUPPLY
- PACKAGE: 28-Lead SOIC and 28-Lead SSOP

## APPLICATIONS

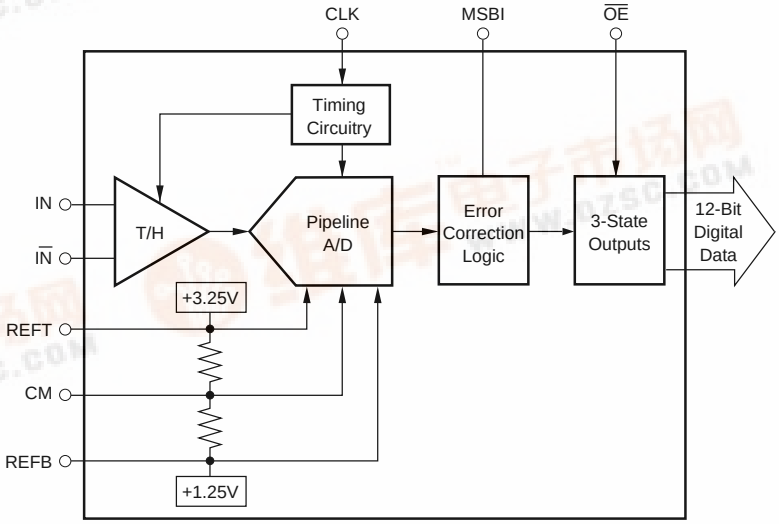
- IF AND BASEBAND DIGITIZATION
- DIGITAL COMMUNICATIONS
- ULTRASOUND IMAGING
- GAMMA CAMERAS
- TEST INSTRUMENTATION
- CCD IMAGING
  - Copiers
  - Scanners
  - Cameras
- VIDEO DIGITIZING

## DESCRIPTION

The ADS800 is a low power, monolithic 12-bit, 40MHz analog-to-digital converter utilizing a small geometry CMOS process. This COMPLETE converter includes a 12-bit quantizer, wideband track/hold, reference and three-state outputs. It operates from a single +5V power supply and can be configured to accept either differential or single-ended input signals.

The ADS800 employs digital error correction to provide excellent Nyquist differential linearity performance for demanding imaging applications. Its low distortion, high SNR and high oversampling capability give it the extra margin needed for telecommunications, test instrumentation and video applications.

This high performance A/D converter is specified over temperature for AC and DC performance at a 40MHz sampling rate. The ADS800 is available in 28-lead SOIC and SSOP packages.

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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

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# SPECIFICATIONS

At $T_A$ = +25°C, $V_S$ = +5V, Sampling Rate = 40MHz, with a 50% duty cycle clock having a 2ns rise/fall time, unless otherwise noted.

| PARAMETER | CONDITIONS | TEMP | ADS800U (SOIC) MIN | ADS800U (SOIC) TYP | ADS800U (SOIC) MAX | ADS800E (SSOP) MIN | ADS800E (SSOP) TYP | ADS800E (SSOP) MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| Resolution | | | | 12 | | | * | | Bits |
| Specified Temperature Range | $T_{AMBIENT}$ | | 0 | | +70 | *(1) | | * | °C |
| Operating Temperature Range | $T_{AMBIENT}$ | | –40 | | +85 | * | | * | °C |
| **ANALOG INPUT** | | | | | | | | | |
| Differential Full Scale Input Range | Both Inputs, 180° Out of Phase | | +1.25 | | +3.25 | * | | * | V |
| Common-Mode Voltage | | | | +2.25 | | | * | | V |
| Analog Input Bandwidth (–3dB) | | | | | | | | | |
| Small Signal | –20dBFS(2) Input | +25°C | | 400 | | | * | | MHz |
| Full Power | 0dBFS Input | +25°C | | 65 | | | * | | MHz |
| Input Impedance | | | | 1.25 \|\| 4 | | | * | | MΩ \|\| pF |
| **DIGITAL INPUT** | | | | | | | | | |
| Logic Family | | | TTL/HCT Compatible CMOS | | | TTL/HCT Compatible CMOS | | | |
| Convert Command | Start Conversion | | Falling Edge | | | Falling Edge | | | |
| **ACCURACY(3)** | | | | | | | | | |
| Gain Error | | +25°C | | ±0.4 | ±1.5 | | * | * | % |
| | | Full | | ±0.6 | ±2.5 | | * | * | % |
| Gain Drift | | | | ±95 | | | * | | ppm/°C |
| Power Supply Rejection of Gain | Delta +$V_S$ = ±5% | +25°C | | 0.01 | 0.15 | | * | * | %FSR/% |
| Input Offset Error | | Full | | ±2.6 | ±3.5 | | * | * | % |
| Power Supply Rejection of Offset | Delta +$V_S$ = ±5% | +25°C | | 0.02 | 0.15 | | * | * | %FSR/% |
| **CONVERSION CHARACTERISTICS** | | | | | | | | | |
| Sample Rate | | | 10k | | 40M | * | | * | Sample/s |
| Data Latency | | | | 6.5 | | | * | | Convert Cycle |
| **DYNAMIC CHARACTERISTICS** | | | | | | | | | |
| Differential Linearity Error | | | | | | | | | |
| f = 500kHz | $t_H$ = 13ns(4) | +25°C | | ±0.6 | ±1.0 | | * | | LSB |
| | | Full | | ±0.8 | | | * | | LSB |
| f = 12MHz | | +25°C | | ±0.4 | ±1.0 | | ±0.7 | | LSB |
| | | Full | | ±0.5 | | | ±0.8 | | LSB |
| No Missing Codes | $t_H$ = 13ns(4) | +25°C | | Guaranteed | | | Guaranteed | | LSB |
| Integral Linearity Error at f = 500kHz | | Full | | ±1.9 | | | * | | LSB |
| Spurious-Free Dynamic Range (SFDR) | | | | | | | | | |
| f = 500kHz (–1dBFS input) | | +25°C | 65 | 72 | | * | * | | dBFS |
| | | Full | 60 | 66 | | * | * | | dBFS |
| f = 12MHz (–1dBFS input) | | +25°C | 58 | 61 | | * | * | | dBFS |
| | | Full | 55 | 61 | | * | * | | dBFS |
| Two-Tone Intermodulation Distortion (IMD)(5) | | | | | | | | | |
| f = 4.4MHz and 4.5MHz (–7dBFS each tone) | | +25°C | | –63 | | | * | | dBc |
| | | Full | | –62 | | | * | | dBc |
| Signal-to-Noise Ratio (SNR) | | | | | | | | | |
| f = 500kHz (–1dBFS input) | | +25°C | 61 | 64 | | 59 | * | | dB |
| | | Full | 57 | 63 | | * | * | | dB |
| f = 12MHz (–1dBFS input) | | +25°C | 61 | 62 | | 59 | * | | dB |
| | | Full | 56 | 62 | | * | * | | dB |
| Signal-to-(Noise + Distortion) (SINAD) | | | | | | | | | |
| f = 500kHz (–1dBFS input) | | +25°C | 59 | 63 | | 57 | * | | dB |
| | | Full | 54 | 64 | | * | * | | dB |
| f = 12MHz (–1dBFS input) | | +25°C | 56 | 58 | | 54 | * | | dB |
| | | Full | 51 | 57 | | * | * | | dB |
| Differential Gain Error | NTSC or PAL | +25°C | | 0.5 | | | * | | % |
| Differential Phase Error | NTSC or PAL | +25°C | | 0.1 | | | * | | degrees |
| Aperture Delay Time | | +25°C | | 2 | | | * | | ns |
| Aperture Jitter | | +25°C | | 7 | | | * | | ps rms |
| Overvoltage Recovery Time(6) | 1.5x Full Scale Input | +25°C | | 2 | | | * | | ns |

NOTE: (1) An asterisk (*) indicates same specifications as the ADS800U. (2) dBFS refers to dB below Full Scale. (3) Percentage accuracies are referred to the internal A/D Full Scale Range of 4Vp-p. (4) Refer to Timing Diagram footnotes for the guaranteed differential linearity performance and no missing codes condition for the SOIC and SSOP packages. (5) IMD is referred to the larger of the two input signals. If referred to the peak envelope signal (≈0dB), the intermodulation products will be 7dB lower. (6) No "rollover" of bits.

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# SPECIFICATIONS (CONT)

At $T_A$ = +25°C, $V_S$ = +5V, Sampling Rate = 40MHz, with a 50% duty cycle clock having a 2ns rise/fall time, unless otherwise noted.

| PARAMETER | CONDITIONS | TEMP | ADS800U (SOIC) MIN | ADS800U (SOIC) TYP | ADS800U (SOIC) MAX | ADS800E (SSOP) MIN | ADS800E (SSOP) TYP | ADS800E (SSOP) MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| **OUTPUTS** | | | | | | | | | |
| Logic Family | | | | TTL/HCT Compatible CMOS | | | TTL/HCT Compatible CMOS | | |
| Logic Coding | Logic Selectable | | | SOB or BTC | | | SOB or BTC | | |
| Logic Levels | Logic "LO", $C_L$ = 15pF max | Full | 0 | | 0.4 | * | | * | V |
| | Logic "HI", $C_L$ = 15pF max | Full | +2.5 | | $+V_S$ | * | | * | V |
| 3-State Enable Time | | | | 20 | 40 | | * | * | ns |
| 3-State Disable Time | | Full | | 2 | 10 | | * | * | ns |
| **POWER SUPPLY REQUIREMENTS** | | | | | | | | | |
| Supply Voltage: $+V_S$ | Operating | Full | +4.75 | +5.0 | +5.25 | * | * | * | V |
| Supply Current: $+I_S$ | Operating | +25°C | | 78 | 93 | | * | * | mA |
| | Operating | Full | | 78 | 97 | | * | * | mA |
| Power Consumption | Operating | +25°C | | 390 | 465 | | * | * | mW |
| | Operating | Full | | 390 | 485 | | * | * | mW |
| Thermal Resistance, $\theta_{JA}$ | | | | | | | | | |
| 28-Lead SOIC | | | | 75 | | | | | °C/W |
| 28-Lead SSOP | | | | | | | 50 | | °C/W |

* Specifications same as ADS800U.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| $+V_S$ | +6V |
| Analog Input | 0V to ($+V_S$ + 300mV) |
| Logic Input | 0V to ($+V_S$ + 300mV) |
| Case Temperature | +100°C |
| Junction Temperature | +150°C |
| Storage Temperature | +125°C |
| External Top Reference Voltage (REFT) | +3.4V Max |
| External Bottom Reference Voltage (REFB) | +1.1V Min |

NOTE: (1) Stresses above these ratings may permanently damage the device.

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|
| ADS800U | 28-Lead SOIC | 217 | –40°C to +85°C |
| ADS800E | 28-Lead SSOP | 324 | –40°C to +85°C |

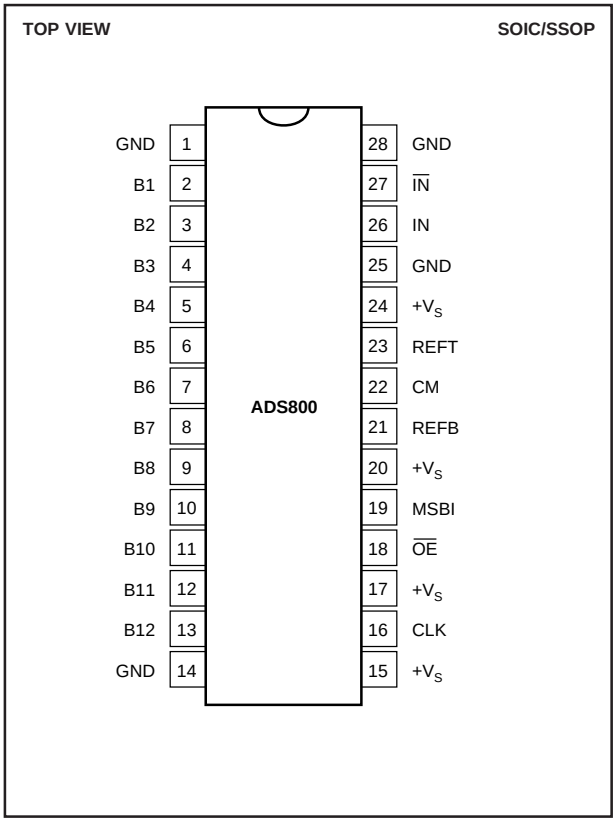
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

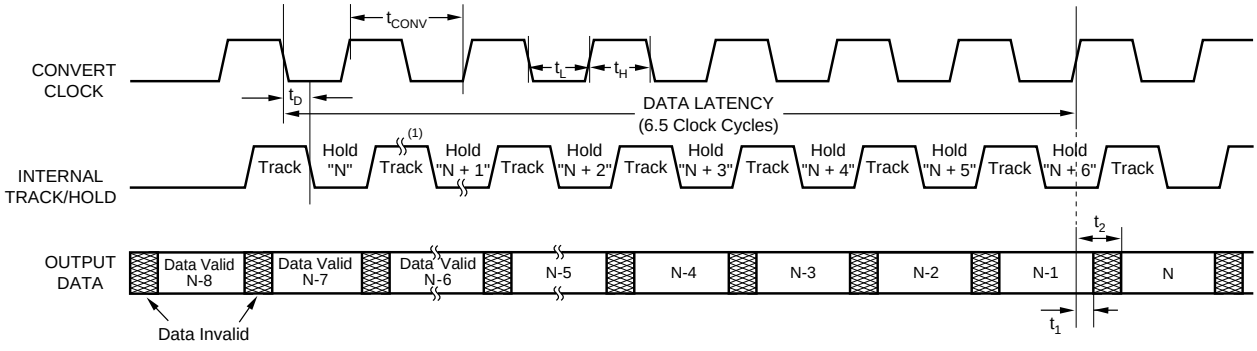
## PIN CONFIGURATION




## PIN DESCRIPTIONS

| PIN | DESIGNATOR | DESCRIPTION |
|---|---|---|
| 1 | GND | Ground |
| 2 | B1 | Bit 1, Most Significant Bit |
| 3 | B2 | Bit 2 |
| 4 | B3 | Bit 3 |
| 5 | B4 | Bit 4 |
| 6 | B5 | Bit 5 |
| 7 | B6 | Bit 6 |
| 8 | B7 | Bit 7 |
| 9 | B8 | Bit 8 |
| 10 | B9 | Bit 9 |
| 11 | B10 | Bit 10 |
| 12 | B11 | Bit 11 |
| 13 | B12 | Bit 12, Least Significant Bit |
| 14 | GND | Ground |
| 15 | $+V_S$ | +5V Power Supply |
| 16 | CLK | Convert Clock Input, 50% Duty Cycle |
| 17 | $+V_S$ | +5V Power Supply |
| 18 | $\overline{OE}$ | HI: High Impedance State. LO or Floating: Normal Operation. Internal pull-down resistors. |
| 19 | MSBI | Most Significant Bit Inversion, HI: MSB inverted for complementary output. LO or Floating: Straight output. Internal pull-down resistors. |
| 20 | $+V_S$ | +5V Power Supply |
| 21 | REFB | Bottom Reference Bypass. For external bypassing of internal +1.25V reference. |
| 22 | CM | Common-Mode Voltage. It is derived by (REFT + REFB)/2. |
| 23 | REFT | Top Reference Bypass. For external bypassing of internal +3.25V reference. |
| 24 | $+V_S$ | +5V Power Supply |
| 25 | GND | Ground |
| 26 | IN | Input |
| 27 | $\overline{IN}$ | Complementary Input |
| 28 | GND | Ground |

## TIMING DIAGRAM



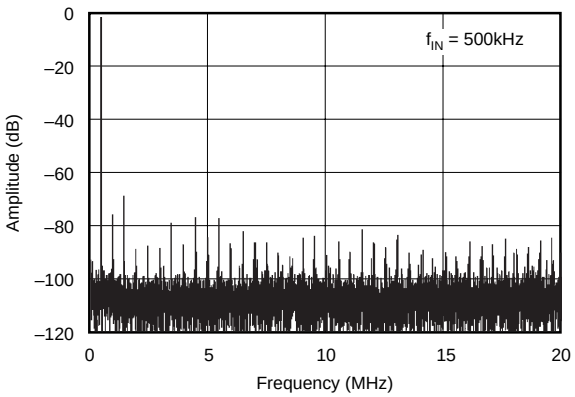

| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| $t_{CONV}$ | Convert Clock Period | 25 | | 100µs | ns |
| $t_L$ | Clock Pulse Low | 12 | 12.5 | | ns |
| $t_H$ | Clock Pulse High | 12(2) | 12.5 | | ns |
| $t_D$ | Aperture Delay | | 2 | | ns |
| $t_1$ | Data Hold Time, $C_L$ = 0pF | 3.9 | | | ns |
| $t_2$ | New Data Delay Time, $C_L$ = 15pF max | | | 12.5 | ns |

NOTE: (1) " ⟆ " indicates the portion of the waveform that will stretch out at slower sample rates. (2) $t_H$ must be 13ns minimum if no missing codes is desired only for the conditions of $t_{CONV}$ ≤28ns and $f_{IN}$ <2MHz for the SOIC package. For best performance in the SSOP package, $t_H$ must be 13ns minimum for all input frequencies and $t_{CONV}$ ≤28ns. Refer to the Clock Requirements for a possible clock skew circuit for this condition.

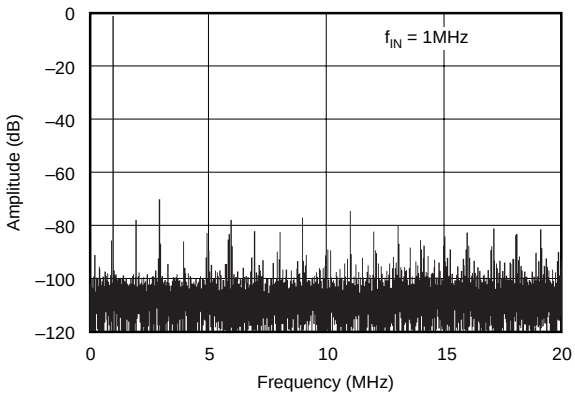
# TYPICAL PERFORMANCE CURVES

At $T_A$ = +25°C, $V_S$ = +5V, Sampling Rate = 40MHz, with a 50% duty cycle clock having a 2ns rise/fall time, unless otherwise noted.

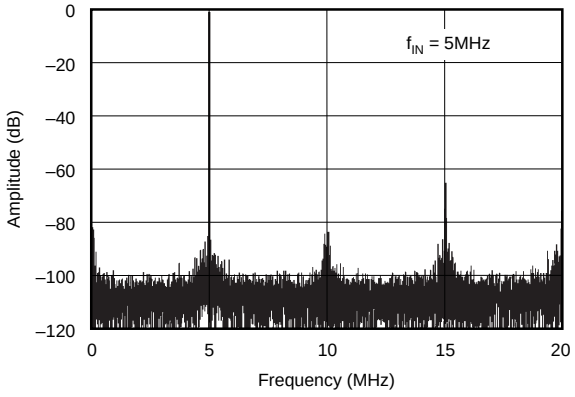
SPECTRAL PERFORMANCE



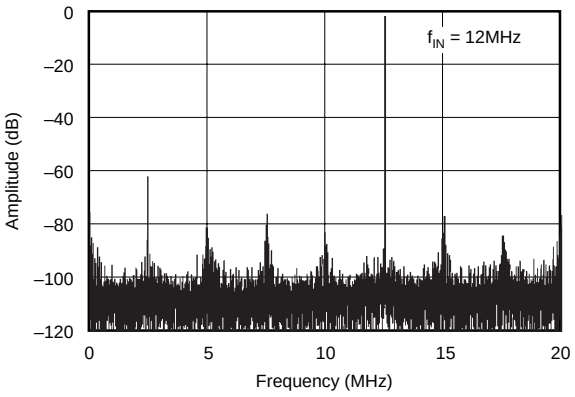

SPECTRAL PERFORMANCE



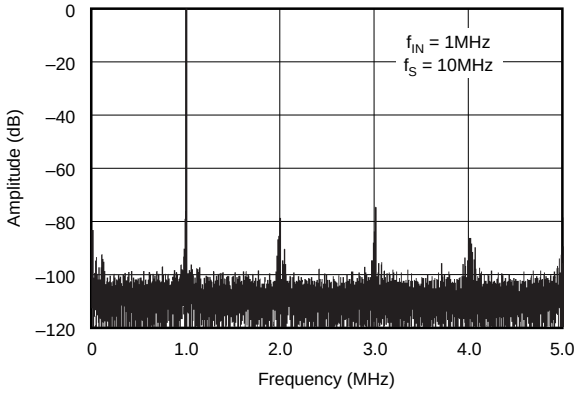

SPECTRAL PERFORMANCE



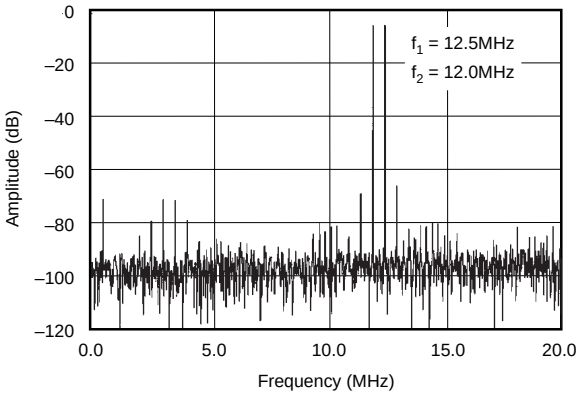

SPECTRAL PERFORMANCE




SPECTRAL PERFORMANCE



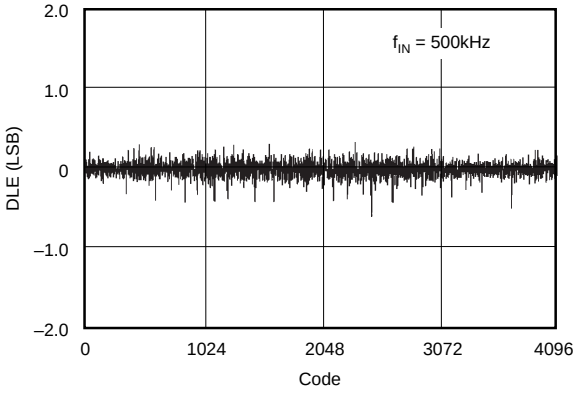

TWO-TONE INTERMODULATION



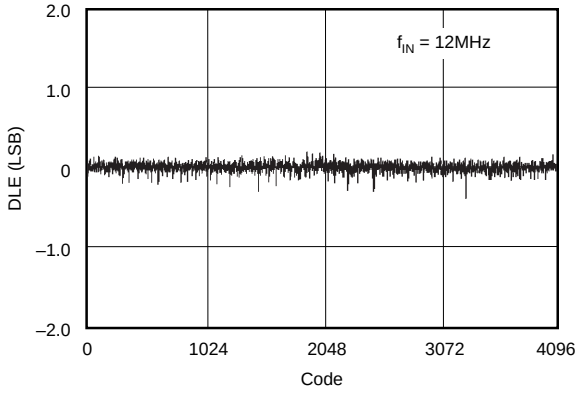
# TYPICAL PERFORMANCE CURVES (CONT)

At $T_A$ = +25°C, $V_S$ = +5V, Sampling Rate = 40MHz, with a 50% duty cycle clock having a 2ns rise/fall time, unless otherwise noted.

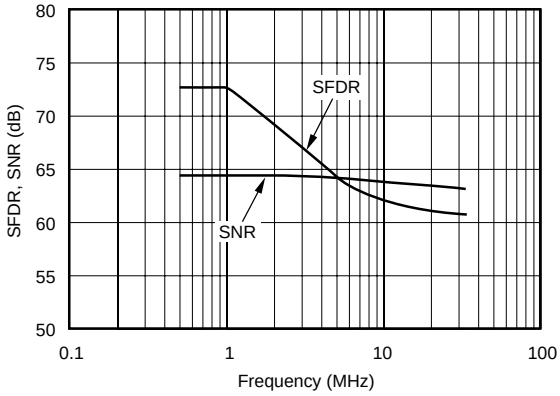
DIFFERENTIAL LINEARITY ERROR



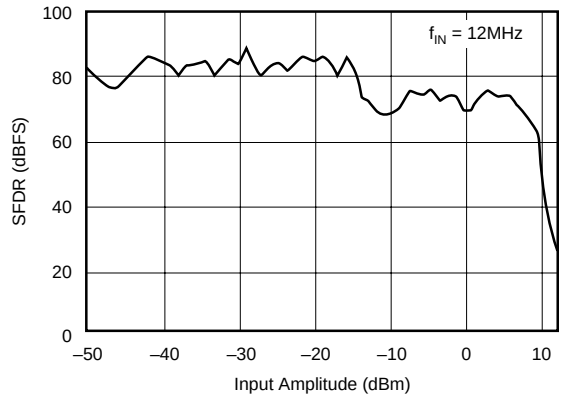

DIFFERENTIAL LINEARITY ERROR



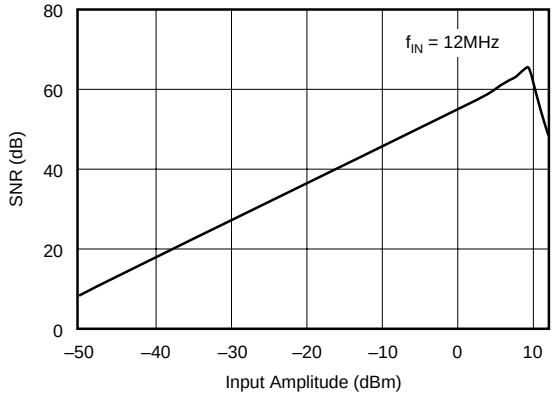

DYNAMIC PERFORMANCE vs INPUT FREQUENCY



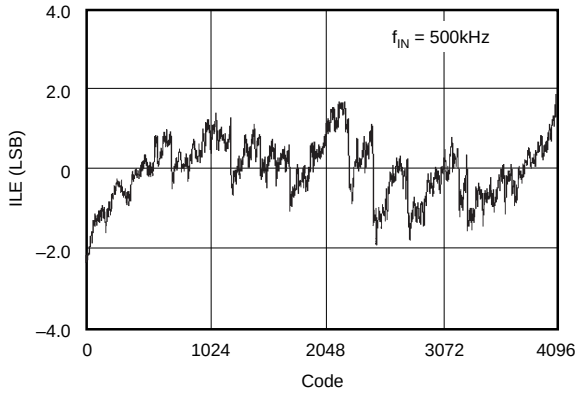

SWEPT POWER SFDR




SWEPT POWER SNR



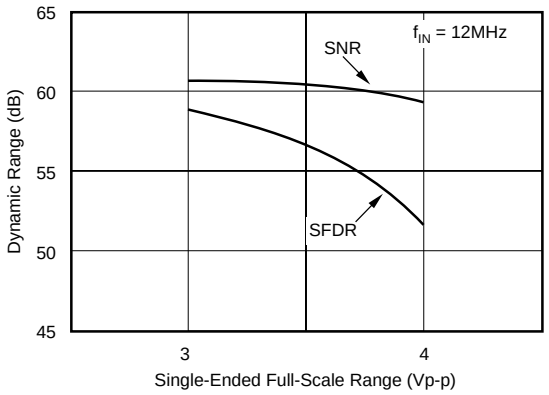

INTEGRAL LINEARITY ERROR



# TYPICAL PERFORMANCE CURVES (CONT)

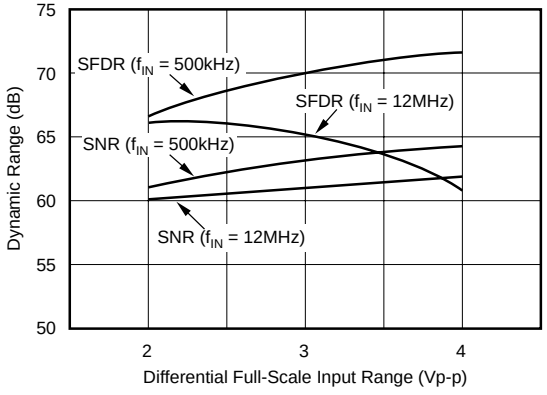
At $T_A$ = +25°C, $V_S$ = +5V, Sampling Rate = 40MHz, with a 50% duty cycle clock having a 2ns rise/fall time, unless otherwise noted.

DYNAMIC PERFORMANCE
vs SINGLE-ENDED FULL-SCALE INPUT RANGE



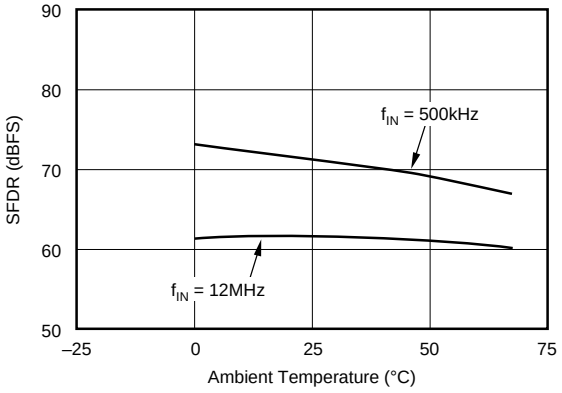

NOTE: $REFT_{EXT}$ varied, REFB is fixed at the internal value of +1.25V.

DYNAMIC PERFORMANCE
vs DIFFERENTIAL FULL-SCALE INPUT RANGE

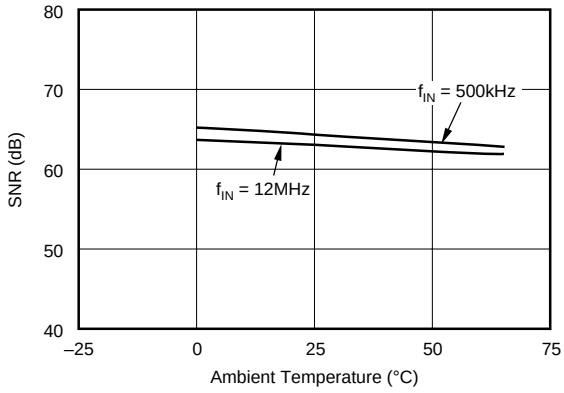



NOTE: $REFT_{EXT}$ varied, REFB is fixed at the internal value of +1.25V.

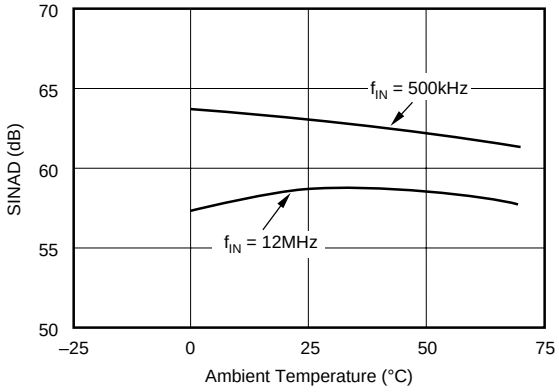
SPURIOUS FREE DYNAMIC RANGE (SFDR)
vs TEMPERATURE



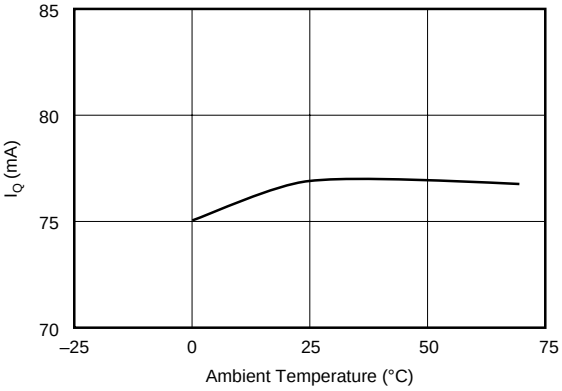

SIGNAL-TO-NOISE RATIO vs TEMPERATURE




SIGNAL-TO-(NOISE + DISTORTION)
vs TEMPERATURE



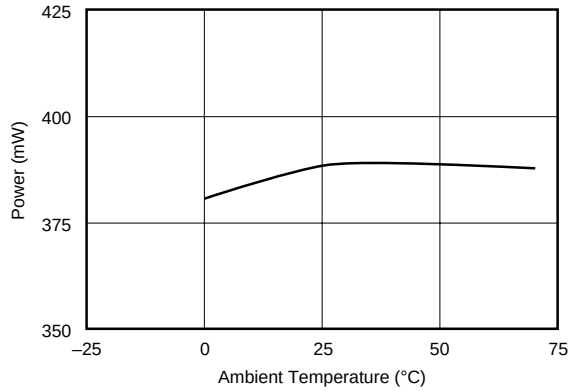

SUPPLY CURRENT vs TEMPERATURE



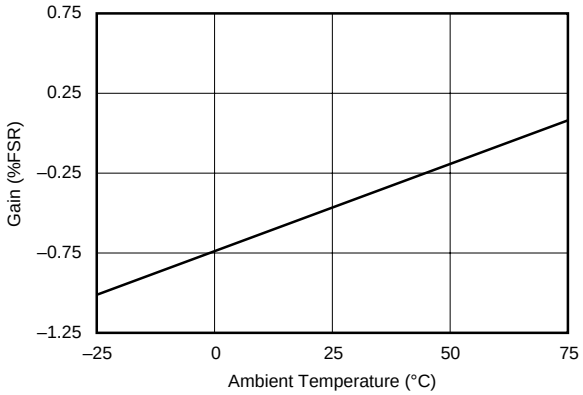
# TYPICAL PERFORMANCE CURVES (CONT)

At $T_A$ = +25°C, $V_S$ = +5V, Sampling Rate = 40MHz, with a 50% duty cycle clock having a 2ns rise/fall time, unless otherwise noted.

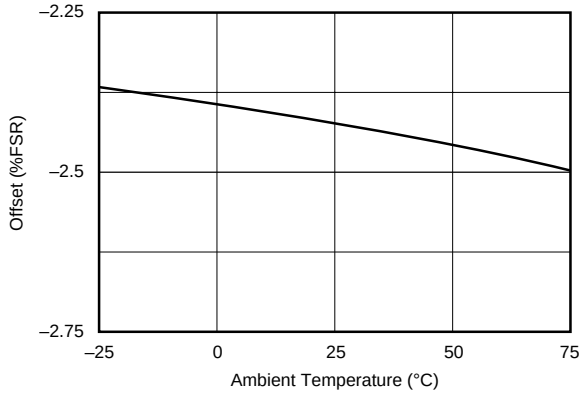
POWER DISSIPATION vs TEMPERATURE



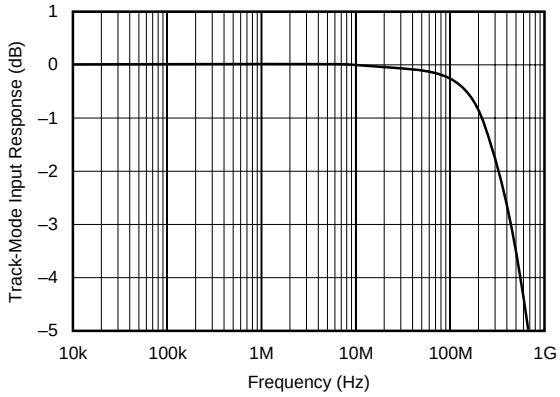

GAIN ERROR vs TEMPERATURE



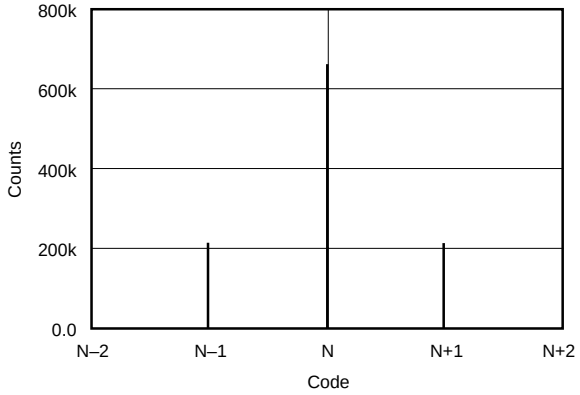

OFFSET ERROR vs TEMPERATURE




TRACK-MODE SMALL-SIGNAL INPUT BANDWIDTH




OUTPUT NOISE HISTOGRAM (NO SIGNAL)



## THEORY OF OPERATION

The ADS800 is a high speed sampling analog-to-digital converter with pipelining. It uses a fully differential architecture and digital error correction to guarantee 12-bit resolution. The differential track/hold circuit is shown in Figure 1. The switches are controlled by an internal clock which has a non-overlapping two phase signal, $\phi1$ and $\phi2$. At the sampling time the input signal is sampled on the bottom plates of the input capacitors. In the next clock phase, $\phi2$, the bottom plates of the input capacitors are connected together and the feedback capacitors are switched to the op amp output. At this time the charge redistributes between $C_I$ and $C_H$, completing one track/hold cycle. The differential output is a held DC representation of the analog input at the sample time. The track/hold circuit can also convert a single-ended input signal into a fully differential signal for the quantizer.

The pipelined quantizer architecture has 11 stages with each stage containing a two-bit quantizer and a two bit digital-to-analog converter, as shown in Figure 2. Each two-bit quantizer stage converts on the edge of the sub-clock, which is twice the frequency of the externally applied clock. The output of each quantizer is fed into its own delay line to

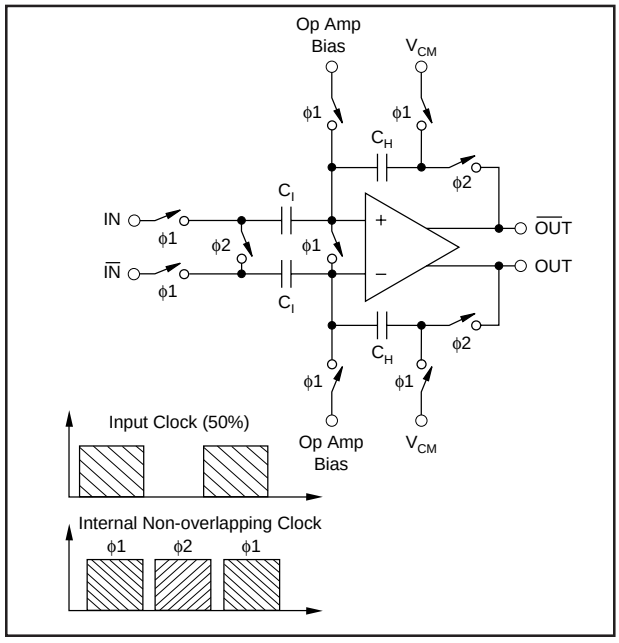



FIGURE 1. Input Track/Hold Configuration with Timing Signals.

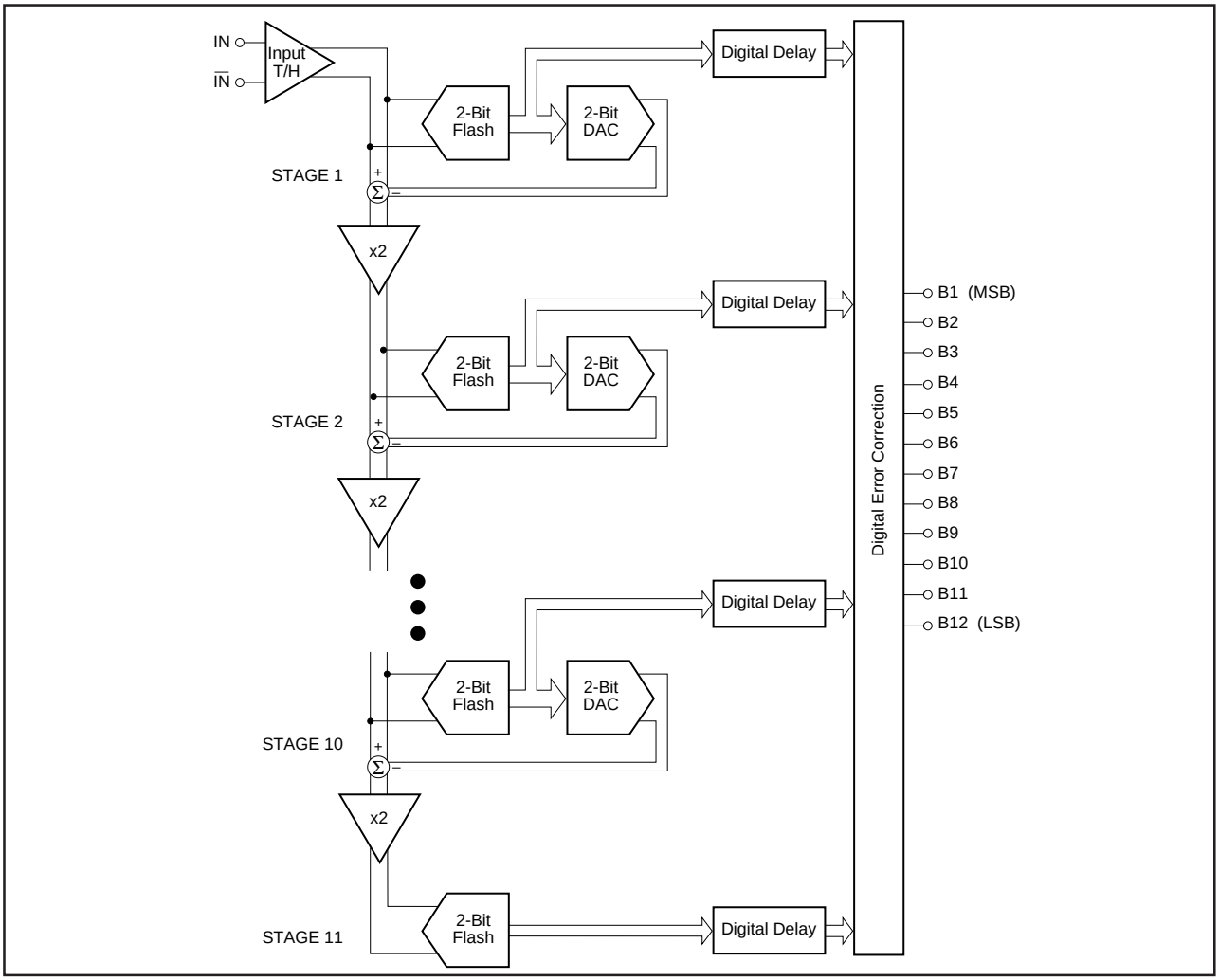



FIGURE 2. Pipeline A/D Architecture.

time-align it with the data created from the following quantizer stages. This aligned data is fed into a digital error correction circuit which can adjust the output data based on the information found on the redundant bits. This technique gives the ADS800 excellent differential linearity and guarantees no missing codes at the 12-bit level.

Since there are two pipeline stages per external clock cycle, there is a 6.5 clock cycle data latency from the start convert signal to the valid output data. The output data is available in Straight Offset Binary (SOB) or Binary Two's Complement (BTC) format.

## THE ANALOG INPUT AND INTERNAL REFERENCE

The analog input of the ADS800 can be configured in various ways and driven with different circuits, depending on the nature of the signal and the level of performance desired. The ADS800 has an internal reference that sets the full scale input range of the A/D. The differential input range has each input centered around the common-mode of +2.25V, with each of the two inputs having a full scale range of +1.25V to +3.25V. Since each input is 2V peak-to-peak and 180° out of phase with the other, a 4V differential input signal to the quantizer results. As shown in Figure 3, the positive full scale reference (REFT) and the negative full scale (REFB) are brought out for external bypassing. In addition, the common-mode voltage (CM) may be used as a reference to provide the appropriate offset for the driving circuitry. However, care must be taken not to appreciably load this reference node. For more information regarding external references, single-ended input, and ADS800 drive circuits, refer to the applications section.

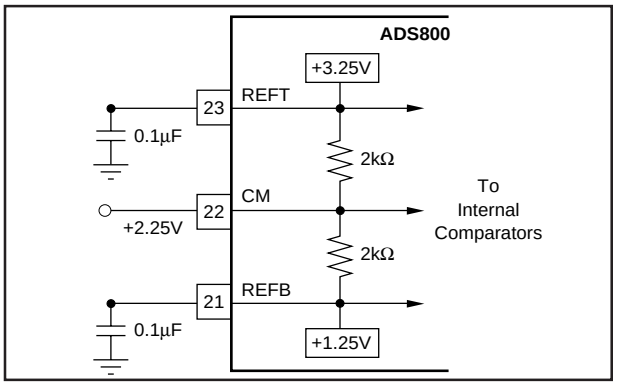



FIGURE 3. Internal Reference Structure.

## CLOCK REQUIREMENTS

The CLK pin accepts a CMOS level clock input. Both the rising and falling edges of the externally applied clock control the various interstage conversions in the pipeline. Therefore, the clock signal's jitter, rise/fall times and duty cycle can affect conversion performance.

- Low clock **jitter** is critical to SNR performance in frequency-domain signal environments.
- Clock **rise and fall times** should be as short as possible (<2ns for best performance).
- For most applications, the clock duty should be set to 50%. However, for applications requiring no missing codes, a slight skew in the duty cycle will improve DNL performance for conversion rates >35MHz and input frequencies <2MHz (see Timing Diagram) in the SOIC package. For the best performance in the SSOP package, the clock should be skewed under all input frequencies with conversion rates >35MHz. A possible method for skewing the 50% duty cycle source is shown in Figure 4.

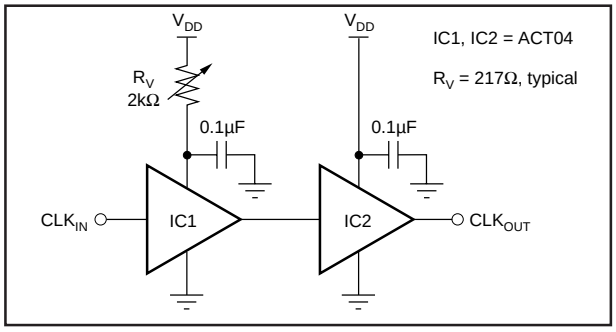



FIGURE 4. Clock Skew Circuit.

## DIGITAL OUTPUT DATA

The 12-bit output data is provided at CMOS logic levels. The standard output coding is Straight Offset Binary where a full scale input signal corresponds to all "1's" at the output. This condition is met with pin 19 "LO" or Floating due to an internal pull-down resistor. By applying a logic "HI" voltage to this pin, a Binary Two's Complement output will be provided where the most significant bit is inverted. The digital outputs of the ADS800 can be set to a high impedance state by driving $\overline{OE}$ (pin 18) with a logic "HI". Normal operation is achieved with pin 18 "LO" or Floating due to internal pull-down resistors. This function is provided for testability purposes and is not meant to drive digital buses directly or be dynamically changed during the conversion process.

| | OUTPUT CODE | |
|---|---|---|
| DIFFERENTIAL INPUT[1] | SOB PIN 19 FLOATING or LO | BTC PIN 19 HI |
| +FS (IN = +3.25V, $\overline{IN}$ = +1.25V) | 111111111111 | 011111111111 |
| +FS –1LSB | 111111111111 | 011111111111 |
| +FS –2LSB | 111111111110 | 011111111110 |
| +3/4 Full Scale | 111000000000 | 011000000000 |
| +1/2 Full Scale | 110000000000 | 010000000000 |
| +1/4 Full Scale | 101000000000 | 001000000000 |
| +1LSB | 100000000001 | 000000000001 |
| Bipolar Zero (IN = $\overline{IN}$ = +2.25V) | 100000000000 | 000000000000 |
| –1LSB | 011111111111 | 111111111111 |
| –1/4 Full Scale | 011000000000 | 111000000000 |
| –1/2 Full Scale | 010000000000 | 110000000000 |
| –3/4 Full Scale | 001000000000 | 101000000000 |
| –FS +1LSB | 000000000001 | 100000000001 |
| –FS (IN = +1.25V, $\overline{IN}$ = +3.25V) | 000000000000 | 100000000000 |
| Note: In the single-ended input mode, +FS = +4.25V and –FS = +0.25V. | | |

TABLE I. Coding Table for the ADS800.

# APPLICATIONS

## DRIVING THE ADS800

The ADS800 has a differential input with a common-mode of +2.25V. For AC-coupled applications, the simplest way to create this differential input is to drive the primary winding of a transformer with a single-ended input. A differential output is created on the secondary if the center tap is tied to the common-mode voltage of +2.25V per Figure 5. This transformer-coupled input arrangement provides good high frequency AC performance. It is important to select a transformer that gives low distortion and does not exhibit core saturation at full scale voltage levels. Since the transformer does not appreciably load the ladder, there is no need to buffer the common-mode (CM) output in this instance. In general, it is advisable to keep the current draw from the CM output pin below 0.5µA to avoid nonlinearity in the internal reference ladder. A FET input operational amplifier such as the OPA130 can provide a buffered reference for driving external circuitry. The analog IN and $\overline{IN}$ inputs should be bypassed with 22pF capacitors to minimize track/hold glitches and to improve high input frequency performance.

Figure 6 illustrates another possible low cost interface circuit which utilizes resistors and capacitors in place of a transformer. Depending on the signal bandwidth, the component values should be carefully selected in order to maintain the performance outlined in the data sheet. The input capacitors, $C_{IN}$, and the input resistors, $R_{IN}$, create a high-pass filter with the lower corner frequency at $f_C = 1/(2\pi R_{IN}C_{IN})$. The corner frequency can be reduced by either increasing the value of $R_{IN}$ or $C_{IN}$. If the circuit operates with a 50Ω or 75Ω impedance level, the resistors are fixed and only the value of the capacitor can be increased. Usually AC-coupling capacitors are electrolytic or tantalum capacitors with values of 1µF or higher. It should be noted that these large capacitors become inductive with increased input frequency, which could lead to signal amplitude errors or oscillation. To maintain a low AC-coupling impedance throughout the signal band, a small value (e.g. 1µF) ceramic capacitor could be added in parallel with the polarized capacitor.

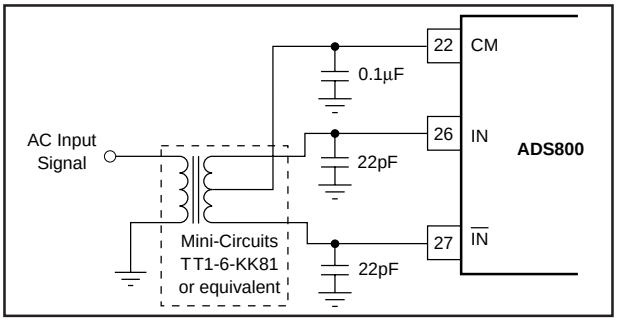



FIGURE 5. AC-Coupled Single-Ended to Differential Drive Circuit Using a Transformer.

Capacitors $C_{SH1}$ and $C_{SH2}$ are used to minimize current glitches resulting from the switching in the input track and hold stage and to improve signal-to-noise performance. These capacitors can also be used to establish a low-pass filter and effectively reduce the noise bandwidth. In order to create a real pole, resistors $R_{SER1}$ and $R_{SER2}$ were added in series with each input. The cut-off frequency of the filter is determined by $f_C = 1/(2\pi R_{SER}\bullet(C_{SH}+C_{ADC}))$ where $R_{SER}$ is the resistor in series with the input, $C_{SH}$ is the external capacitor from the input to ground, and $C_{ADC}$ is the internal input capacitance of the A/D converter (typically 4pF).

Resistors $R_1$ and $R_2$ are used to derive the necessary common mode voltage from the buffered top and bottom references. The total load of the resistor string should be selected so that the current does not exceed 1mA. Although the circuit in Figure 6 uses two resistors of equal value so that the common mode voltage is centered between the top and bottom reference (+2.25V), it is not necessary to do so. In all cases the center point, $V_{CM}$, should be bypassed to ground in order to provide a low impedance AC ground.

If the signal needs to be DC coupled to the input of the ADS800, an operational amplifier input circuit is required. In the differential input mode, any single-ended signal must be modified to create a differential signal. This can be

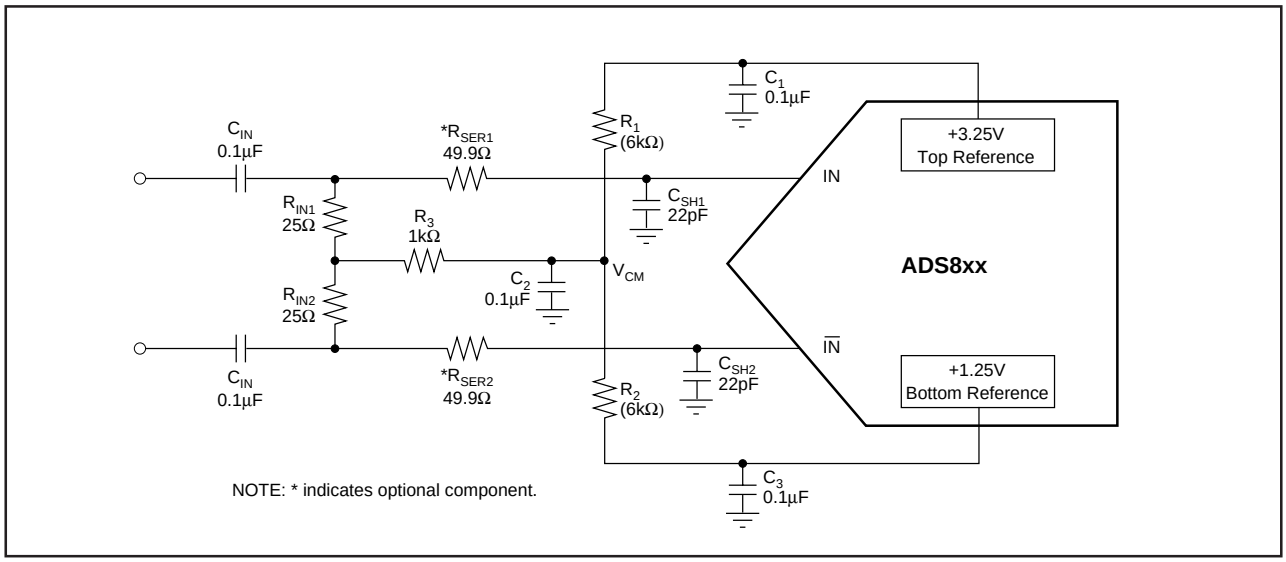



FIGURE 6. AC-Coupled Differential Input Circuit.

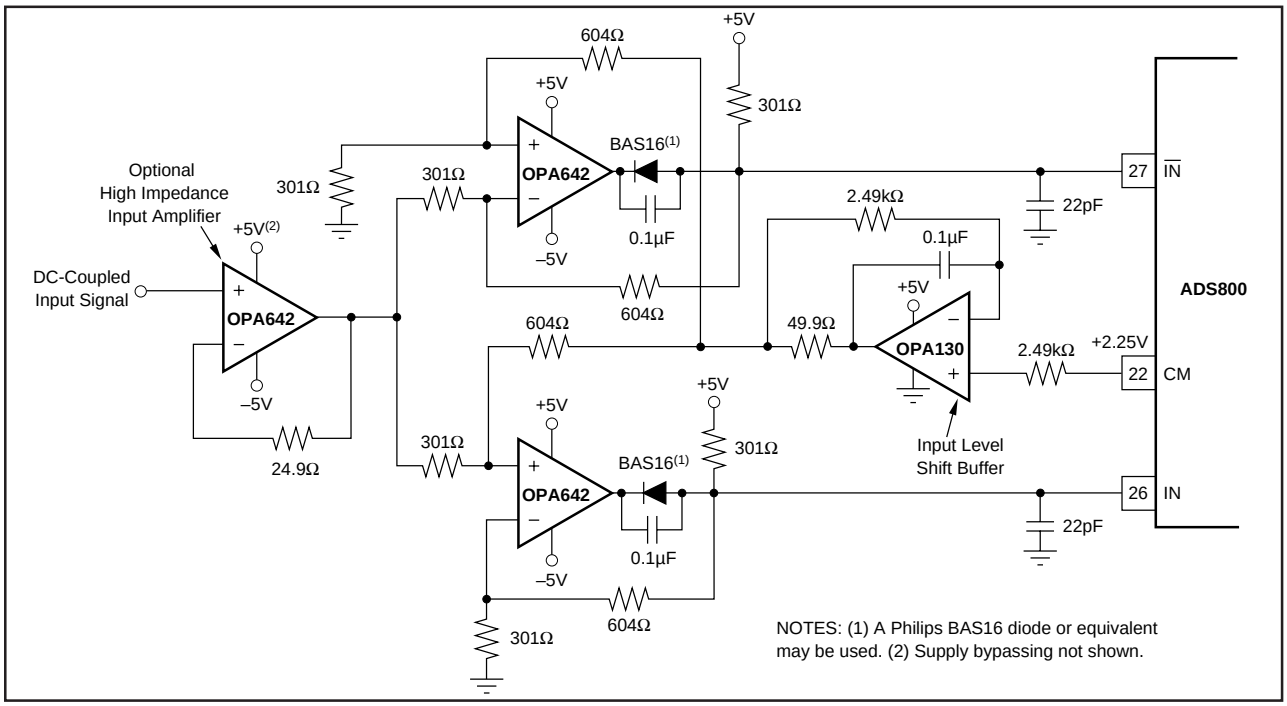



FIGURE 7. A Low Distortion DC-Coupled, Single-Ended to Differential Input Driver Circuit.

accomplished by using two operational amplifiers, one in the noninverting mode for the input and the other amplifier in the inverting mode for the complementary input. The low distortion circuit in Figure 7 will provide the necessary input shifting required for signals centered around ground. It also employs a diode for output level shifting to guarantee a low distortion +3.25V output swing. Other amplifiers can be used in place of the OPA642s if the lowest distortion is not necessary. If output level shifting circuits are not used, care must be taken to select operational amplifiers that give the necessary performance when swinging to +3.25V with a ±5V supply operational amplifier.

The ADS800 can also be configured with a single-ended input full scale range of +0.25V to +4.25V by tying the complementary input to the common-mode reference voltage as shown in Figure 8. This configuration will result in increased even-order harmonics, especially at higher input frequencies. However, this tradeoff may be quite acceptable for time-domain applications. The driving amplifier must give adequate performance with a +0.25V to +4.25V output swing in this case.

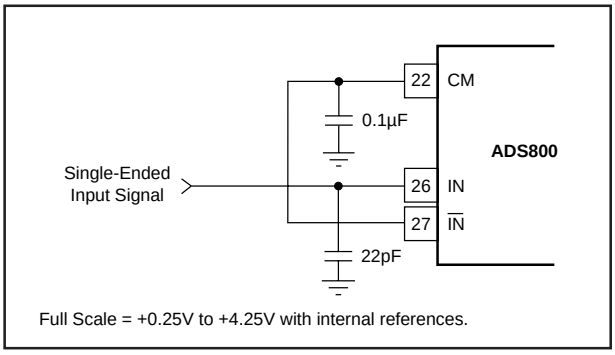



FIGURE 8. Single-Ended Input Connection.

## EXTERNAL REFERENCES AND ADJUSTMENT OF FULL SCALE RANGE

The internal reference buffers are limited to approximately 1mA of output current. As a result, these internal +1.25V and +3.25V references may be overridden by external references that have at least 18mA (at room temperature) of output drive capability. In this instance, the common-mode voltage will be set halfway between the two references. This feature can be used to adjust the gain error, improve gain drift, or to change the full scale input range of the ADS800. Changing the full scale range to a lower value has the benefit of easing the swing requirements of external input drive amplifiers. The external references can vary as long as the value of the external top reference ($REFT_{EXT}$) is less than or equal to +3.4V and the value of the external bottom reference ($REFB_{EXT}$) is greater than or equal to +1.1V and the difference between the external references are greater than or equal to 1.5V.

For the differential configuration, the full scale input range will be set to the external reference values that are selected. For the single-ended mode, the input range is $2 \bullet (REFT_{EXT} - REFB_{EXT})$, with the common-mode being centered at $(REFT_{EXT} + REFB_{EXT})/2$. Refer to the typical performance curves for expected performance vs full scale input range.

The circuit in Figure 10 works completely on a single +5V supply. As a reference element, it uses the micro-power reference REF1004-2.5, which is set to a quiescent current of 0.1mA. Amplifier $A_2$ is configured as a follower to buffer the +1.25V generated from the resistor divider. To provide the necessary current drive, a pull-down resistor, $R_P$ is added.

Amplifier $A_1$ is configured as an adjustable gain stage, with a range of approximately 1 to 1.32. The pull-up resistor again relieves the op amp from providing the full current drive. The value of the pull-up/down resistors is not critical and can be varied to optimize power consumption. The need for pull-up/down resistors depends only on the drive capability of the selected drive amplifiers and thus can be omitted.

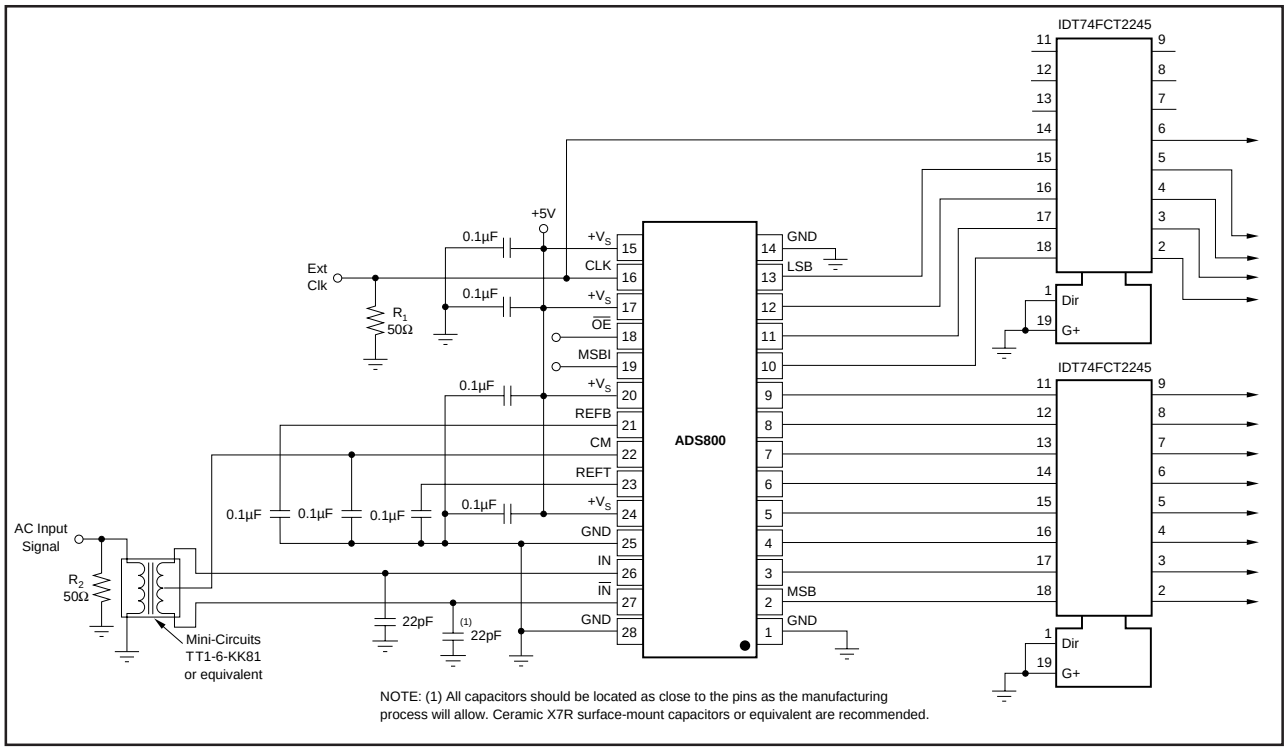



FIGURE 9. ADS800 Interface Schematic with AC-Coupling and External Buffers.

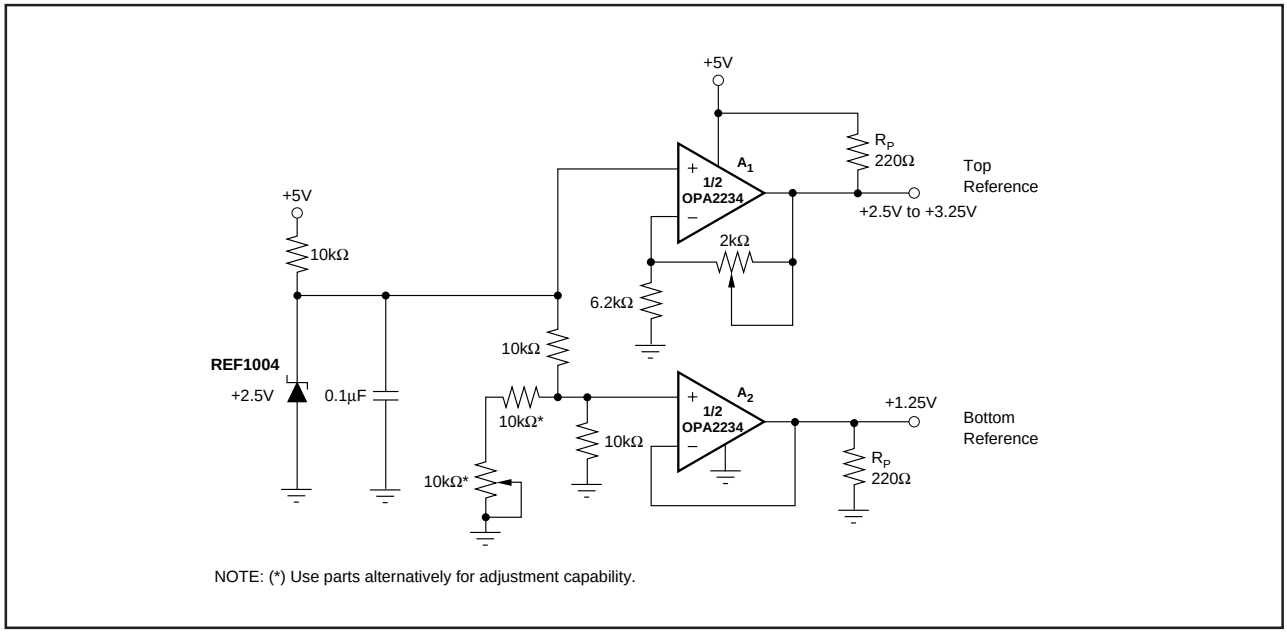



FIGURE 10. Optional External Reference to Set the Full-Scale Range Utilizing a Dual, Single-Supply Op Amp.

## PC BOARD LAYOUT AND BYPASSING

A well-designed, clean PC board layout will assure proper operation and clean spectral response. Proper grounding and bypassing, short lead lengths, and the use of ground planes are particularly important for high frequency circuits. Multilayer PC boards are recommended for best performance but if carefully designed, a two-sided PC board with large, heavy ground planes can give excellent results. It is recommended that the analog and digital ground pins of the ADS800 be connected directly to the analog ground plane. In our experience, this gives the most consistent results. The A/D power supply commons should be tied together at the analog ground plane. Power supplies should be bypassed with 0.1µF ceramic capacitors as close to the pin as possible.

## DYNAMIC PERFORMANCE TESTING

The ADS800 is a high performance converter and careful attention to test techniques is necessary to achieve accurate results. Highly accurate phase-locked signal sources allow high resolution FFT measurements to be made without using data windowing functions. A low jitter signal generator such as the HP8644A for the test signal, phase-locked with a low jitter HP8022A pulse generator for the A/D clock, gives excellent results. Low pass filtering (or bandpass filtering) of test signals is absolutely necessary to test the low distortion of the ADS800. Using a signal amplitude slightly lower than full scale will allow a small amount of "headroom" so that noise or DC offset voltage will not overrange the A/D and cause clipping on signal peaks.

## DYNAMIC PERFORMANCE DEFINITIONS

1. Signal-to-Noise-and-Distortion Ratio (SINAD):

$$10 \log \frac{\text{Sinewave Signal Power}}{\text{Noise + Harmonic Power (first 15 harmonics)}}$$

2. Signal-to-Noise Ratio (SNR):

$$10 \log \frac{\text{Sinewave Signal Power}}{\text{Noise Power}}$$

3. Intermodulation Distortion (IMD):

$$10 \log \frac{\text{Highest IMD Product Power (to 5th-order)}}{\text{Sinewave Signal Power}}$$

IMD is referenced to the larger of the test signals $f_1$ or $f_2$. Five "bins" either side of peak are used for calculation of fundamental and harmonic power. The "0" frequency bin (DC) is not included in these calculations as it is of little importance in dynamic signal processing applications.