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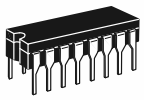
Dual 3-Input/3-Ouput OR Gate

MC10110

The MC10110 is designed to drive up to three transmission lines simul–taneously. The multiple outputs of this device also allow the wire “OR”–ing of several levels of gating for minimization of gate and package count.

The ability to control three parallel lines from a single point makes the MC10110 particularly useful in clock distribution applications where minimum clock skew is desired. Three V_{CC} pins are provided and each one should be used.

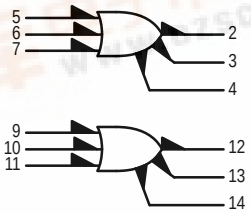
P_D = 80 mW typ/pkg (No Load)
t_{pd} = 2.4 ns typ (All Outputs Loaded)
t_r, t_f = 2.2 ns typ (20%–80%)



L SUFFIX
CERAMIC PACKAGE
CASE 620–10

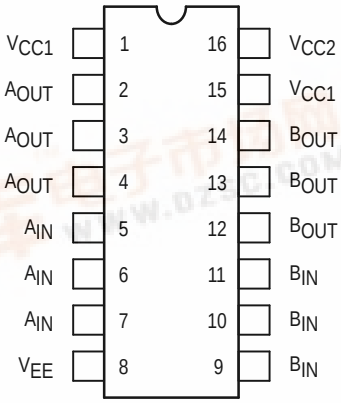
P SUFFIX
PLASTIC PACKAGE
CASE 648–08

LOGIC DIAGRAM



V_{CC1} = PIN 1, 15
V_{CC2} = PIN 16
V_{EE} = PIN 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package. For PLCC pin assignment, see the Pin Conversion Tables on page 6–36 of the Motorola MECL Data Book (DL122/D).

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ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			–30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		42		30	38		42	mAdc
Input Current	I_{inH}	5, 6, 7		680			425		425	µAdc
	I_{inL}	5, 6, 7	0.5		0.5			0.3		µAdc
Output Voltage Logic 1	V_{OH}	2 3 4	–1.060 –1.060 –1.060	–0.890 –0.890 –0.890	–0.960 –0.960 –0.960		–0.810 –0.810 –0.810	–0.890 –0.890 –0.890	–0.700 –0.700 –0.700	Vdc
Output Voltage Logic 0	V_{OL}	2 3 4	–1.890 –1.890 –1.890	–1.675 –1.675 –1.675	–1.850 –1.850 –1.850		–1.650 –1.650 –1.650	–1.825 –1.825 –1.825	–1.615 –1.615 –1.615	Vdc
Threshold Voltage Logic 1	V_{OHA}	2 3 4	–1.080 –1.080 –1.080		–0.980 –0.980 –0.980			–0.910 –0.910 –0.910		Vdc
Threshold Voltage Logic 0	V_{OLA}	2 3 4		–1.655 –1.655 –1.655			–1.630 –1.630 –1.630		–1.595 –1.595 –1.595	Vdc
Switching Times (50Ω Load)										ns
Propagation Delay	t_{5+2+} t_{5-2-} t_{5+3+} t_{5-3-} t_{5+4+} t_{5-4-}	2 2 3 3 4 4	1.4 1.4 1.4 1.4 1.4 1.4	3.5 3.5 3.5 3.5 3.5 3.5	1.4 1.4 1.4 1.4 1.4 1.4	2.4 2.4 2.4 2.4 2.4 2.4	3.5 3.5 3.5 3.5 3.5 3.5	1.5 1.5 1.5 1.5 1.5 1.5	3.8 3.8 3.8 3.8 3.8 3.8	
Rise Time (20 to 80%)	t_{2+} t_{3+} t_{4+}	2 3 4	1.0 1.0 1.0	3.5 3.5 3.5	1.1 1.1 1.1	2.2 2.2 2.2	3.5 3.5 3.5	1.2 1.2 1.2	3.8 3.8 3.8	
Fall Time (20 to 80%)	t_{2-} t_{3-} t_{4-}	2 3 4	1.0 1.0 1.0	3.5 3.5 3.5	1.1 1.1 1.1	2.2 2.2 2.2	3.5 3.5 3.5	1.2 1.2 1.2	3.8 3.8 3.8	

ELECTRICAL CHARACTERISTICS (continued)

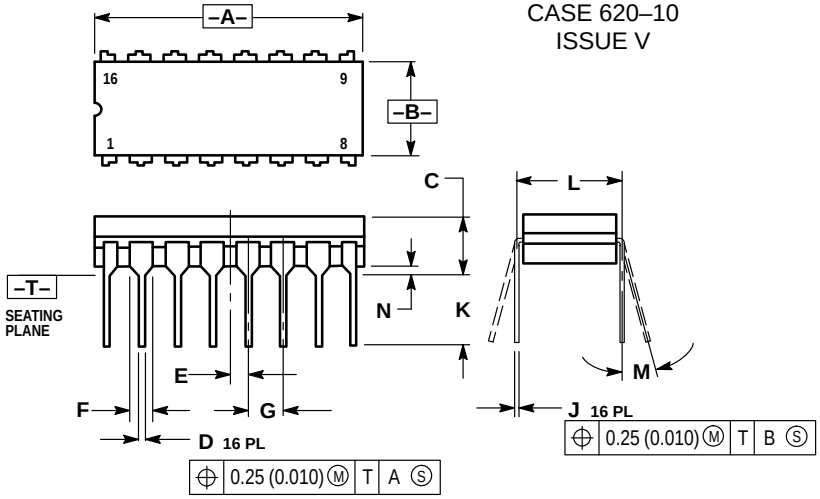
			TEST VOLTAGE VALUES (Volts)					
		@ Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
		–30°C	–0.890	–1.890	–1.205	–1.500	–5.2	
		+25°C	–0.810	–1.850	–1.105	–1.475	–5.2	
		+85°C	–0.700	–1.825	–1.035	–1.440	–5.2	
Characteristic	**Symbol**	**Pin Under Test**	**TEST VOLTAGE APPLIED TO PINS LISTED BELOW**					**(V_{CC}) Gnd**
			V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
Power Supply Drain Current	I_E	8					8	1, 15, 16
Input Current	I_{inH}	5, 6, 7	*				8	1, 15, 16
	I_{inL}	5, 6, 7		*			8	1, 15, 16
Output Voltage Logic 1	V_{OH}	2	5				8	1, 15, 16
		3	6				8	1, 15, 16
		4	7				8	1, 15, 16
Output Voltage Logic 0	V_{OL}	2					8	1, 15, 16
		3					8	1, 15, 16
		4					8	1, 15, 16
Threshold Voltage Logic 1	V_{OHA}	2			5		8	1, 15, 16
		3			6		8	1, 15, 16
		4			7		8	1, 15, 16
Threshold Voltage Logic 0	V_{OLA}	2				5	8	1, 15, 16
		3				6	8	1, 15, 16
		4				7	8	1, 15, 16
Switching Times (50Ω Load)					**Pulse In**	**Pulse Out**	**–3.2 V**	**+2.0 V**
Propagation Delay	t_{5+2+}	2			5	2	8	1, 15, 16
	t_{5-2-}	2			5	2	8	1, 15, 16
	t_{5+3+}	3			5	3	8	1, 15, 16
	t_{5-3-}	3			5	3	8	1, 15, 16
	t_{5+4+}	4			5	4	8	1, 15, 16
	t_{5-4-}	4			5	4	8	1, 15, 16
Rise Time (20 to 80%)	t_{2+}	2			5	2	8	1, 15, 16
	t_{3+}	3			5	3	8	1, 15, 16
	t_{4+}	4			5	4	8	1, 15, 16
Fall Time (20 to 80%)	t_{2-}	2			5	2	8	1, 15, 16
	t_{3-}	3			5	3	8	1, 15, 16
	t_{4-}	4			5	4	8	1, 15, 16

* Individually test each input using the pin connections shown.

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

OUTLINE DIMENSIONS

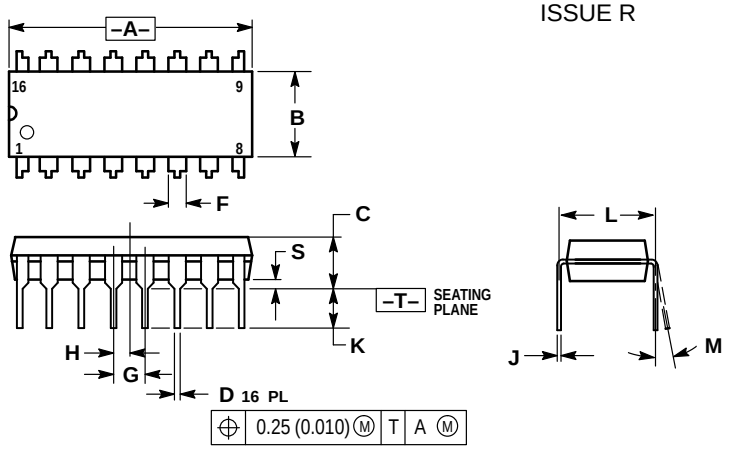
L SUFFIX
CERAMIC DIP PACKAGE
CASE 620–10
ISSUE V



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

P SUFFIX
PLASTIC DIP PACKAGE
CASE 648–08
ISSUE R



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

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