

## Quad Bus Receiver

The MC10129 data inputs are compatible with, and accept TTL logic levels as well as levels compatible with IBM-type buses. The clock, strobe, and reset inputs accept MECL 10,000 logic levels.

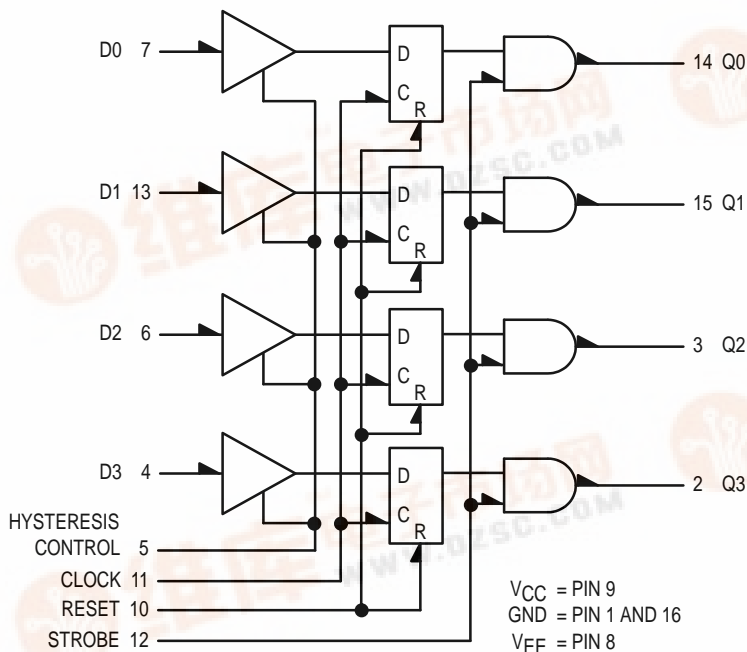
The data inputs accept the bus levels, and storage elements are provided to yield temporary latch storage of the information after receiving it from the bus. The outputs can be strobed to allow accurate synchronization of signals and/or connection to MECL 10,000 level buses. When the clock is low, and the reset input is disabled, the outputs will follow the D inputs. The latches will store the data on the rising edge of the clock. The outputs are enabled when the strobe input is high. Unused D inputs must be tied to  $V_{CC}$  or Gnd. The clock, strobe, and reset inputs each have 50 k ohm pulldown resistors to  $V_{EE}$ . They may be left floating, if not used.

The MC10129 will operate in either of two modes. The first mode is obtained by tying the hysteresis control input to  $V_{EE}$ . In this mode, the input threshold points of the D inputs are fixed. The second mode is obtained by tying the hysteresis control input to ground. In this mode, input hysteresis is achieved as shown in the test table. This hysteresis is desirable where extra noise margin is required on the D inputs. The outer input pins are unaffected by the mode of operation used.

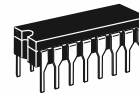
The MC10129 is especially useful in interface applications for central processors, mini-computers, and peripheral equipment.

$P_D = 750 \text{ mW typ/pkg (No Load)}$   
 $t_{pd} = 10 \text{ ns typ}$   
 $V_{CC \text{ Max}} = 7.0 \text{ Vdc}$

### LOGIC DIAGRAM

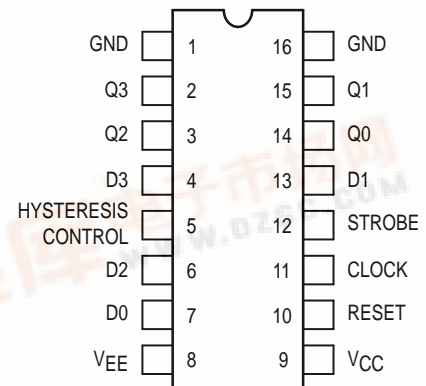


## MC10129



**L SUFFIX**  
 CERAMIC PACKAGE  
 CASE 620-10

### PIN ASSIGNMENT



### TRUTH TABLE

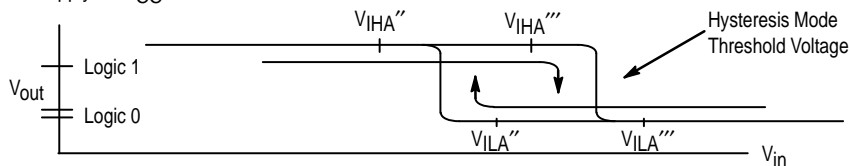
D	C	STROBE	RESET	$Q_{n+1}$
X	X	L	X	L
X	H	X	H	L
L	L	H	X	L
X	H	H	L	$Q_n$
H	L	H	X	H



**ELECTRICAL CHARACTERISTICS**

Characteristic	Symbol	Pin Under Test	Test Limits						Unit	
			-30°C		+25°C		+85°C			
			Min	Max	Min	Typ	Max	Min		Max
Negative Power Supply Drain Current	$I_E$	8 8		167 189			152 172		167 189	mAdc
Positive Power Supply Drain Current	$I_{CC}$	9		8.0			8.0		8.0	mAdc
Input Current	$I_{inH}$	4		150			95		95	$\mu$ Adc
		6		150			95		95	
		7		150			95		95	
10			720			450		450		
11			390			245		245		
12			390			245		245		
13			150			95		95		
	$I_{CBO} (1.)$	4		1.5			-1.0		1.0	$\mu$ Adc
		6		1.5			-1.0		1.0	
		7		1.5			-1.0		1.0	
		13			-1.0					
	$I_{inL}$	10	0.5		0.5			0.3		$\mu$ Adc
		11	0.5		0.5			0.3		
		12	0.5		0.5			0.3		
Output Voltage Logic 1	$V_{OH}$	2	-1.060	-0.890	-0.960		-0.810	-0.890	-0.700	Vdc
		3	-1.060	-0.890	-0.960		-0.810	-0.890	-0.700	
		2	-1.060	-0.890	-0.960		-0.810	-0.890	-0.700	
		3	-1.060	-0.890	-0.960		-0.810	-0.890	-0.700	
Output Voltage Logic 0	$V_{OL}$	2	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615	Vdc
		3	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615	
		2	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615	
		3	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615	
Threshold Voltage Logic 1	$V_{OHA}$	2 (2.)	-1.080		-0.980			-0.910		Vdc
		2	-1.080		-0.980			-0.910		
		2	-1.080		-0.980			-0.910		
		2	-1.080		-0.980			-0.910		
		2 (3.)	-1.080		-0.980			-0.910		
		2 (4.)	-1.080		-0.980			-0.910		
Threshold Voltage Logic 0	$V_{OLA}$	2 (2.)		-1.655			-1.630		-1.595	Vdc
		2		-1.655			-1.630		-1.595	
		2 (2.)		-1.655			-1.630		-1.595	
		2		-1.655			-1.630		-1.595	
		2 (3.)		-1.655			-1.630		-1.595	
		2 (4.)		-1.655			-1.630		-1.595	
Switching Times Propagation Delay									ns	
Data Input	$t_{7+14+}$ $t_{7-14-}$	14	3.7	15	3.7	10	15	3.7	30	
		14	3.7	15	3.7	10	15	3.7	40	
Clock Input	$t_{11-14+}$ $t_{11-14-}$	14	2.7	11	2.7	5.0	9.0	2.7	11	
		14	2.7	11	2.7	5.0	9.0	2.7	11	
Strobe Input	$t_{12+14+}$ $t_{12-14-}$	14	1.6	8.0	1.6	4.0	7.0	1.6	8.0	
		14	1.6	8.0	1.6	4.0	7.0	1.6	8.0	
Reset Input	$t_{10+14-}$	14	2.0	8.0	2.0	5.0	6.5	2.0	8.0	
Hysteresis Mode	$t_{7+14+}$ $t_{7-14-}$	14	6.6	30	6.7	18	25	6.6	30	
		14	3.7	17	3.7	10	15	3.7	40	
Setup Time	$t_{setup}$	14	30		2.7	15		30		
Hold Time	$t_{hold}$	14	0		-2.0	15		-2.0		
Rise Time	$t_+$	14	1.5	5.0	1.5	2.0	4.3	1.5	5.0	
Fall Time	$t_-$	14	1.5	5.0	1.5	2.0	4.3	1.5	5.0	

- Pin 5 to  $V_{EE}$ ,  $V_{IL}$  to Data input one at a time.
- Output latched to logic high state prior to test.  $V_{IHA}'$ ,  $V_{ILA}'$  are standard logic 1 and logic 0 MTTL threshold voltages.  $V_{IHA}''$ ,  $V_{ILA}''$ ,  $V_{IHA}'''$  and  $V_{ILA}'''$  are logic 1 and logic 0 threshold voltages in the hysteresis mode as shown in Figure 1 on page 3-2.
- Input level on data input taken from +0.4V up to voltage level given.
- Input level on data input taken from +4.0V down to voltage level given.
- Operation and limits shown also apply for  $V_{CC} = +6.0V$ .



**Figure 1. Hysteresis Mode Threshold Voltage**

## ELECTRICAL CHARACTERISTICS

			TEST VOLTAGE VALUES (Volts)							Gnd		
			MECL 10,000 INPUT LEVELS				TTL INPUT LEVELS (6.)					
			V <sub>IHmax</sub>	V <sub>ILmin</sub>	V <sub>IHAmin</sub>	V <sub>ILAmx</sub>	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IHA'</sub>		V <sub>ILA'</sub>	
			@ Test Temperature	-30°C	+25°C	+85°C						
			-0.890	-1.890	-1.155	-1.500	3.000	0.400	2.000	0.800		
			-0.810	-1.850	-1.105	-1.475	3.000	0.400	2.000	0.800		
			-0.700	-1.825	-1.035	-1.440	3.000	0.400	2.000	0.800		
Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW							Gnd		
			V <sub>IHmax</sub>	V <sub>ILmin</sub>	V <sub>IHAmin</sub>	V <sub>ILAmx</sub>	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IHA'</sub>		V <sub>ILA'</sub>	
Negative Power Supply Drain Current	I <sub>E</sub>	8 8	11 11	12 12							1,5,16 1,16	
Positive Power Supply Drain Current	I <sub>CC</sub>	9						4,6,7,13			1,16	
Input Current	I <sub>inH</sub>	4 6 7 10 11 12 13	10,11 11 12				4 6 7 13				1,16 1,16 1,16 1,16 1,16 1,16 1,16	
		I <sub>CBO</sub> (1.)	4 6 7 13					4 6 7 13			1,16 1,16 1,16 1,16	
		I <sub>inL</sub>	10 11 12	10 11 12							1,16 1,16 1,16	
Output Voltage Logic 1	V <sub>OH</sub>	2 3 2 3	12 12 12 12	10,11 10,11 10,11 10,11			4 6 4 6				1,16 1,16 1,5,16 1,5,16	
		Output Voltage Logic 0	V <sub>OL</sub>	2 3 2 3	12 12 12 12	10,11 10,11 10,11 10,11			4 6 4 6			1,16 1,16 1,5,16 1,5,16
				Threshold Voltage Logic 1	V <sub>OHA</sub>	2 (2.) 2 2 2 2 (3.) 2 (4.)	11,12 10,12 12 12 12 12	10,11 10,11 10,11 10,11 10,11 10,11	12 12 10 11	4 4 4		4
Threshold Voltage Logic 0	V <sub>OLA</sub>					2 (2.) 2 2 (2.) 2 2 (3.) 2 (4.)	11,12 10,12 12 12 12 12	10,11 10,11 10,11 10,11 10,11 10,11	10 11	4 4 4		4
		Switching Times Propagation Delay										Figure
				+1.11V	+0.31V							
Data Input	t <sub>7+14+</sub> t <sub>7-14-</sub>	14 14	12 12	10,11 10,11	7 7	14 14				Figure 3 Figure 3	1,16 1,16	
			Clock Input	t <sub>11-14+</sub> t <sub>11-14-</sub>	14 14	12 12	10 10	7,11 7,11	14 14			Figure 6 Figure 6
Strobe Input	t <sub>12+14+</sub> t <sub>12-14-</sub>	14 14				10,11 10,11	12 12	14 14	7 7			Figure 4 Figure 4
			Reset Input	t <sub>10+14-</sub>	14	12		10,11	14	7	7	Figure 5
Hysteresis Mode	t <sub>7+14+</sub> t <sub>7-14-</sub>	14 14	12 12	10,11 10,11	7 7	14 14				Figure 3 Figure 3	1,5,16 1,5,16	
			Setup Time	t <sub>setup</sub>	14	12	10	7,11	14			Figure 7
Hold Time	t <sub>hold</sub>	14	12	10	7,11	14				Figure 7	1,16	
Rise Time	t <sub>+</sub>	14	12	10,11	7	14				Figure 3	1,16	
Fall Time	t <sub>-</sub>	14	12	10,11	7	14				Figure 3	1,16	

- Pin 5 to V<sub>EE</sub>, V<sub>IL</sub> to Data input one at a time.
- Output latched to logic high state prior to test. V<sub>IHA'</sub>, V<sub>ILA'</sub> are standard logic 1 and logic 0 MTTL threshold voltages. V<sub>IHA''</sub>, V<sub>ILA''</sub>, V<sub>IHA'''</sub> and V<sub>ILA'''</sub> are logic 1 and logic 0 threshold voltages in the hysteresis mode as shown in Figure 1 on page 3-2.
- Input level on data input taken from +0.4V up to voltage level given.
- Input level on data input taken from +4.0V down to voltage level given.
- Operation and limits shown also apply for V<sub>CC</sub> = +6.0V.
- When testing, choose either TTL or IBM input levels.

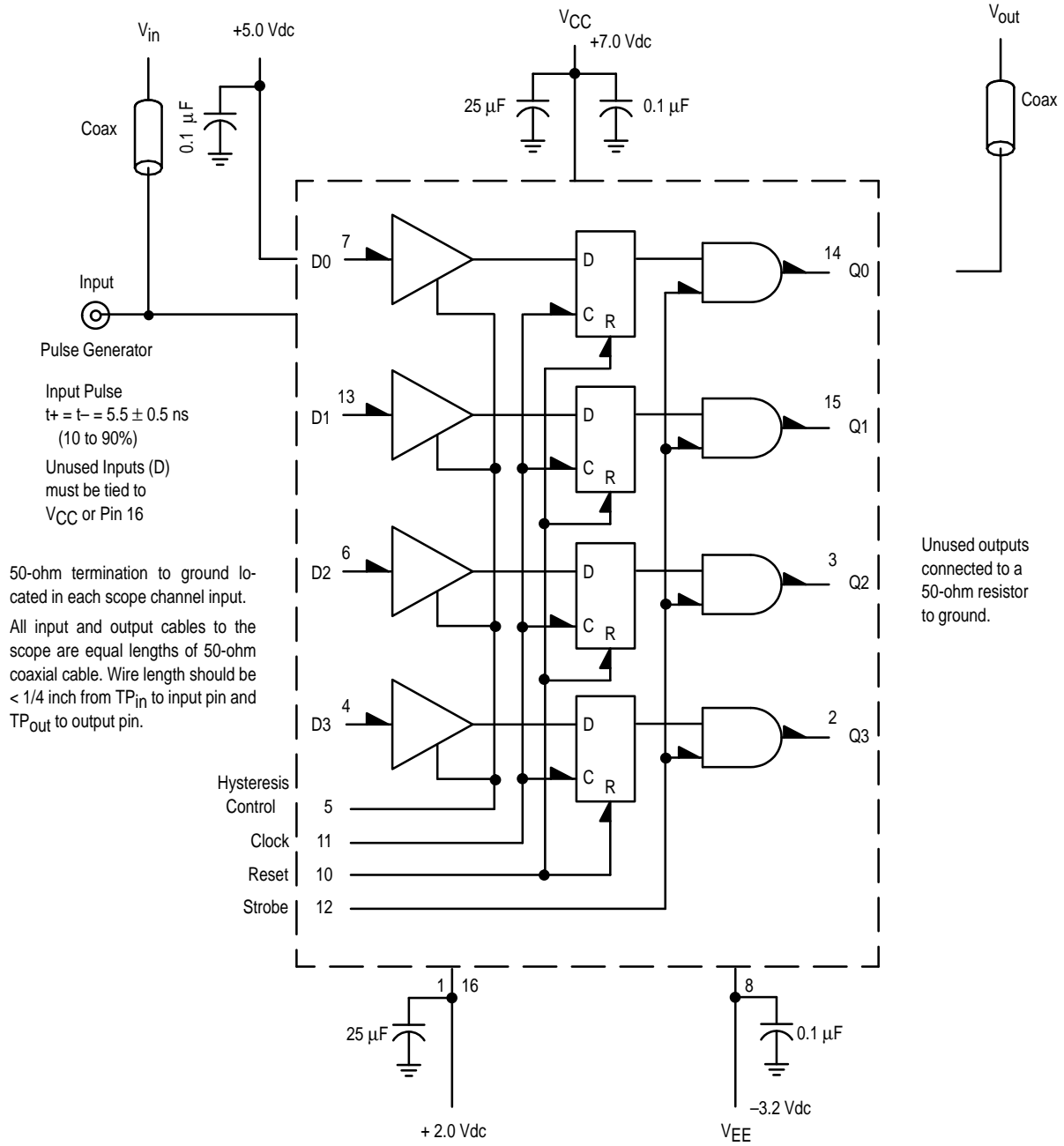
MC10129

ELECTRICAL CHARACTERISTICS

@ Test Temperature -30°C +25°C +85°C			TEST VOLTAGE VALUES (Volts)									Gnd	
			IBM INPUT LEVELS (6.)				HYSTERESIS MODE				V <sub>CC</sub> (5.)		V <sub>EE</sub>
			V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IHA'</sub>	V <sub>ILA'</sub>	V <sub>IHA''</sub>	V <sub>ILA''</sub>	V <sub>IHA'''</sub>	V <sub>ILA'''</sub>			
			3.11	0.150			2.90	2.00	2.20	1.30	+5.0		-5.2
			3.11	0.150	1.700	0.70	2.60	1.70	1.90	1.00	+5.0		-5.2
3.11	0.150			2.30	1.40	1.60	0.70	+5.0	-5.2				
Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW									Gnd	
			V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IHA'</sub>	V <sub>ILA'</sub>	V <sub>IHA''</sub>	V <sub>ILA''</sub>	V <sub>IHA'''</sub>	V <sub>ILA'''</sub>	V <sub>CC</sub> (5.)		V <sub>EE</sub>
Negative Power Supply Drain Current	I <sub>E</sub>	8 8								9 9	8 5,8	1,5,16 1,16	
Positive Power Supply Drain Current	I <sub>CC</sub>	9		4,6, 7,13						9 9	5,8 5,8	1,16 1,16	
Input Current	I <sub>inH</sub>	4	4							9	8	1,16	
		6	6							9	8	1,16	
		7	7							9	8	1,16	
		10								9	8	1,16	
		11								9	8	1,16	
	12								9	8	1,16		
		13	13							9	8	1,16	
	I <sub>CBO</sub> (1-)	4		4						9	8	1,16	
		6		6						9	8	1,16	
		7		7						9	8	1,16	
		13		13						9	8	1,16	
	I <sub>inL</sub>	10								9	8	1,16	
		11								9	8	1,16	
		12								9	8	1,16	
Output Voltage Logic 1	V <sub>OH</sub>	2	4							9	5,8	1,16	
		3	6							9	5,8	1,16	
		2	4							9	8	1,5,16	
		3	6							9	8	1,5,16	
Output Voltage Logic 0	V <sub>OL</sub>	2	4							9	5,8	1,16	
		3	6							9	5,8	1,16	
		2	4							9	8	1,5,16	
		3	6							9	8	1,5,16	
Threshold Voltage Logic 1	V <sub>OHA</sub>	2 (2.)	4							9	5,8	1,16	
		2	4							9	5,8	1,16	
		2	4							9	5,8	1,16	
		2		4		4				9	5,8	1,16	
		2 (3.)					4			9	8	1,5,16	
2 (4.)							4		9	8	1,5,16		
Threshold Voltage Logic 0	V <sub>OLA</sub>	2 (2.)	4							9	5,8	1,16	
		2	4							9	5,8	1,16	
		2 (2.)	4							9	5,8	1,16	
		2			4					9	5,8	1,16	
		2 (3.)					4			9	8	1,5,16	
2 (4.)							4		9	8	1,5,16		
Switching Times Propagation Delay			+5.0V	+2.40V	Figure					+7.0V	-3.2V	+2.0V	
Data Input	t <sub>7+14+</sub> t <sub>7-14-</sub>	14			Figure 3					9	5,8	1,16	
		14			Figure 3					9	5,8	1,16	
Clock Input	t <sub>11-14+</sub> t <sub>11-14-</sub>	14			Figure 6					9	5,8	1,16	
		14			Figure 6					9	5,8	1,16	
Strobe Input	t <sub>12+14+</sub> t <sub>12-14-</sub>	14	7		Figure 4					9	5,8	1,16	
		14	7		Figure 4					9	5,8	1,16	
Reset Input	t <sub>10+14-</sub>	14	7		Figure 5					9	5,8	1,16	
Hysteresis Mode	t <sub>7+14+</sub> t <sub>7-14-</sub>	14			Figure 3					9	8	1,5,16	
		14			Figure 3					9	8	1,5,16	
Setup Time	t <sub>setup</sub>	14			Figure 7					9	5,8	1,16	
Hold Time	t <sub>hold</sub>	14			Figure 7					9	5,8	1,16	
Rise Time	t <sub>+</sub>	14			Figure 3					9	5,8	1,16	
Fall Time	t <sub>-</sub>	14			Figure 3					9	5,8	1,16	

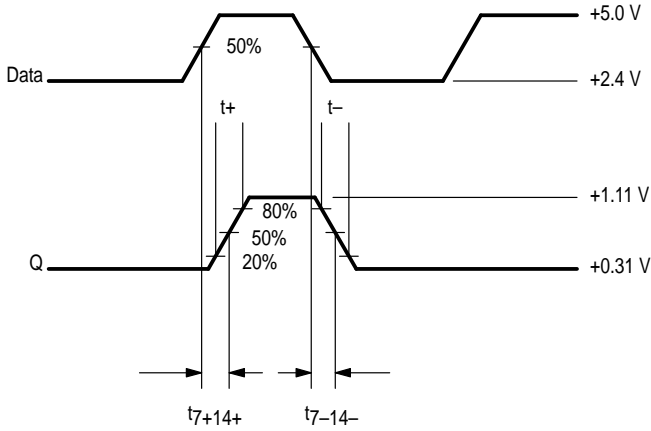
- Pin 5 to V<sub>EE</sub>, V<sub>IL</sub> to Data input one at a time.
- Output latched to logic high state prior to test. V<sub>IHA'</sub>, V<sub>ILA'</sub> are standard logic 1 and logic 0 MTTL threshold voltages. V<sub>IHA''</sub>, V<sub>ILA''</sub>, V<sub>IHA'''</sub> and V<sub>ILA'''</sub> are logic 1 and logic 0 threshold voltages in the hysteresis mode as shown in Figure 1 on page 3-2.
- Input level on data input taken from +0.4V up to voltage level given.
- Input level on data input taken from +4.0V down to voltage level given.
- Operation and limits shown also apply for V<sub>CC</sub> = +6.0V.
- When testing, choose either TTL or IBM input levels.

Figure 2. SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C

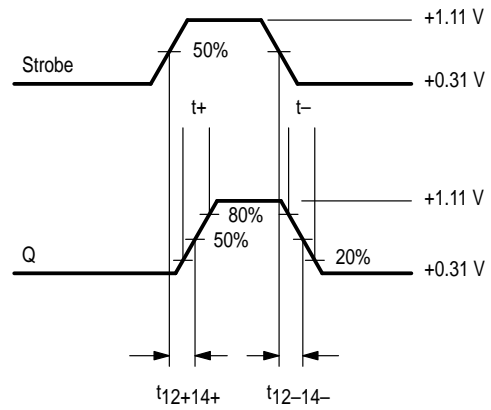


NOTE: All power supplies and logic levels are shifted 2 volts positive.

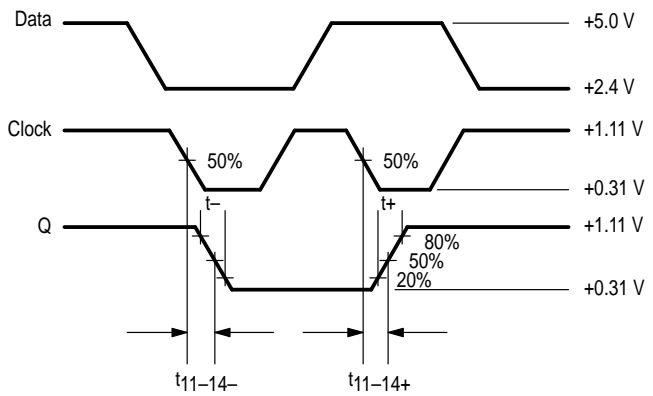
**Figure 3 – DATA to OUTPUT**  
(Clock and Reset are low, Strobe is high)



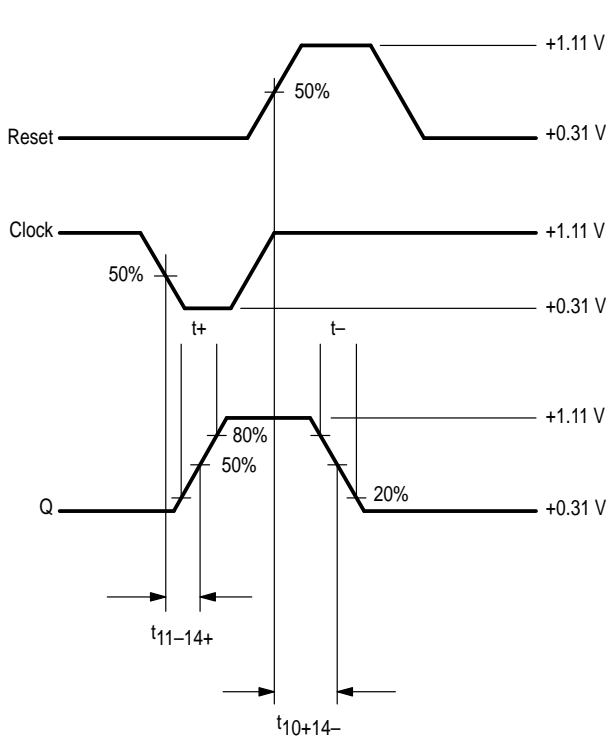
**Figure 4 – STROBE to OUTPUT**  
(Data is high, Clock and Reset are low)



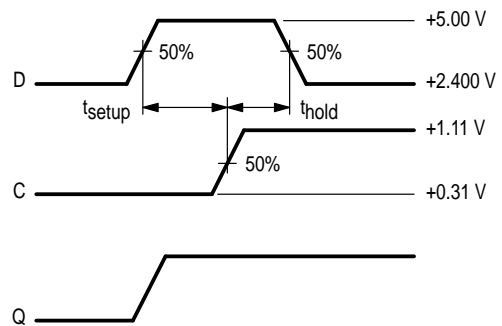
**Figure 6 – CLOCK to OUTPUT**  
(Reset is low, Strobe is high)



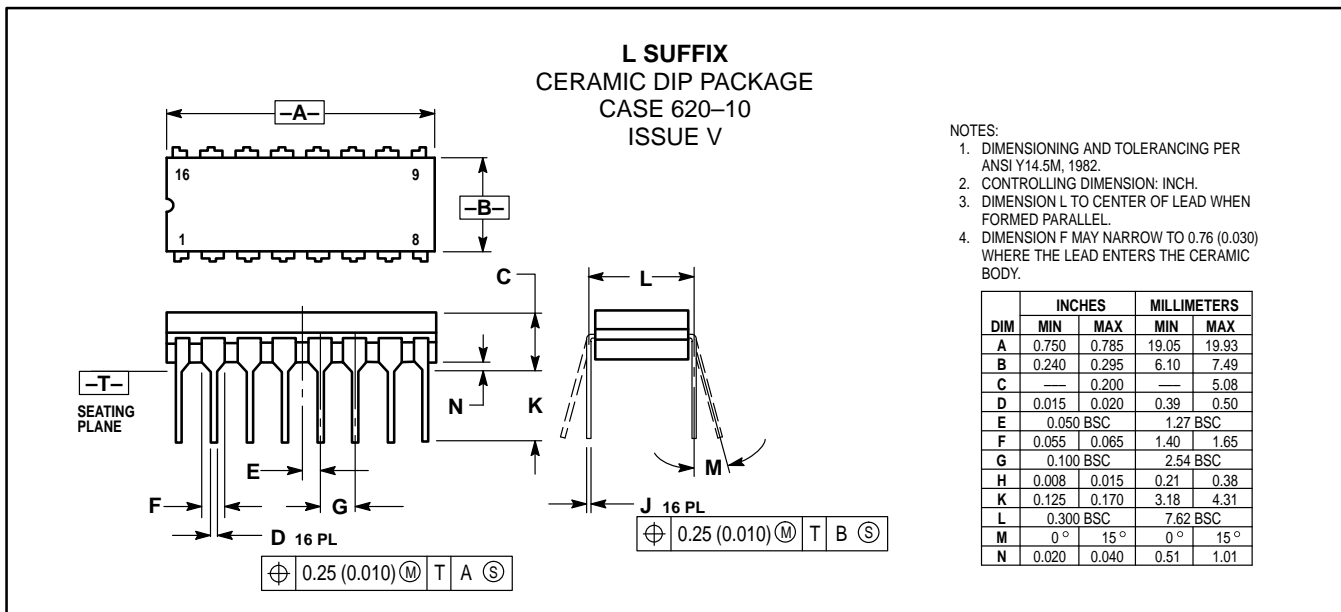
**Figure 5 – RESET to OUTPUT**  
(Data and Strobe are high)



**Figure 7 – TSET UP AND THOLD WAVEFORMS**



OUTLINE DIMENSIONS



Motorola reserves the right to make changes without further notice to any products herein. Motorola makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters which may be provided in Motorola data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part. Motorola and are registered trademarks of Motorola, Inc. Motorola, Inc. is an Equal Opportunity/Affirmative Action Employer.

**How to reach us:**

**USA/EUROPE/Locations Not Listed:** Motorola Literature Distribution; P.O. Box 5405, Denver, Colorado 80217. 303-675-2140 or 1-800-441-2447

**JAPAN:** Nippon Motorola Ltd.; Tatsumi-SPD-JLDC, 6F Seibu-Butsuryu-Center, 3-14-2 Tatsumi Koto-Ku, Tokyo 135, Japan. 81-3-3521-8315

**Mfax™:** RMFAX0@email.sps.mot.com - TOUCHTONE 602-244-6609  
**INTERNET:** http://Design-NET.com

**ASIA/PACIFIC:** Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park, 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298