

# Dual J-K Master-Slave Flip-Flop

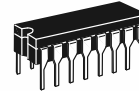
The MC10135 is a dual master-slave dc coupled J-K flip-flop. Asynchronous set (S) and reset (R) are provided. The set and reset inputs override the clock.

A common clock is provided with separate J-K inputs. When the clock is static, the J-K inputs do not effect the output.

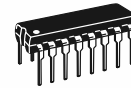
The output states of the flip-flop change on the positive transition of the clock.

$P_D = 280 \text{ mW typ/pkg (No Load)}$   
 $f_{Tog} = 140 \text{ MHz typ}$   
 $t_{pd} = 3.0 \text{ ns typ}$   
 $t_r, t_f = 2.5 \text{ ns typ (20\%--80\%)}$

## MC10135



**L SUFFIX**  
 CERAMIC PACKAGE  
 CASE 620-10

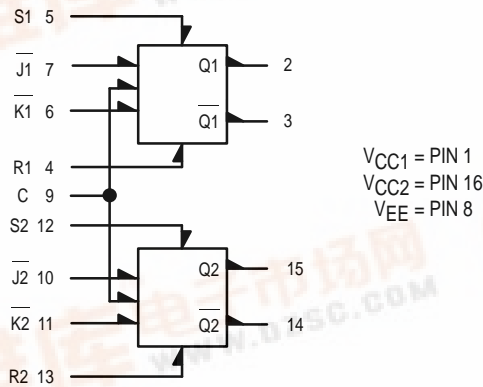


**P SUFFIX**  
 PLASTIC PACKAGE  
 CASE 648-08

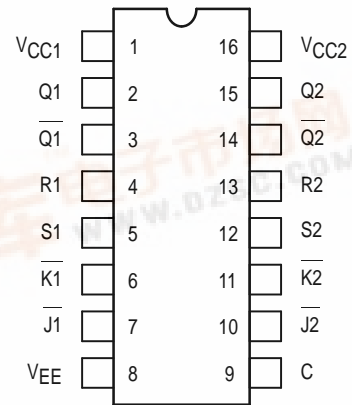


**FN SUFFIX**  
 PLCC  
 CASE 775-02

### LOGIC DIAGRAM



### DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-Line Package. For PLCC pin assignment, see the Pin Conversion Tables on page 6-11 of the Motorola MECL Data Book (DL122/D).

### R-S TRUTH TABLE

R	S	$Q_{n+1}$
L	L	$Q_n$
L	H	H
H	L	L
H	H	N.D.

N.D. = Not Defined

### CLOCK J-K TRUTH TABLE\*

J	K	$Q_{n+1}$
L	L	$Q_n$
H	L	L
L	H	H
H	H	$Q_n$

\*Output states change on positive transition of clock for J-K input condition present.

## ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			-30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	$I_E$	8		75		54	68		75	mAdc
Input Current	$I_{inH}$	6,7,9,10,11 4,5,12,13		425 620			265 390		265 390	$\mu$ Adc
	$I_{inL}$	4,5,6,7,9, 10,11,12,13	0.5 0.5		0.5 0.5			0.3 0.3		$\mu$ Adc
Output Voltage Logic 1	$V_{OH}$	2 2 (3.)	-1.060 -1.060	-0.890 -0.890	-0.960 -0.960		-0.810 -0.810	-0.890 -0.890	-0.700 -0.700	Vdc
Output Voltage Logic 0	$V_{OL}$	3 3 (3.)	-1.890 -1.890	-1.675 -1.675	-1.850 -1.850		-1.650 -1.650	-1.825 -1.825	-1.615 -1.615	Vdc
Threshold Voltage Logic 1	$V_{OHA}$	2 2 (4.)	-1.080 -1.080		-0.980 -0.980			-0.910 -0.910		Vdc
Threshold Voltage Logic 0	$V_{OLA}$	3 3 (4.)		-1.655 -1.655			-1.630 -1.630		-1.595 -1.595	Vdc
Switching Times (50 $\Omega$ Load) Clock Input										ns
Propagation Delay	$t_{g+2+}$ $t_{g+2-}$	2 2	1.8 1.8	5.0 5.0	1.8 1.8	3.0 3.0	4.5 4.5	1.8 1.8	4.6 4.6	
Rise Time (20 to 80%)	$t_{2+}$ , $t_{3+}$	2, 3	1.1	4.8	1.1	2.0	4.5	1.1	4.7	
Fall Time (20 to 80%)	$t_{2-}$ , $t_{3-}$	2, 3	1.1	4.8	1.1	2.0	4.5	1.1	4.7	
Set Input										ns
Propagation Delay	$t_{5+2+}$ $t_{12+15+}$ $t_{5+3-}$ $t_{12+14-}$	2 15 3 14	1.8 1.8 1.8 1.8	5.6 5.6 5.6 5.6	1.8 1.8 1.8 1.8	3.0 3.0 3.0 3.0	5.0 5.0 5.0 5.0	1.8 1.8 1.8 1.8	5.2 5.2 5.2 5.2	
Reset Input										ns
Propagation Delay	$t_{4+2-}$ $t_{4+3-}$ $t_{13+15-}$ $t_{13+14+}$	2 3 15 14	1.8 1.8 1.8 1.8	5.6 5.6 5.6 5.6	1.8 1.8 1.8 1.8	3.0 3.0 3.0 3.0	5.0 5.0 5.0 5.0	1.8 1.8 1.8 1.8	5.2 5.2 5.2 5.2	
Setup Time	$t_{setup}$	7	2.5		2.5	1.0		2.5		ns
Hold Time	$t_{hold}$	7	1.5		1.5	1.0		2.5		ns
Toggle Frequency (Max)	$f_{tog}$	2	125		125	140		125		MHz

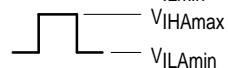
1. Individually test each input; apply  $V_{IHmax}$  to pin under test.

2. Individually test each input; apply  $V_{ILmin}$  to pin under test.

3. Output level to be measured after a clock pulse has been applied to the  $\overline{C_E}$  Input (Pin 6)



4. Output level to be measured after a clock pulse has been applied to the  $\overline{C_E}$  Input (Pin 6)



MC10135

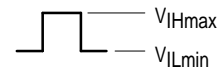
**ELECTRICAL CHARACTERISTICS** (continued)

			TEST VOLTAGE VALUES (Volts)					(V <sub>CC</sub> ) Gnd	
			V <sub>IHmax</sub>	V <sub>ILmin</sub>	V <sub>IHAmin</sub>	V <sub>ILAmax</sub>	V <sub>EE</sub>		
@ Test Temperature									
-30°C			-0.890	-1.890	-1.205	-1.500	-5.2		
+25°C			-0.810	-1.850	-1.105	-1.475	-5.2		
+85°C			-0.700	-1.825	-1.035	-1.440	-5.2		
Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW						
			V <sub>IHmax</sub>	V <sub>ILmin</sub>	V <sub>IHAmin</sub>	V <sub>ILAmax</sub>	V <sub>EE</sub>		
Power Supply Drain Current	I <sub>E</sub>	8					8	1, 16	
Input Current	I <sub>inH</sub>	6,7,9,10,11 4,5,12,13	Note 1. Note 1.				8 8	1, 16 1, 16	
	I <sub>inL</sub>	4,5,6,7,9, 10,11,12,13		Note 2. Note 2.			8 8	1, 16 1, 16	
Output Voltage	Logic 1	V <sub>OH</sub>	2 2 (3.)	5 6			8 8	1, 16 1, 16	
Output Voltage	Logic 0	V <sub>OL</sub>	3 3 (3.)	5 6			8 8	1, 16 1, 16	
Threshold Voltage	Logic 1	V <sub>OHA</sub>	2 2 (4.)	6		5	8 8	1, 16 1, 16	
Threshold Voltage	Logic 0	V <sub>OLA</sub>	3 3 (4.)	6		5	8 8	1, 16 1, 16	
Switching Times (50Ω Load) Clock Input						Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t <sub>g+2+</sub>	2				9	2	8	1, 16
	t <sub>g+2-</sub>	2				9	2	8	1, 16
Rise Time (20 to 80%)	t <sub>2+</sub> , t <sub>3+</sub>	2, 3				9	2, 3	8	1, 16
Fall Time (20 to 80%)	t <sub>2-</sub> , t <sub>3-</sub>	2, 3				9	2, 3	8	1, 16
Set Input	Propagation Delay	t <sub>5+2+</sub>	2			5	2	8	1, 16
		t <sub>12+15+</sub>	15			12	15	8	1, 16
		t <sub>5+3-</sub>	3			5	3	8	1, 16
		t <sub>12+14-</sub>	14			12	14	8	1, 16
Reset Input	Propagation Delay	t <sub>4+2-</sub>	2			4	2	8	1, 16
		t <sub>4+3-</sub>	3			4	3	8	1, 16
		t <sub>13+15-</sub>	15			13	15	8	1, 16
		t <sub>13+14+</sub>	14			13	14	8	1, 16
Setup Time	t <sub>setup</sub>	7			6, 9	2	8	1, 16	
Hold Time	t <sub>hold</sub>	7			6, 9	2	8	1, 16	
Toggle Frequency (Max)	f <sub>tog</sub>	2			9	2	8	1, 16	

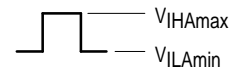
1. Individually test each input; apply V<sub>IHmax</sub> to pin under test.

2. Individually test each input; apply V<sub>ILmin</sub> to pin under test.

3. Output level to be measured after a clock pulse has been applied to the  $\overline{C_E}$  Input (Pin 6)



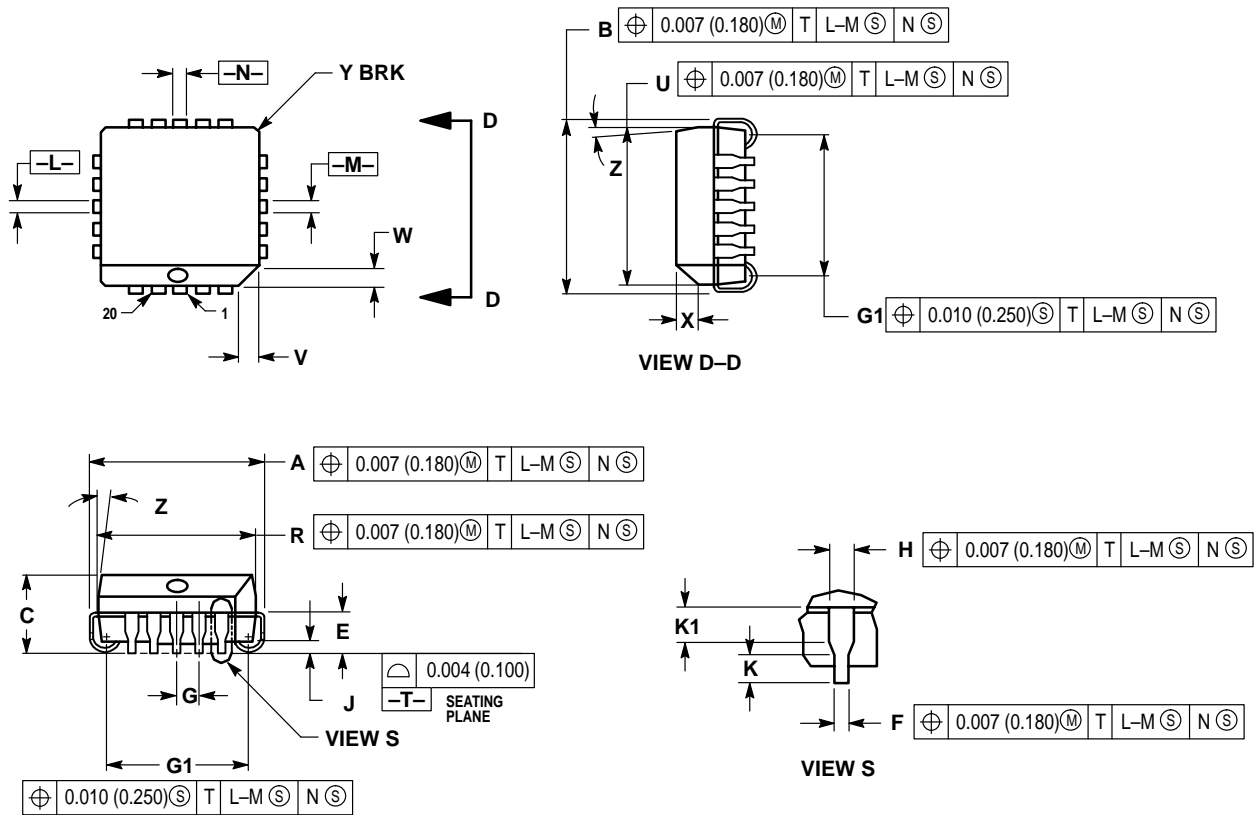
4. Output level to be measured after a clock pulse has been applied to the  $\overline{C_E}$  Input (Pin 6)



Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

OUTLINE DIMENSIONS

FN SUFFIX  
 PLASTIC PLCC PACKAGE  
 CASE 775-02  
 ISSUE C



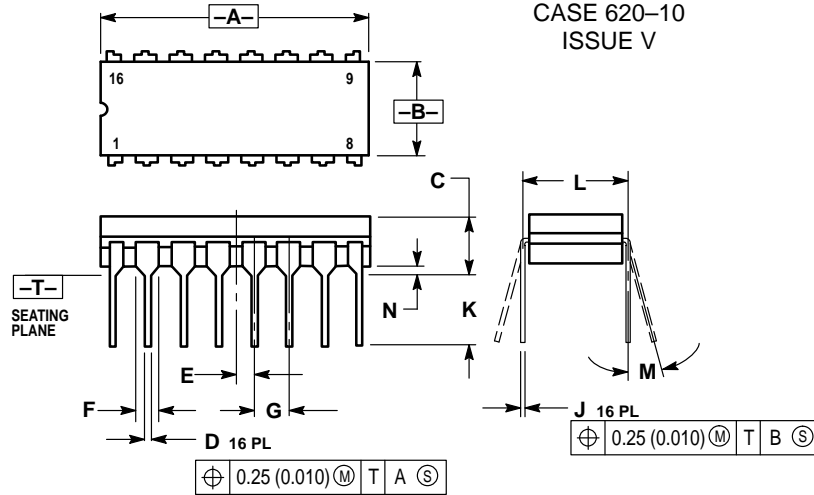
NOTES:

- DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
- DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
- DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.385	0.395	9.78	10.03
B	0.385	0.395	9.78	10.03
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.350	0.356	8.89	9.04
U	0.350	0.356	8.89	9.04
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.310	0.330	7.88	8.38
K1	0.040	—	1.02	—

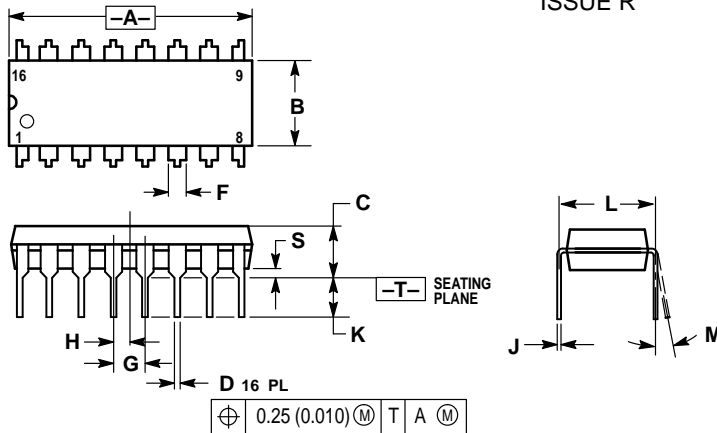
OUTLINE DIMENSIONS

L SUFFIX  
CERAMIC DIP PACKAGE  
CASE 620-10  
ISSUE V



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
  4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

P SUFFIX  
PLASTIC DIP PACKAGE  
CASE 648-08  
ISSUE R



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
  4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
  5. ROUNDED CORNERS OPTIONAL.

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