# Differential PECL to TTL Translator

**MC10ELT21**
**MC100ELT21**

The MC10ELT/100ELT21 is a differential PECL to TTL translator. Because PECL (Positive ECL) levels are used only +5V and ground are required. The small outline 8-lead SOIC package and the single gate of the ELT21 makes it ideal for those applications where space, performance and low power are at a premium. Because the mature MOSAIC 1.5 process is used, low cost can be added to the list of features.

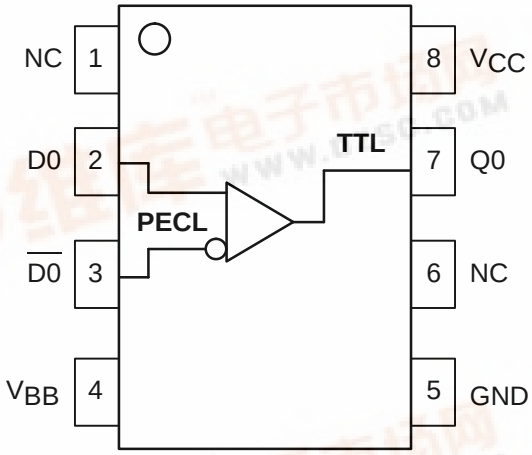
The $V_{BB}$ output allows the ELT21 to also be used in a single-ended input mode. In this mode the $V_{BB}$ output is tied to the IN input for a non-inverting buffer or the IN input for an inverting buffer. If used the $V_{BB}$ pin should be bypassed to ground via a 0.01µF capacitor.

The ELT21 is available in both ECL standards: the 10ELT is compatible with positive MECL 10H logic levels while the 100ELT is compatible with positive ECL 100K logic levels.

- 3.5ns Typical Propagation Delay
- Differential PECL Inputs
- Small Outline SOIC Package
- 24mA TTL Output
- Flow Through Pinouts


**D SUFFIX**
PLASTIC SOIC PACKAGE
CASE 751-05

### LOGIC DIAGRAM AND PINOUT ASSIGNMENT




### PIN DESCRIPTION

| PIN | FUNCTION |
|---|---|
| Q | TTL Output |
| D | Diff PECL Inputs |
| $V_{CC}$ | +5.0V Supply |
| $V_{BB}$ | Reference Output |
| GND | Ground |

**MAXIMUM RATINGS***

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage (Referenced to GND) | 7.0 | V |
| $T_A$ | Operating Temperature Range (In Free-Air) | –40 to 85 | °C |
| $T_{STG}$ | Storage Temperature Range | –55 to +150 | °C |

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

**TTL OUTPUT DC CHARACTERISTICS** ($V_{CC}$ = 4.75V to 5.25V; $T_A$ = –40°C to 85°C)

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | 2.4 | | | V | $I_{OH}$ = –3.0mA |
| $V_{OL}$ | Output LOW Voltage | | | 0.5 | V | $I_{OL}$ = 24mA |
| $I_{CCH}$ | Power Supply Current | | 20 | 29 | mA | |
| $I_{CCL}$ | Power Supply Current | | 22 | 32 | mA | |
| $I_{OS}$ | Output Short Circuit Current | –150 | | –60 | mA | |

**PECL INPUT DC CHARACTERISTICS** ($V_{CC}$ = 4.75V to 5.25V; $T_A$ = –40°C to 85°C)

| | | –40°C | | 0°C | | 25°C | | | 85°C | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Symbol | Characteristic | Min | Max | Min | Max | Min | Typ | Max | Min | Max | Unit | Condition |
| $I_{IH}$ | Input HIGH Current | | 150 | | 150 | | | 150 | | 150 | µA | |
| $I_{IL}$ | Input LOW Current | 0.5 | | 0.5 | | 0.5 | | | 0.5 | | µA | |
| $V_{CMR}$ | Common Mode Range | 2.2 | $V_{CC}$ | 2.2 | $V_{CC}$ | 2.2 | | $V_{CC}$ | 2.2 | $V_{CC}$ | V | |
| $V_{PP}$ | Minimum Peak-to-Peak Input[1] | 200 | | 200 | | 200 | | | 200 | | mV | |
| $V_{IH}$ | Input HIGH Voltage 10ELT<br>100ELT | 3.770<br>3.835 | 4.110<br>4.120 | 3.830<br>3.835 | 4.16<br>4.12 | 3.870<br>3.835 | | 4.19<br>4.12 | 3.930<br>3.835 | 4.265<br>4.120 | V | $V_{CC}$ = 5.0V |
| $V_{IL}$ | Input LOW Voltage 10ELT<br>100ELT | 3.05<br>3.19 | 3.500<br>3.525 | 3.05<br>3.19 | 3.520<br>3.525 | 3.05<br>3.19 | | 3.520<br>3.525 | 3.05<br>3.19 | 3.550<br>3.525 | V | $V_{CC}$ = 5.0V |
| $V_{BB}$ | Reference Output 10ELT<br>100ELT | 3.57<br>3.62 | 3.70<br>3.74 | 3.62<br>3.62 | 3.73<br>3.74 | 3.65<br>3.62 | | 3.75<br>3.74 | 3.69<br>3.62 | 3.81<br>3.75 | V | $V_{CC}$ = 5.0V |

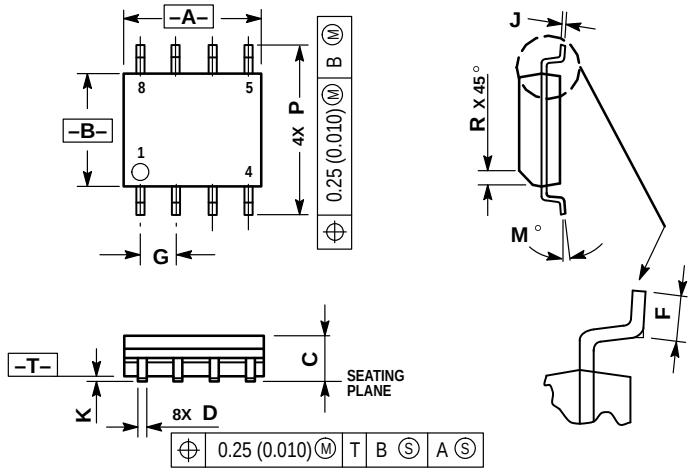
1. 200mV input guarantees full logic swing at the output.

**AC CHARACTERISTICS** ($V_{CC}$ = 4.75V to 5.25V; $T_A$ = –40°C to 85°C)

| | | –40°C | | 0°C | | 25°C | | | 85°C | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Symbol | Characteristic | Min | Max | Min | Max | Min | Typ | Max | Min | Max | Unit | Condition |
| $t_{PLH}$ | Propagation Delay[1] | 2.0 | 5.5 | 2.0 | 5.5 | 2.0 | | 5.5 | 2.0 | 5.5 | ns | $C_L$ = 20pF |
| $t_{PHL}$ | Propagation Delay[1] | 2.0 | 5.5 | 2.0 | 5.5 | 2.0 | | 5.5 | 2.0 | 5.5 | ns | $C_L$ = 20pF |

## OUTLINE DIMENSIONS

**D SUFFIX**
PLASTIC SOIC PACKAGE
CASE 751–05
ISSUE P




NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. DIMENSIONS ARE IN MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
6. DIMENSION D DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 4.80 | 5.00 |
| B | 3.80 | 4.00 |
| C | 1.35 | 1.75 |
| D | 0.35 | 0.49 |
| F | 0.40 | 1.25 |
| G | 1.27 BSC | |
| J | 0.18 | 0.25 |
| K | 0.10 | 0.25 |
| M | 0 ° | 7 ° |
| P | 5.80 | 6.20 |
| R | 0.25 | 0.50 |



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