

2-Bit by 2-Bit Parallel Binary Multiplier

The MC14554B 2 x 2-bit parallel binary multiplier is constructed with complementary MOS (CMOS) enhancement mode devices. The multiplier can perform the multiplication of two binary numbers and simultaneously add two other binary numbers to the product. The MC14554B has two multiplicand inputs (X0 and X1), two multiplier inputs (Y0 and Y1), five cascading or adding inputs (K0, K1, M0, M1, and M2), and five sum and carry outputs (S0, S1, S2, C1 [S3], and C0). The basic multiplier can be expanded into a straightforward m-bit by n-bit parallel multiplier without additional logic elements.

Application areas include arithmetic processing (multiplying/adding, obtaining square roots, polynomial evaluation, obtaining reciprocals, and dividing), Fast Fourier Transform processing, digital filtering, communications (convolution and correlation), and process and machine controls.

- Diode Protection on All Inputs
- All Outputs Buffered
- Straight-forward m-Bit By n-Bit Expansion
- No Additional Logic Elements Needed for Expansion
- Multiplies and Adds Simultaneously
- Positive Logic Design
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	− 0.5 to + 18.0	V
V _{in} , V _{out}	Input or Output Voltage (DC or Transient)	− 0.5 to V _{DD} + 0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P _D	Power Dissipation, per Package†	500	mW
T _{stg}	Storage Temperature	− 65 to + 150	°C
T _L	Lead Temperature (8-Second Soldering)	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

† Temperature Derating:

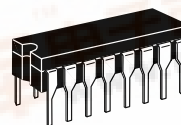
Plastic "P and D/DW" Packages: − 7.0 mW/°C From 65°C To 125°C

Ceramic "L" Packages: − 12 mW/°C From 100°C To 125°C

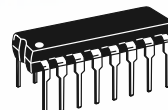
PIN ASSIGNMENT

Y1	1	16	V _{DD}
M0	2	15	Y0
M1	3	14	X0
C0	4	13	X1
M2	5	12	K0
C1 (S3)	6	11	S0
S2	7	10	K1
V _{SS}	8	9	S1

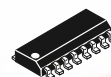
MC14554B



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



D SUFFIX
SOIC
CASE 751B

ORDERING INFORMATION

MC14XXXBCP	Plastic
MC14XXXBCL	Ceramic
MC14XXXBD	SOIC

T_A = − 55° to 125°C for all packages.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

EQUATIONS

$$S = (X \times Y) + K + M$$

Where:

x Means Arithmetic Times.

+ Means Arithmetic Plus.

$$S = S3 \ S2 \ S1 \ S0, X = X1X0, Y = Y1Y0,$$

$$K = K1 \ K0, M = M1 \ M0 \text{ (Binary Numbers).}$$

Example:

$$\text{Given: } X = 2(1), Y = 3(11)$$

$$K = 1(01), M = 2(10)$$

$$\text{Then: } S = (2 \times 3) + 1 + 2 = 9$$

$$S = (10 \times 11) + 01 + 10 = 1001$$

NOTE: C0 connected to M2 for this size multiplier. See general expansion diagram for other size multipliers.



ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

[illegible]

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_I) = I_T(50 \text{ pF}) + (C_I - 50) \text{ Vfk}$$

where: I_T is in μA (per package), C_I in pF, $V = (V_{DD} - V_{SS})$ in volts, f in kHz is input frequency, and $k = 0.0035$.

SWITCHING CHARACTERISTICS* ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	V_{DD}	Min	Typ #	Max	Unit
Output Rise and Fall Time $t_{TLH}, t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}, t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}, t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	t_{TLH} , t_{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time K0 to C0 $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 185 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 82 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 60 \text{ ns}$ M0 to S2 $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 595 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 247 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 185 \text{ ns}$	t_{PLH} , t_{PHL}	5.0 10 15	— — —	270 115 85	675 290 215	ns
		5.0 10 15	— — —	680 280 210	1700 750 570	

* The formulas given are for the typical characteristics only at 25°C .

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

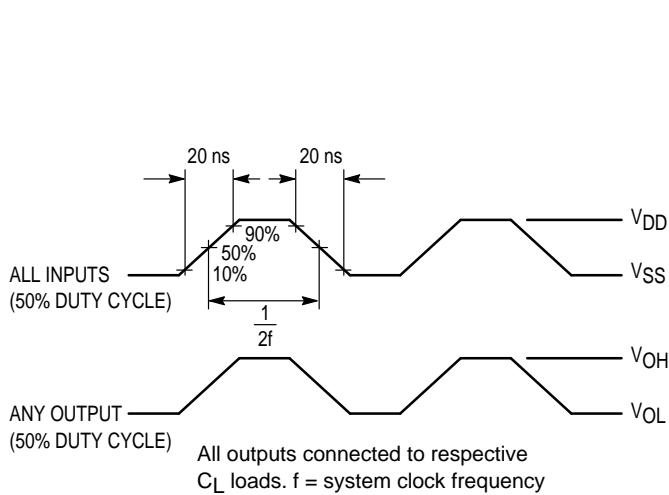
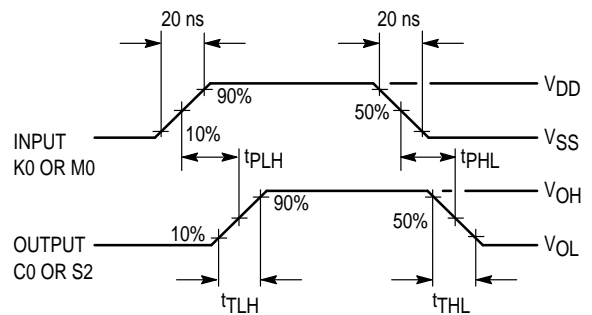


Figure 1. Dynamic Power Dissipation Waveforms



For K0 to C0:

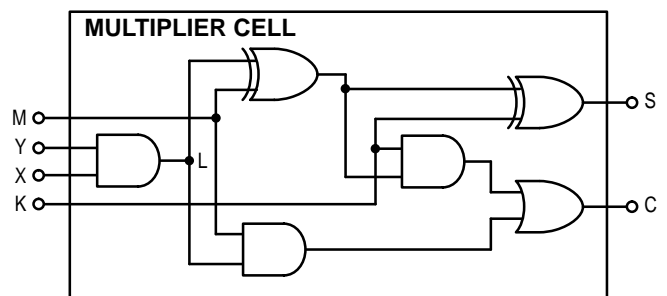
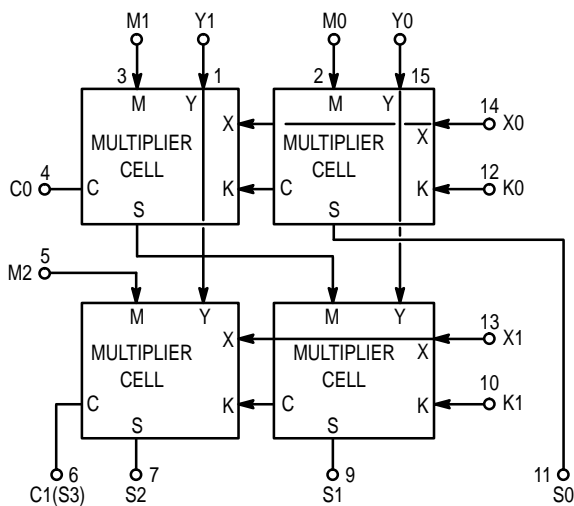
Inputs X0, X1, Y0, Y1, K1, and M2 low, and inputs M0 and M1 high.

For M0 to S2:

Inputs X1, Y1, and K0 low, and inputs X0, Y0, K1, M1, and M2 high.

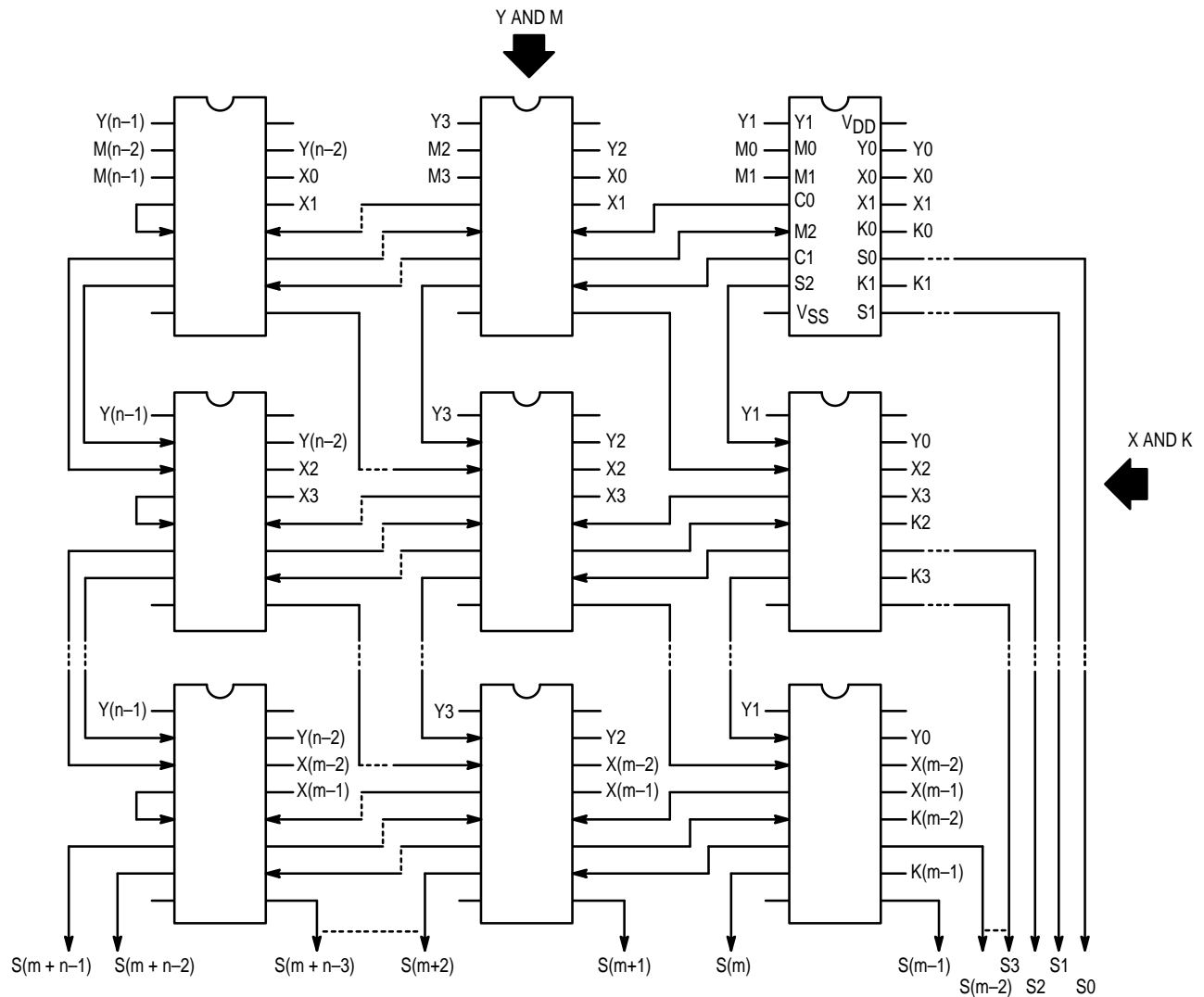
Figure 2. Dynamic Signal Waveforms

LOGIC DIAGRAM



EXPANSION DIAGRAM

m-Bit by n-Bit Parallel Binary Multiplier (Top View)



$S = (X \times Y) + K + M$ Where: \times means Arithmetic Times.
 $+$ means Arithmetic Plus.

$S = S(m+n-1) S(m+n-2) \dots S2 S1 S0$

$X = X(m-1) X(m-2) \dots X2 X1 X0, Y = Y(n-1) Y(n-2) \dots Y2 Y1 Y0$

$K = K(m-1) K(m-2) \dots K2 K1 K0$ and $M = M(n-1) M(n-2) \dots M2 M1 M0$

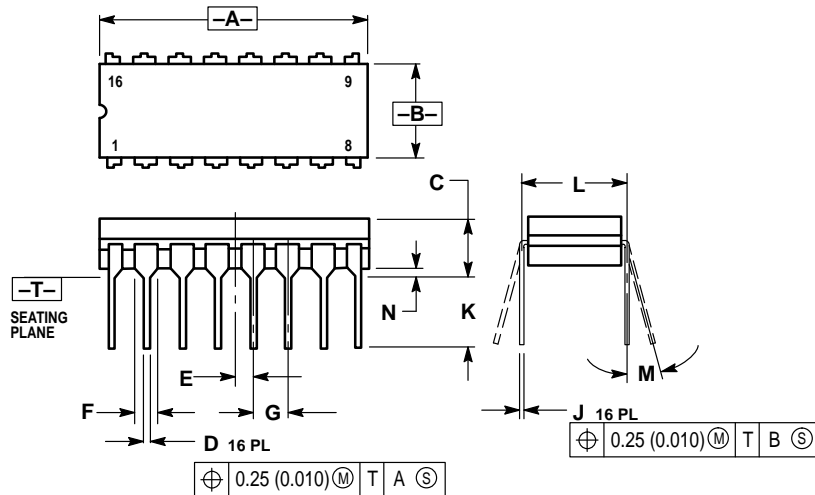
(Binary Numbers).

Number of output binary digits = $m + n$

Number of packages = $mxn/4$ (For m or n of both odd select next highest even number.)

OUTLINE DIMENSIONS

L SUFFIX CERAMIC DIP PACKAGE CASE 620-10 ISSUE V

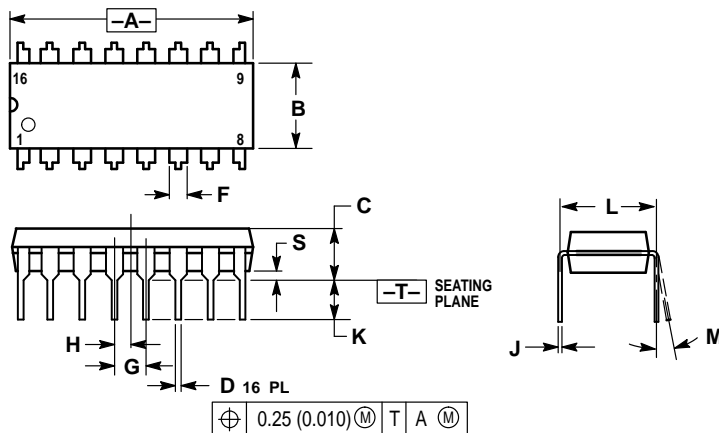


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.076 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC	—	1.27 BSC	—
F	0.055	0.065	1.40	1.65
G	0.100 BSC	—	2.54 BSC	—
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC	—	7.62 BSC	—
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

P SUFFIX PLASTIC DIP PACKAGE CASE 648-08 ISSUE R



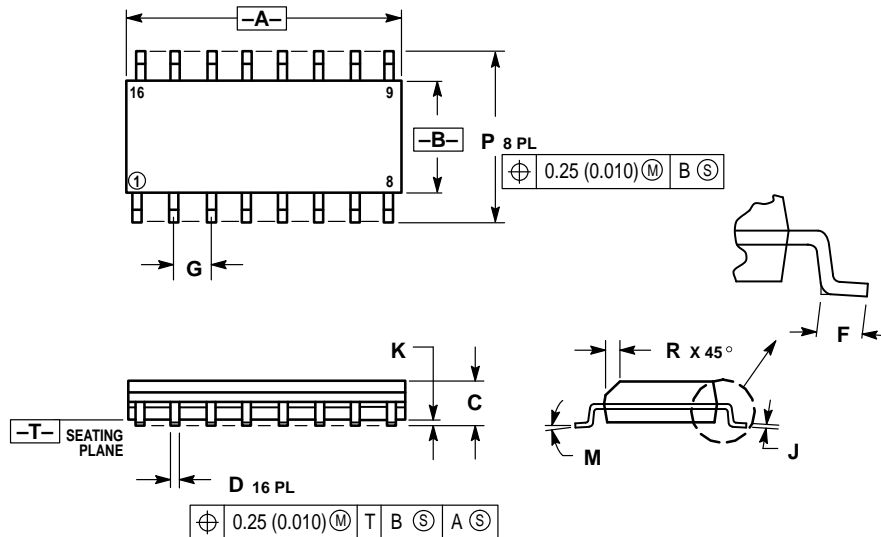
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC	—	2.54 BSC	—
H	0.050 BSC	—	1.27 BSC	—
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

OUTLINE DIMENSIONS


D SUFFIX PLASTIC SOIC PACKAGE CASE 751B-05 ISSUE J



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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