Preferred Device

# **Sensitive Gate Silicon Controlled Rectifiers**

## **Reverse Blocking Thyristors**

Designed for high volume, low cost, industrial and consumer applications such as motor control; process control; temperature, light and speed control.

- Small Size
- Passivated Die for Reliability and Uniformity
- Low Level Triggering and Holding Characteristics
- Available in Two Package Styles
   Surface Mount Lead Form Case 369A
   Miniature Plastic Package Straight Leads Case 369
- Device Marking: Logo, Device Type, e.g., CR8DSM, Date Code

#### MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Repetitive Off–State Voltage <sup>(1)</sup> (T <sub>J</sub> = -40 to 110°C, Sine Wave, 50 to 60 Hz, Gate Open)	V <sub>DRM</sub> , V <sub>RRM</sub>		Volts
MCR8DSM MCR8DSN		600 800	
On–State RMS Current (180° Conduction Angles; T <sub>C</sub> = 90°C)	IT(RMS)	8.0	Amps
Average On–State Current (180° Conduction Angles; T <sub>C</sub> = 90°C)	I <sub>T(AV)</sub>	5.1	Amps
Peak Non-Repetitive Surge Current (1/2 Cycle, Sine Wave, 60 Hz, T <sub>J</sub> = 110°C)	ITSM	90	Amps
Circuit Fusing Consideration (t = 8.3 msec)	l <sup>2</sup> t	34	A <sup>2</sup> sec
Forward Peak Gate Power (Pulse Width ≤ 10 μsec, T <sub>C</sub> = 90°C)	PGM	5.0	Watts
Forward Average Gate Power (t = 8.3 msec, T <sub>C</sub> = 90°C)	P <sub>G</sub> (AV)	0.5	Watt
Forward Peak Gate Current (Pulse Width ≤ 10 μsec, T <sub>C</sub> = 90°C)	I <sub>GM</sub>	2.0	Amps
Operating Junction Temperature Range	TJ	-40 to 110	°C
Storage Temperature Range	T <sub>stg</sub>	-40 to 150	°C

<sup>(1)</sup> VDRM and VRRM for all types can be applied on a continuous basis. Ratings apply for negative gate voltage; positive gate voltage shall not be applied concurrent with negative potential on the anode. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the device are exceeded.



#### ON Semiconductor

http://onsemi.com

#### SCRs 8 AMPERES RMS 600 thru 800 VOLTS





#### D-PAK CASE 369A STYLE 4

PIN ASSIGNMENT			
1 Cathode			
2	Anode		
3	Gate		
4	Anode		

#### ORDERING INFORMATION

		and the second second
Device	Package	Shipping
MCR8DSMT4	DPAK 369A	16mm Tape and Reel (2.5K/Reel)
MCR8DSNT4	DPAK 369A	16mm Tape and Reel (2.5K/Reel)

**Preferred** devices are recommended choices for future use and best overall value.



#### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient <sup>(1)</sup>	R <sub>θ</sub> JC R <sub>θ</sub> JA R <sub>θ</sub> JA	2.2 88 80	°C/W
Maximum Lead Temperature for Soldering Purposes 1/8" from Case for 10 Seconds	TL	260	°C

#### **ELECTRICAL CHARACTERISTICS** (T<sub>J</sub> = 25°C unless otherwise noted)

Characteristics	Symbol	Min	Тур	Max	Unit		
OFF CHARACTERISTICS							
Peak Repetitive Forward or Reverse Blocking Current (VAK = Rated VDRM or VRRM; RGK = 1.0 K $\Omega$ )(2)	T <sub>J</sub> = 25°C T <sub>J</sub> = 110°C	I <sub>DRM</sub> I <sub>RRM</sub>		_	10 500	μΑ	
ON CHARACTERISTICS						•	
Peak Reverse Gate Blocking Voltage (I <sub>GR</sub> = 10 μA)		VGRM	10	12.5	18	Volts	
Peak Reverse Gate Blocking Current (VGR = 10 V)		IRGM		_	1.2	μΑ	
Peak Forward On–State Voltage(3) (I <sub>TM</sub> = 16 A)		V <sub>TM</sub>	_	1.4	1.8	Volts	
Gate Trigger Current (Continuous dc) <sup>(4)</sup> $(V_D = 12 \text{ V}, R_L = 100 \Omega)$	T <sub>J</sub> = 25°C T <sub>J</sub> = -40°C	l <sub>GT</sub>	5.0 —	12 —	200 300	μΑ	
Gate Trigger Voltage (Continuous dc) <sup>(4)</sup> $(V_D = 12 \text{ V}, \text{ R}_L = 100 \Omega)$	T <sub>J</sub> = 25°C T <sub>J</sub> = -40°C T <sub>J</sub> = 110°C	VGT	0.45 — 0.2	0.65 — —	1.0 1.5 —	Volts	
Holding Current (V <sub>D</sub> = 12 V, Initiating Current = 200 mA, Gate Open)	T <sub>J</sub> = 25°C T <sub>J</sub> = -40°C	lн	0.5 —	1.0	6.0 10	mA	
Latching Current (V <sub>D</sub> = 12 V, I <sub>G</sub> = 2.0 mA)	T <sub>J</sub> = 25°C T <sub>J</sub> = -40°C	ΙL	0.5 —	1.0 —	6.0 10	mA	
Total Turn–On Time (Source Voltage = 12 V, R <sub>S</sub> = 6.0 K $\Omega$ , I <sub>T</sub> = 16 A(pk), R <sub>O</sub> (V <sub>D</sub> = Rated V <sub>DRM</sub> , Rise Time = 20 ns, Pulse Width =		tgt	_	2.0	5.0	μS	

#### **DYNAMIC CHARACTERISTICS**

Characteristics	Symbol	Min	Тур	Max	Unit
Critical Rate of Rise of Off–State Voltage ( $V_D = 0.67 \text{ X}$ Rated $V_{DRM}$ , Exponential Waveform, $R_{GK} = 1.0 \text{ K}\Omega$ , $T_J = 110^{\circ}\text{C}$ )	dv/dt	2.0	10	_	V/μs

<sup>(1)</sup> Surface mounted on minimum recommended pad size.

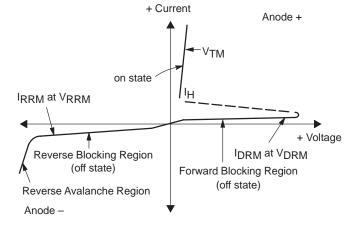
<sup>(2)</sup> Ratings apply for negative gate voltage or R<sub>GK</sub> = 1.0 KΩ. Devices shall not have a positive gate voltage concurrently with a negative voltage on the anode. Devices should not be tested with a constant current source for forward and reverse blocking capability such that the voltage applied exceeds the rated blocking voltage.

<sup>(3)</sup> Pulse Test; Pulse Width  $\leq$  2.0 msec, Duty Cycle  $\leq$  2%.

<sup>(4)</sup> RGK current not included in measurements.

#### **Voltage Current Characteristic of SCR**

Symbol	Parameter
VDRM	Peak Repetitive Off State Forward Voltage
I <sub>DRM</sub>	Peak Forward Blocking Current
VRRM	Peak Repetitive Off State Reverse Voltage
IRRM	Peak Reverse Blocking Current
V <sub>TM</sub>	Peak On State Voltage
lΗ	Holding Current



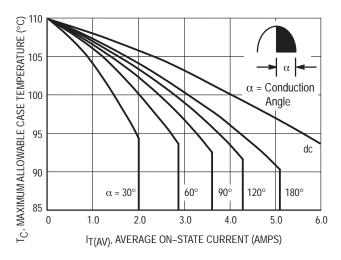


Figure 1. Average Current Derating

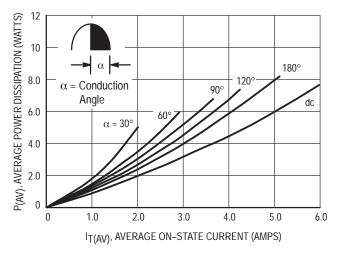


Figure 2. On-State Power Dissipation

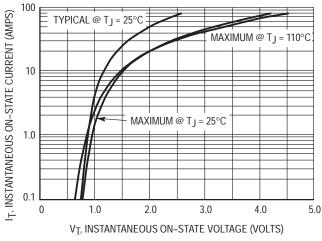


Figure 3. On-State Characteristics

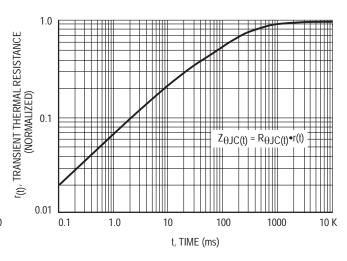


Figure 4. Transient Thermal Response

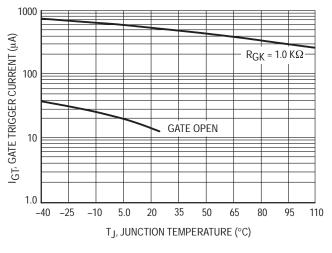


Figure 5. Typical Gate Trigger Current versus Junction Temperature

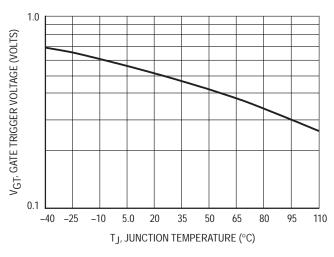


Figure 6. Typical Gate Trigger Voltage versus
Junction Temperature

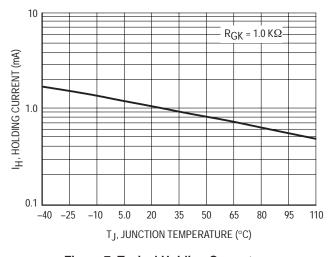


Figure 7. Typical Holding Current versus Junction Temperature

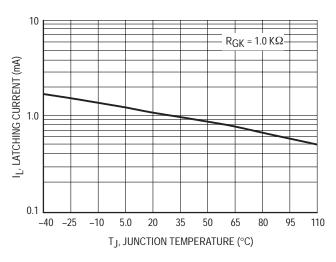


Figure 8. Typical Latching Current versus Junction Temperature

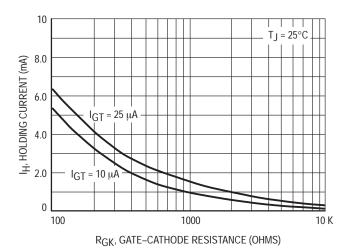
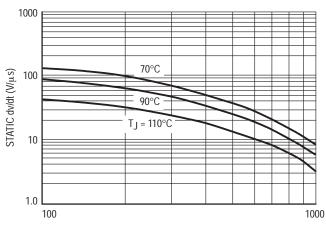


Figure 9. Holding Current versus Gate-Cathode Resistance



R<sub>GK</sub>, GATE-CATHODE RESISTANCE (OHMS)

Figure 10. Exponential Static dv/dt versus Gate—Cathode Resistance and Junction Temperature

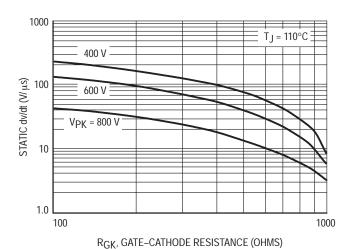
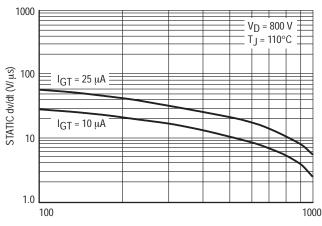


Figure 11. Exponential Static dv/dt versus Gate-Cathode Resistance and Peak Voltage



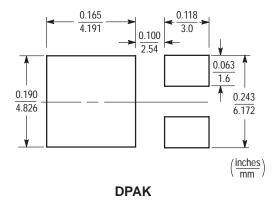
RGK, GATE-CATHODE RESISTANCE (OHMS)

Figure 12. Exponential Static dv/dt versus Gate-Cathode Resistance and Gate Trigger Current Sensitivity

#### MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

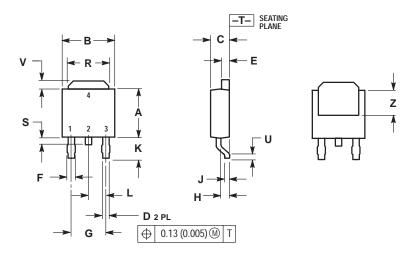
Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection

interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



#### **PACKAGE DIMENSIONS**

#### D-PAK CASE 369A-13 ISSUE Z



- NOTES:
  1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.

	INC	HES	MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
Α	0.235	0.250	5.97	6.35
В	0.250	0.265	6.35	6.73
С	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
Ε	0.033	0.040	0.84	1.01
F	0.037	0.047	0.94	1.19
G	0.180 BSC		4.58	BSC
Н	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29	BSC
R	0.175	0.215	4.45	5.46
S	0.020	0.050	0.51	1.27
U	0.020		0.51	
٧	0.030	0.050	0.77	1.27
Z	0.138		3.51	

STYLE 4: PIN 1. CATHODE 2. ANODE 3. GATE 4. ANODE

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