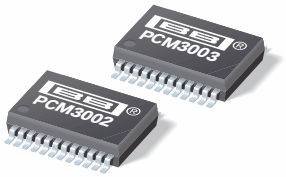
BURR-BROWN®



PCM3002
PCM3003

16-/20-Bit Single-Ended Analog Input/Output SoundPLUS™ STEREO AUDIO CODECs

FEATURES

- MONOLITHIC 20-BIT ΔΣ ADC AND DAC
- 16-/20-BIT INPUT/OUTPUT DATA
- SOFTWARE CONTROL: PCM3002
- HARDWARE CONTROL: PCM3003
- STEREO ADC:
  - Single-Ended Voltage Input
  - 64X Oversampling
  - High Performance
    - THD+N: –86dB
    - SNR: 90dB
    - Dynamic Range: 90dB
- STEREO DAC:
  - Single-Ended Voltage Output
  - Analog Low Pass Filter
  - 8X Oversampling Digital Filter
  - High Performance
    - THD+N: –86dB
    - SNR: 94dB
    - Dynamic Range: 94dB
- SPECIAL FEATURES
  - Digital De-emphasis
  - Digital Attenuation (256 Steps)
  - Soft Mute
  - Digital Loop Back
  - Power Down: ADC/DAC Independent
- SAMPLING RATE: Up to 48kHz
- SYSTEM CLOCK: $256f_S$, $384f_S$, $512f_S$
- SINGLE +3V POWER SUPPLY
- SMALL PACKAGE: 24-Lead SSOP

DESCRIPTION

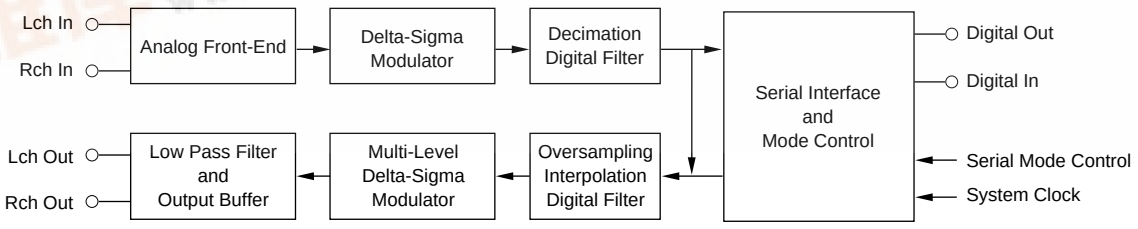
The PCM3002 and PCM3003 are low cost single chip stereo audio CODECs (analog-to-digital and digital-to-analog converters) with single-ended analog voltage input and output.

The ADCs and DACs employ delta-sigma modulation with 64X oversampling. The ADCs include a digital decimation filter, and the DACs include an 8X oversampling digital interpolation filter. The DACs also include digital attenuation, de-emphasis, infinite zero detection and soft mute to form a complete subsystem. PCM3002 and PCM3003 operate with left-justified, right-justified, or I^2S data formats.

PCM3002 and PCM3003 provide a power-down mode that operates on the ADCs and DACs independently.

Fabricated on a highly advanced 0.6µs CMOS process, PCM3002 and PCM3003 are suitable for a wide variety of cost-sensitive consumer applications where good performance is required.

PCM3002's multi-functions are controlled by software and the PCM3003's functions include de-emphasis, power down, and audio data format selections, which are controlled by hardware.



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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

All specifications at +25°C, V_{DD} = V_{CC} = 3.0V, f_S = 44.1kHz, SYSCLK = 384f_S, and 16-bit data, unless otherwise noted.

PARAMETER	CONDITIONS	PCM3002E/3003E MIN	PCM3002E/3003E TYP	PCM3002E/3003E MAX	UNITS
DIGITAL INPUT/OUTPUT					
Input Logic					
Input Logic Level: V_{IH}[1, 2, 3]		0.7 x V_{DD}			VDC
V_{IL}[1, 2, 3]				0.3 x V_{DD}	VDC
Input Logic Current: I_{IN}[2]				±1	µA
Input Logic Current: I_{IN}[1]				100	µA
Output Logic					
Output Logic Level: V_{OH}[5]	I_{OUT} = –1mA	V_{DD} –0.3			VDC
V_{OL}[5]	I_{OUT} = +1mA			0.3	VDC
Output Logic Level: V_{OL}[4]	I_{OUT} = +1mA			0.3	VDC
CLOCK FREQUENCY					
Sampling Frequency (f_S)		32	44.1	48	kHz
System Clock Frequency	256f_S	8.1920	11.2896	12.2880	MHz
	384f_S	12.2880	16.9344	18.4320	MHz
	512f_S	16.3840	22.5792	24.5760	MHz
ADC CHARACTERISTICS					
RESOLUTION			20		Bits
DC ACCURACY					
Gain Mismatch Channel-to-Channel			±1.0	±3.0	% of FSR
Gain Error			±2.0	±5.0	% of FSR
Gain Drift			±20		ppm of FSR/°C
Bipolar Zero Error	High-Pass Filter Disabled[6]		±1.7		% of FSR
Bipolar Zero Drift	High-Pass Filter Disabled[6]		±20		ppm of FSR/°C
DYNAMIC PERFORMANCE[7]					
THD+N: V_{IN} = –0.5dB			–86	–80	dB
V_{IN} = –60dB			–28		dB
Dynamic Range	A-Weighted	86	90		dB
Signal-to-Noise Ratio	A-Weighted	86	90		dB
Channel Separation		84	88		dB
DIGITAL FILTER PERFORMANCE					
Passband				0.454f_S	Hz
Stopband		0.583f_S			Hz
Passband Ripple				±0.05	dB
Stopband Attenuation		–65			dB
Delay Time			17.4/f_S		sec
HPF Frequency Response	–3dB		0.019f_S		mHz
ANALOG INPUT					
Voltage Range			0.60 V_{CC}		Vp-p
Center Voltage			0.50 V_{CC}		V
Input Impedance			30		kΩ
Anti-Aliasing Filter Frequency Response	–3dB		150		kHz

SPECIFICATIONS

All specifications at +25°C, V_{DD} = V_{CC} = 3.0V, f_S = 44.1kHz, SYSCLK = 384f_S, CLKIO Input, 18-bit data, unless otherwise noted.

PARAMETER	CONDITIONS	PCM3002E/3003E MIN	PCM3002E/3003E TYP	PCM3002E/3003E MAX	UNITS
DAC CHARACTERISTICS					
RESOLUTION			20		Bits
DC ACCURACY					
Gain Mismatch Channel-to-Channel			±1.0	±3	% of FSR
Gain Error			±1.0	±5	% of FSR
Gain Drift			±20		ppm of FSR/°C
Bipolar Zero Error			±1.0		% of FSR
Bipolar Zero Drift			±20		ppm of FSR/°C
DYNAMIC PERFORMANCE(8)					
THD+N: V_{OUT} = 0dB (Full Scale)			–86	–80	dB
V_{OUT} = –60dB			–28		dB
Dynamic Range	EIAJ, A-Weighted	88	94		dB
Signal-to-Noise Ratio	EIAJ, A-Weighted	88	94		dB
Channel Separation		86	91		dB
DIGITAL FILTER PERFORMANCE					
Passband				0.445f_S	Hz
Stopband		0.555f_S			Hz
Passband Ripple				±0.17	dB
Stopband Attenuation		–35			dB
Delay Time			11.1/f_S		sec
ANALOG OUTPUT					
Voltage Range			0.60 x V_{CC}		Vp-p
Center Voltage			0.5 x V_{CC}		VDC
Load Impedance	AC-Coupling	10			kΩ
LPF Frequency Response	f = 20kHz		–0.16		dB
POWER SUPPLY REQUIREMENTS					
Voltage Range: V_{CC}, V_{DD}	–25°C to +85°C	2.7	3.0	3.6	VDC
	0° C to +70°C(9)	2.4	3.0	3.6	VDC
Supply Current: Operation	V_{CC} = V_{DD} = 3.0V		18	24	mA
Power-Down	V_{CC} = V_{DD} = 3.0V		50		µA
Power Dissipation: Operation	V_{CC} = V_{DD} = 3.0V		54	72	mW
Power-Down(10)	V_{CC} = V_{DD} = 3.0V		150		µW
TEMPERATURE RANGE					
Operation		–25		+85	°C
Storage		–55		+125	°C
Thermal Resistance, Θ_{JA}			100		°C/W

NOTES: (1) Pins 7, 8, 17 and 18: $\overline{RST}$, ML, MD, MC for the PCM3002; $\overline{PDAD}$, $\overline{PDDA}$, DEM1, DEM0 for PCM3003 (Schmitt-Trigger input with 100kΩ typical internal pull-down resistor). (2) Pins 9, 10, 11, 15: SYSCLK, LRCIN, BCKIN, DIN (Schmitt Trigger input). (3) Pin16: 20BIT for PCM3003 (Schmitt-Trigger input, 100kΩ typical internal pull-down resistor). (4) Pin 12: DOUT. (5) Pin 16: $\overline{ZFLG}$ (open drain output). (6) High Pass Filter for Offset Cancel. (7) f_{IN} = 1kHz, using Audio Precision System II, rms mode with 20kHz LPF, 400Hz HPF used for performance calculation. (8) f_{OUT} = 1kHz, using Audio Precision System II, rms mode with 20kHz LPF, 400Hz HPF used for performance calculation. (9) Applies for voltages between 2.4V to 2.7V for 0°C to +70°C and 256f_S/512f_S operation (384f_S not available). (10) SYSCLK, BCKIN, and LRCIN are stopped.

PACKAGE INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)
PCM3002E/3003E	24-Lead SSOP	338

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
+V_{DD}, +V_{CC}1, +V_{CC}2 ..... +6.5V
Supply Voltage Differences ..... ±0.1V
GND Voltage Differences ..... ±0.1V
Digital Input Voltage ..... –0.3 to V_{DD} + 0.3V
Analog Input Voltage ..... –0.3 to V_{CC}1, V_{CC}2 + 0.3V
Power Dissipation 300mW
Input Current ..... ±10mA
Operating Temperature Range ..... –25°C to +85°C
Storage Temperature ..... –55°C to +125°C
Lead Temperature (soldering, 5s) ..... +260°C
(reflow, 10s) ..... +235°C

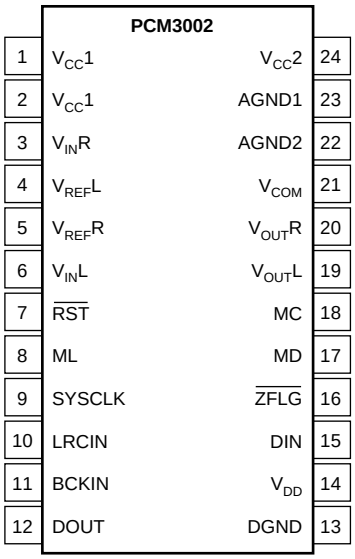
ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

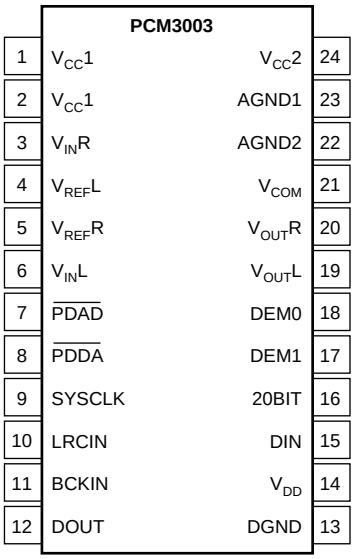
PIN CONFIGURATION—PCM3002

Top View **SSOP**



PIN CONFIGURATION—PCM3003

Top View **SSOP**



PIN ASSIGNMENTS—PCM3002

PIN	NAME	I/O	DESCRIPTION
1	$V_{CC}1$	—	ADC Analog Power Supply
2	$V_{CC}1$	—	ADC Analog Power Supply
3	$V_{IN}R$	IN	ADC Analog Input, Rch
4	$V_{REF}L$	—	ADC Reference, Lch
5	$V_{REF}R$	—	ADC Reference, Rch
6	$V_{IN}L$	IN	ADC Analog Input, Lch
7	$\overline{RST}$	IN	Reset, Active LOW(1, 2)
8	ML	IN	Strobe Pulse for Mode Control(1, 2)
9	SYSCLK	IN	System Clock Input(2)
10	LRCIN	IN	Sample Rate Clock Input (f_S)(2)
11	BCKIN	IN	Bit Clock Input(2)
12	DOUT	OUT	Data Output
13	DGND	—	Digital Ground
14	V_{DD}	—	Digital Power Supply
15	DIN	IN	Data Input(2)
16	$\overline{ZFLG}$	OUT	Zero Flag Output, Active LOW(3)
17	MD	IN	Serial Data for Mode Control(1, 2)
18	MC	IN	Bit Clock for Mode Control(1, 2)
19	$V_{OUT}L$	OUT	DAC Analog Output, Lch
20	$V_{OUT}R$	OUT	DAC Analog Output, Rch
21	V_{COM}	—	ADC/DAC Common
22	AGND2	—	DAC Analog Ground
23	AGND1	—	ADC Analog Ground
24	$V_{CC}2$	—	DAC Analog Power Supply

NOTES: (1) With 100kΩ typical internal pull-down resistor. (2) Schmitt-Trigger input. (3) Open drain output.

PIN ASSIGNMENTS—PCM3003

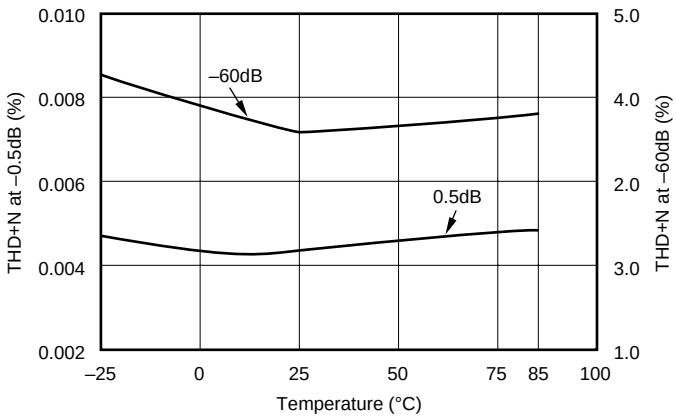
PIN	NAME	I/O	DESCRIPTION
1	$V_{CC}1$	—	ADC Analog Power Supply
2	$V_{CC}1$	—	ADC Analog Power Supply
3	$V_{IN}R$	IN	ADC Analog Input, Rch
4	$V_{REF}L$	—	ADC Reference, Lch
5	$V_{REF}R$	—	ADC Reference, Rch
6	$V_{IN}L$	IN	ADC Analog Input, Lch
7	$\overline{PDAD}$	IN	ADC Power Down, Active LOW(1, 2)
8	$\overline{PDDA}$	IN	DAC Power Down, Active LOW(1, 2)
9	SYSCLK	IN	System Clock Input(2)
10	LRCIN	IN	Sample Rate Clock Input (f_S)(2)
11	BCKIN	IN	Bit Clock Input(2)
12	DOUT	OUT	Data Output
13	DGND	—	Digital Ground
14	V_{DD}	—	Digital Power Supply
15	DIN	IN	Data Input
16	20BIT	IN	20-Bit Format Select(1, 2)
17	DEM1	IN	De-emphasis Control(1, 2)
18	DEM0	IN	De-emphasis Control 0(1, 2)
19	$V_{OUT}L$	OUT	DAC Analog Output, Lch
20	$V_{OUT}R$	OUT	DAC Analog Output, Rch
21	V_{COM}	—	ADC/DAC Common
22	AGND2	—	DAC Analog Ground
23	AGND1	—	ADC Analog Ground
24	$V_{CC}2$	—	DAC Analog Power Supply

NOTE: (1) With 100kΩ typical internal pull-down resistor. (2) Schmitt-Trigger input.

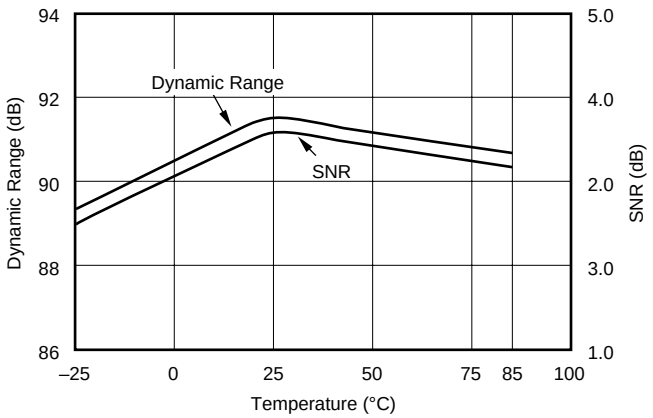
TYPICAL PERFORMANCE CURVES
ADC SECTION

At T_A = +25°C, V_{CC} = V_{DD} = 3.0V, f_S = 44.1kHz, f_{SYSCLK} = 384f_S, and F_{SIGNAL} = 1kHz, unless otherwise noted.

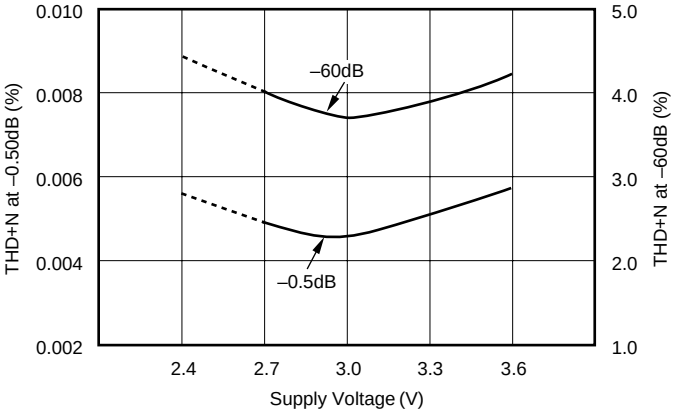
THD+N vs TEMPERATURE



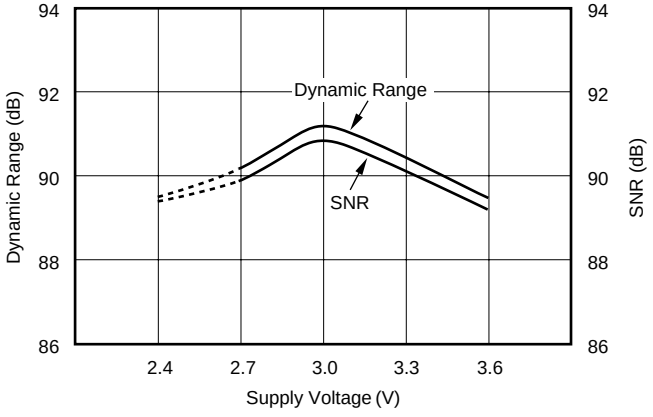
DYNAMIC RANGE and SNR vs TEMPERATURE



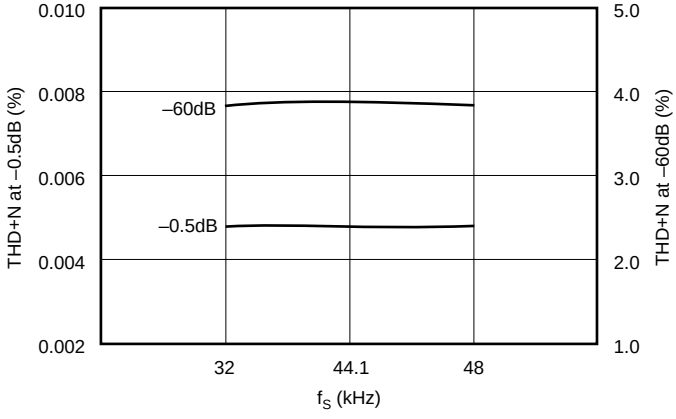
THD+N vs SUPPLY VOLTAGE



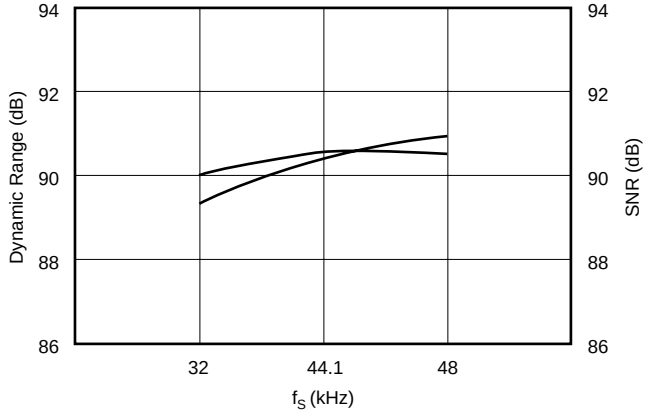
DYNAMIC RANGE and SNR vs SUPPLY VOLTAGE



THD+N vs SAMPLING FREQUENCY



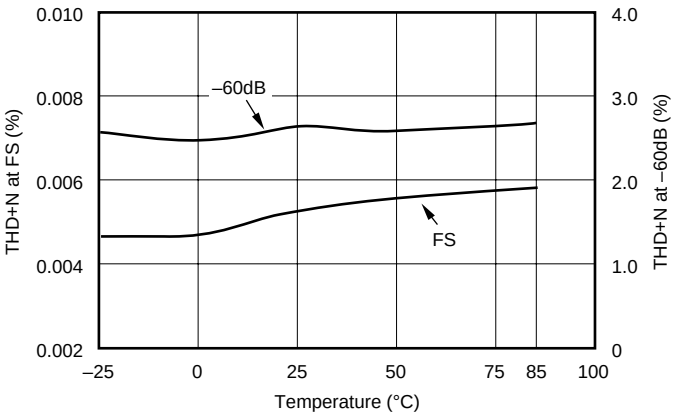
DYNAMIC RANGE and SNR vs SAMPLING FREQUENCY



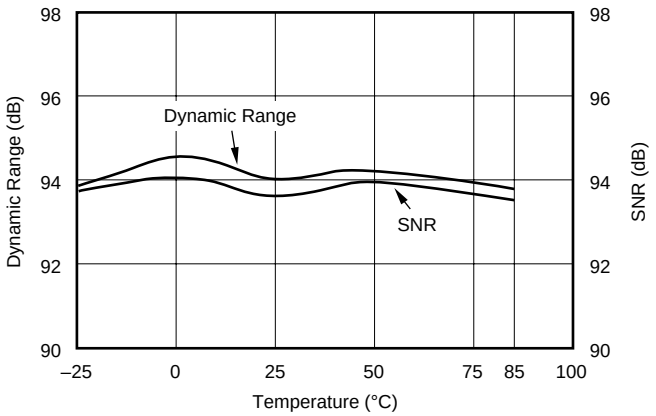
TYPICAL PERFORMANCE CURVES
DAC SECTION

At T_A = +25°C, V_{CC} = V_{DD} = 3.0V, f_S = 44.1kHz, f_{SYSCLK} = 384f_S, and F_{SIGNAL} = 1kHz, unless otherwise noted.

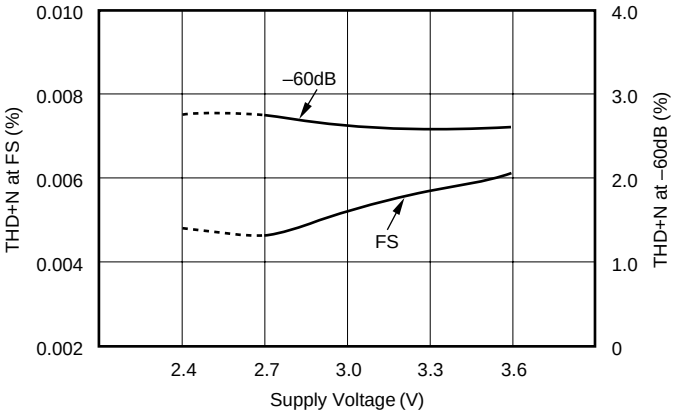
THD+N vs TEMPERATURE



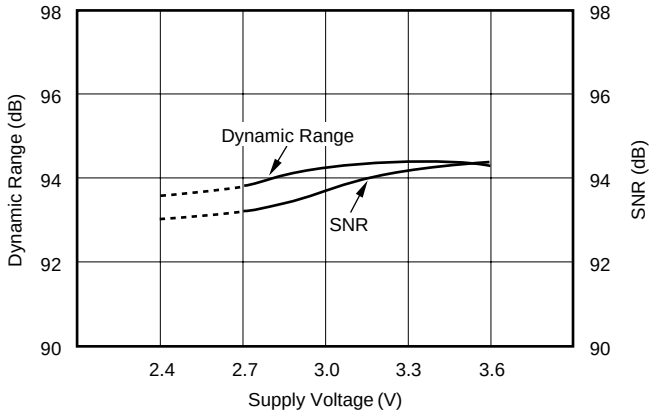
DYNAMIC RANGE and SNR vs TEMPERATURE



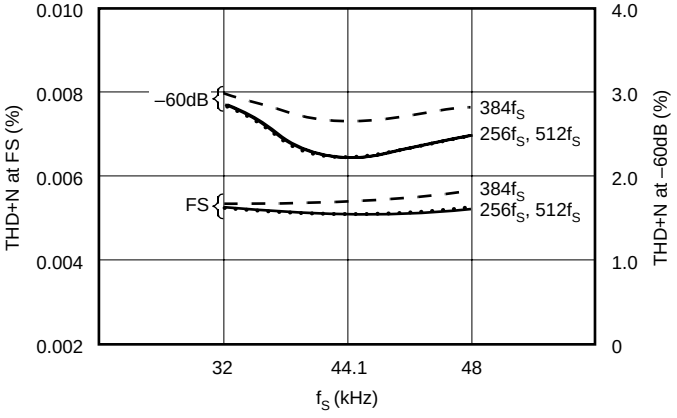
THD+N vs SUPPLY VOLTAGE



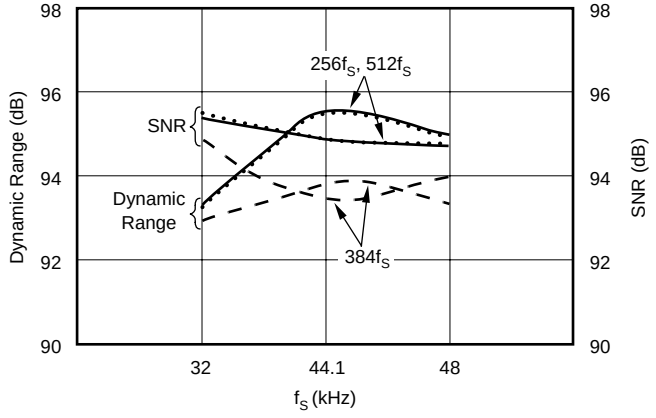
DYNAMIC RANGE and SNR vs SUPPLY VOLTAGE



THD+N vs SAMPLING FREQUENCY
and SYSTEM CLOCK



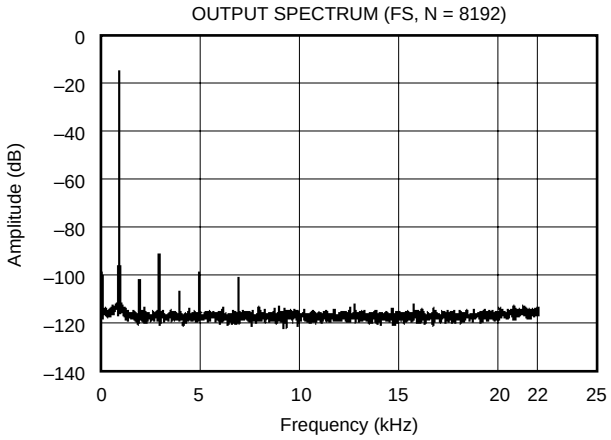
DYNAMIC RANGE and SNR
vs SAMPLING FREQUENCY and SYSTEM CLOCK

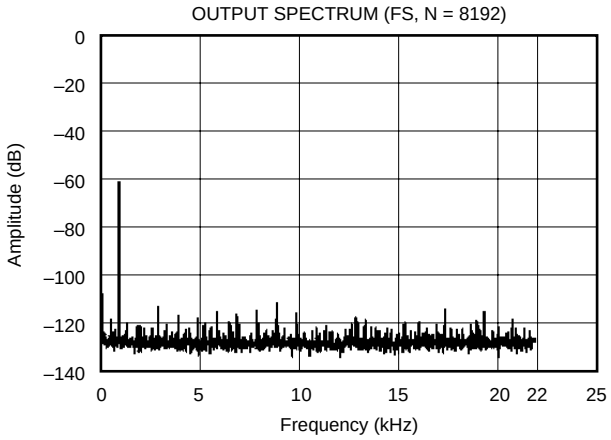


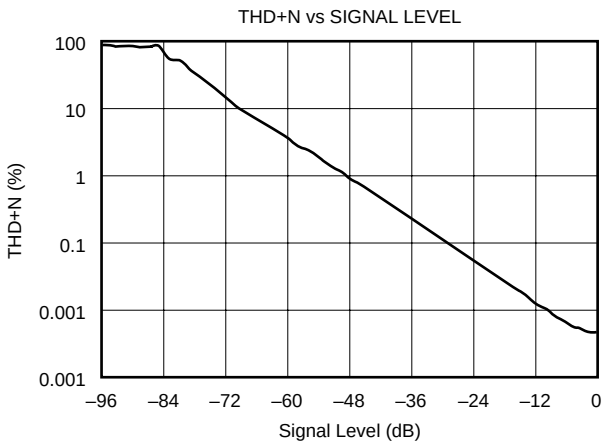
TYPICAL PERFORMANCE CURVES
Output Spectrum

At T_A = +25°C, V_{CC} = V_{DD} = 3.0V, f_S = 44.1kHz, f_{SYSCLK} = 384f_S, and F_{SIGNAL} = 1kHz, unless otherwise noted.

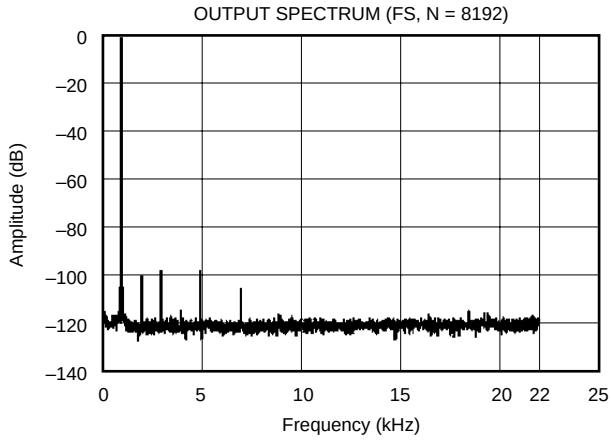
DACs

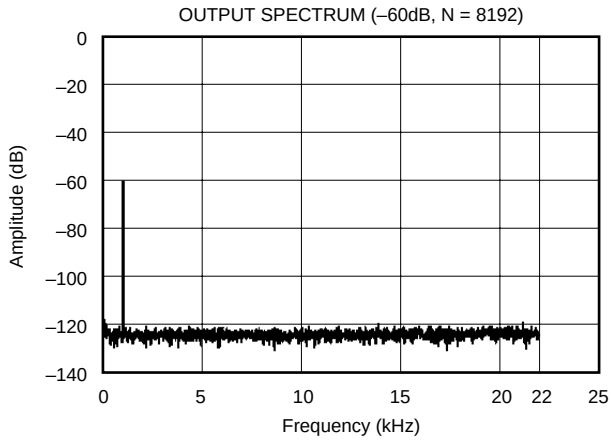


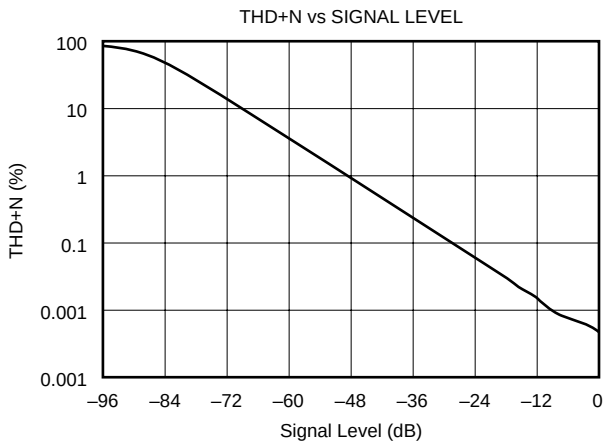




ADCs



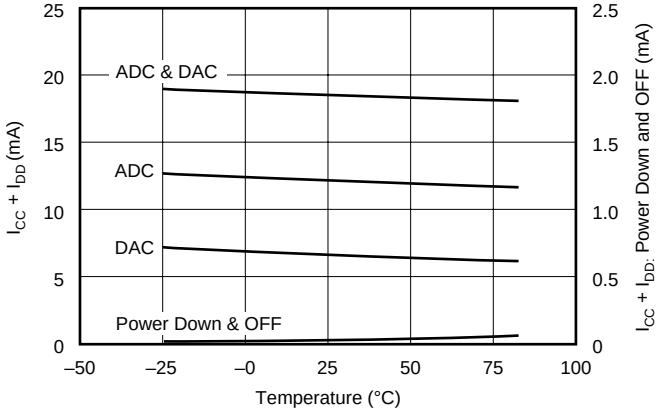




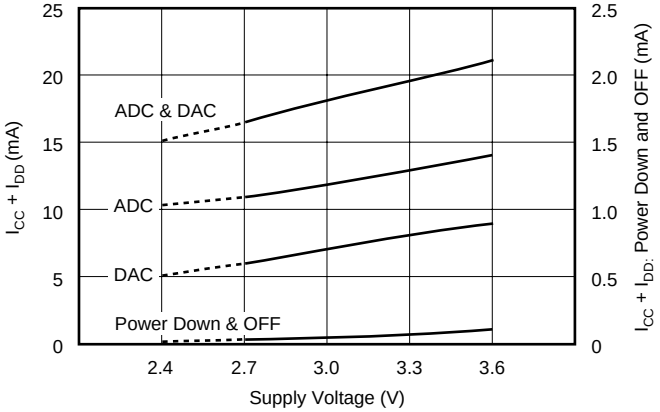
TYPICAL PERFORMANCE CURVES
Supply Current

At T_A = +25°C, V_{CC} = V_{DD} = 3.0V, f_S = 44.1kHz, f_{SYSCLK} = 384f_S, DIN = BPZ, and V_{IN} = BPZ, unless otherwise noted.

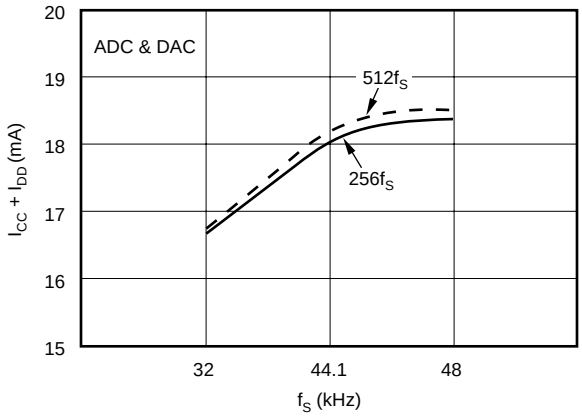
I_{CC} + I_{DD} vs TEMPERATURE



I_{CC} + I_{DD} vs SUPPLY VOLTAGE



I_{CC} + I_{DD} vs SAMPLING FREQUENCY

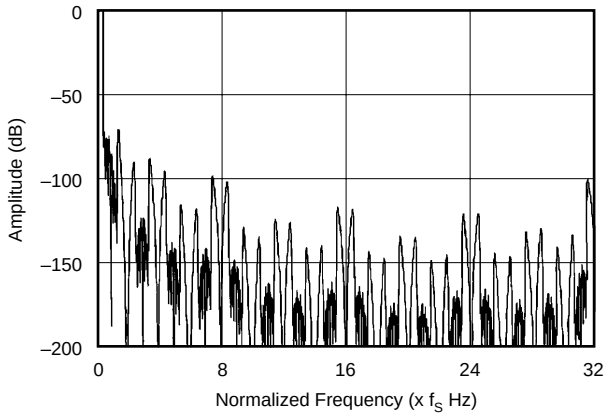


TYPICAL PERFORMANCE CURVES

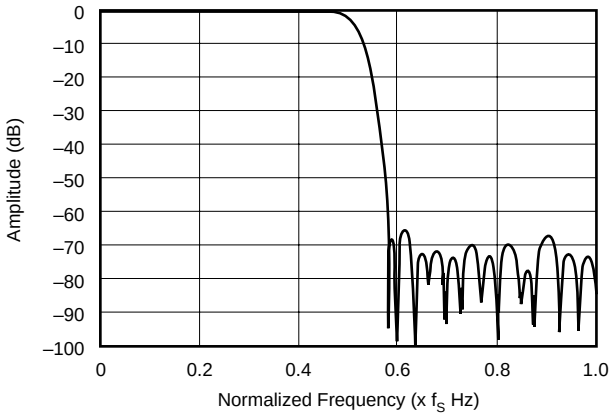
At T_A = +25°C, V_{CC} = V_{DD} = 3.0V, f_S = 44.1kHz, and f_{SYSCLK} = 384f_S, unless otherwise noted.

ADC DIGITAL FILTER

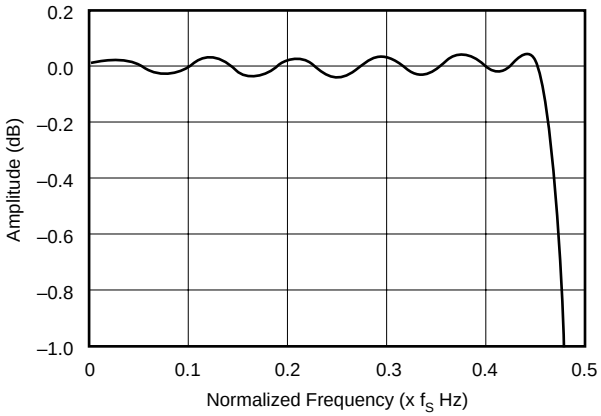
OVERALL CHARACTERISTICS



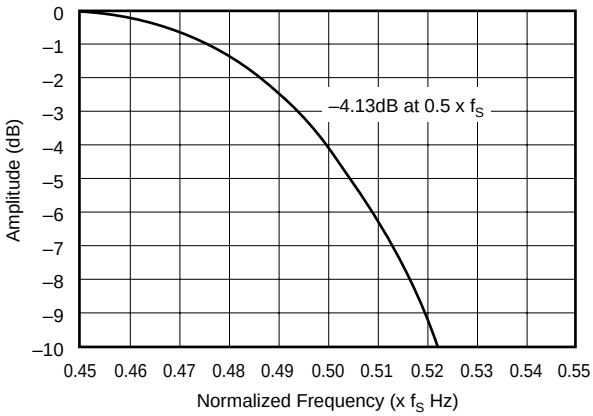
STOPBAND ATTENUATION CHARACTERISTICS



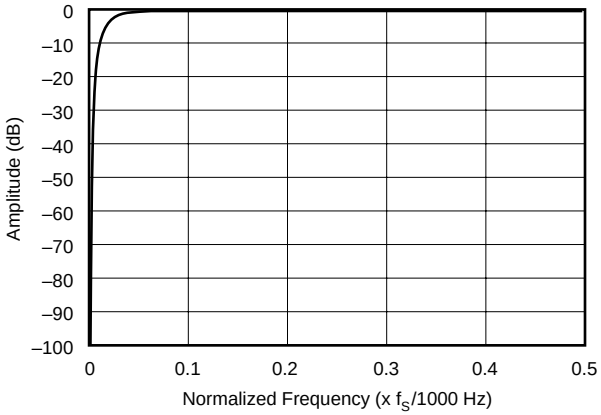
PASSBAND RIPPLE CHARACTERISTICS



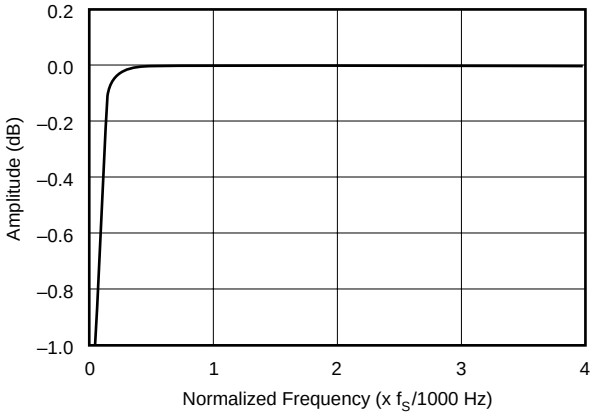
TRANSIENT BAND CHARACTERISTICS



HIGH PASS FILTER RESPONSE



HIGH PASS FILTER RESPONSE

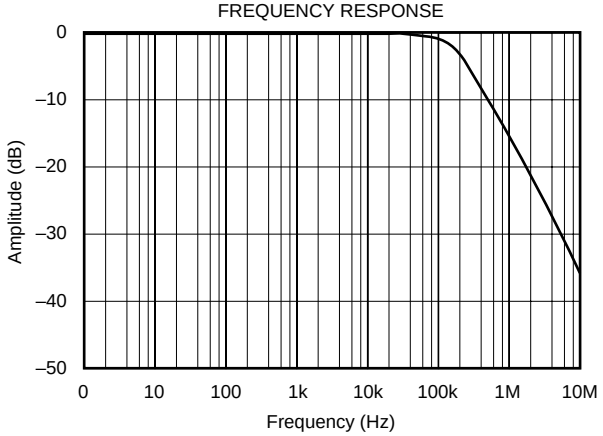


TYPICAL PERFORMANCE CURVES

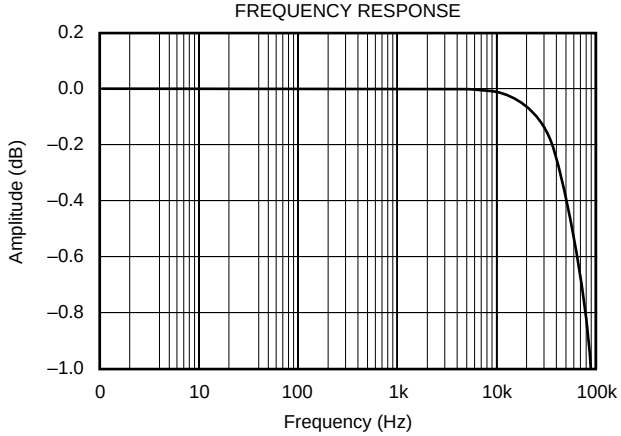
At T_A = +25°C, V_{CC} = V_{DD} = 3.0V, f_S = 44.1kHz, and f_{SYSCLK} = 384f_S, unless otherwise noted.

ANTI-ALIASING FILTER

ANTI-ALIASING FILTER OVERALL FREQUENCY RESPONSE



ANTI-ALIASING FILTER PASSBAND FREQUENCY RESPONSE

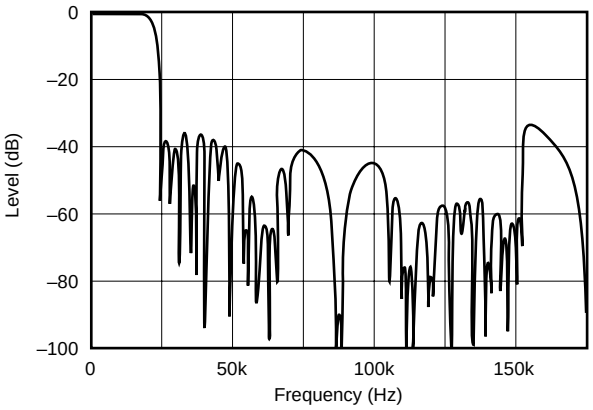


TYPICAL PERFORMANCE CURVES

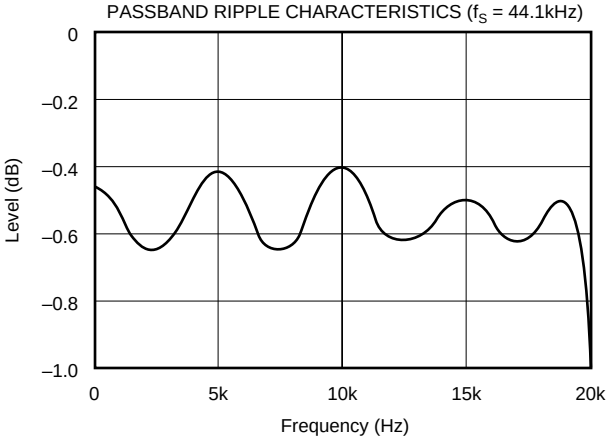
At T_A = +25°C, V_{CC} = V_{DD} = 3.0V, f_S = 44.1kHz, and f_{SYSCLK} = 384f_S, unless otherwise noted.

DAC DIGITAL FILTER

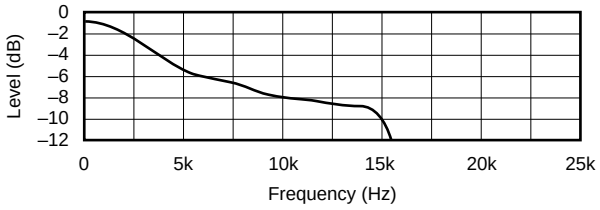
OVERALL FREQUENCY CHARACTERISTICS (f_S = 44.1kHz)



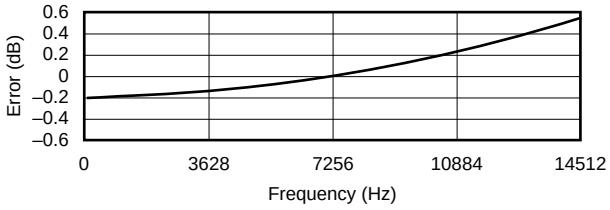
PASSBAND RIPPLE CHARACTERISTICS (f_S = 44.1kHz)



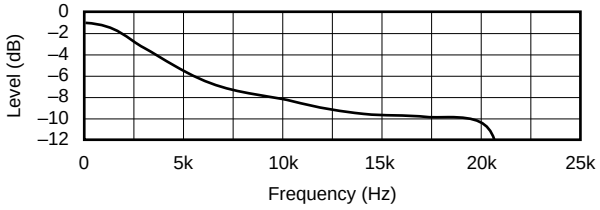
DE-EMPHASIS FREQUENCY RESPONSE (32kHz)



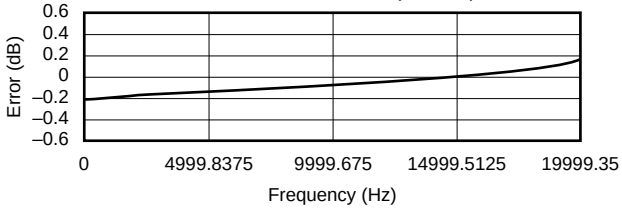
DE-EMPHASIS ERROR (32kHz)



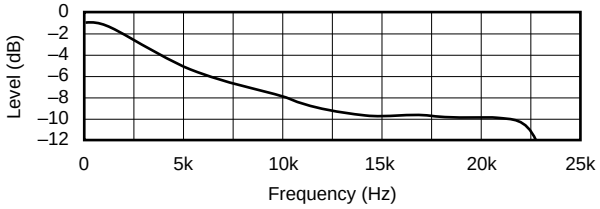
DE-EMPHASIS FREQUENCY RESPONSE (44.1kHz)



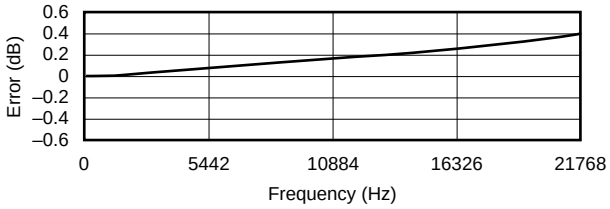
DE-EMPHASIS ERROR (44.1kHz)



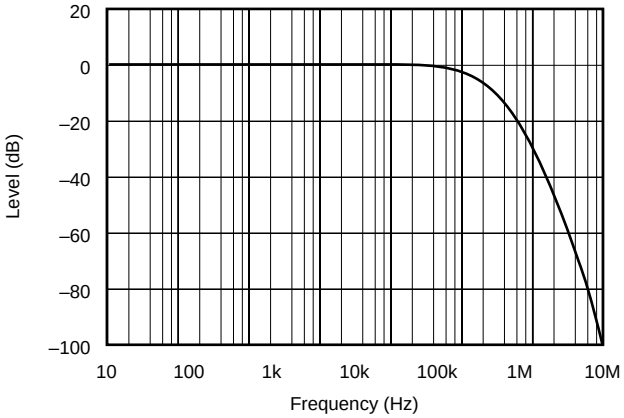
DE-EMPHASIS FREQUENCY RESPONSE (48kHz)



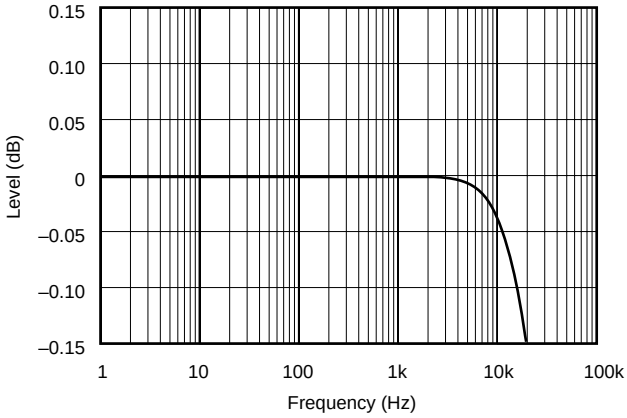
DE-EMPHASIS ERROR (48kHz)



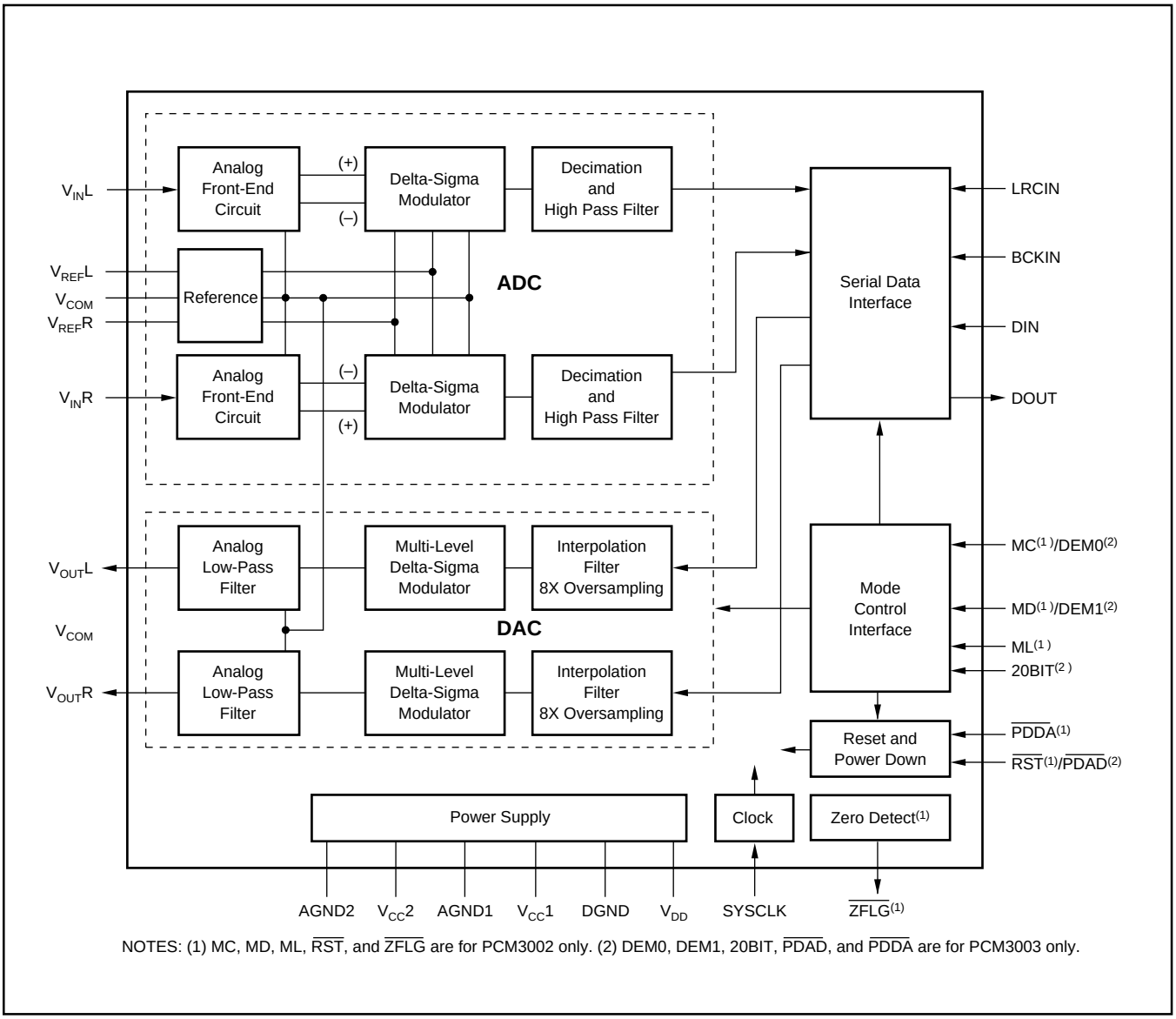
INTERNAL ANALOG FILTER FREQUENCY RESPONSE (10Hz~10MHz)



INTERNAL ANALOG FILTER FREQUENCY RESPONSE (1Hz~20kHz)



BLOCK DIAGRAM



NOTES: (1) MC, MD, ML, $\overline{RST}$, and $\overline{ZFLG}$ are for PCM3002 only. (2) DEM0, DEM1, 20BIT, $\overline{PDAD}$, and $\overline{PDDA}$ are for PCM3003 only.

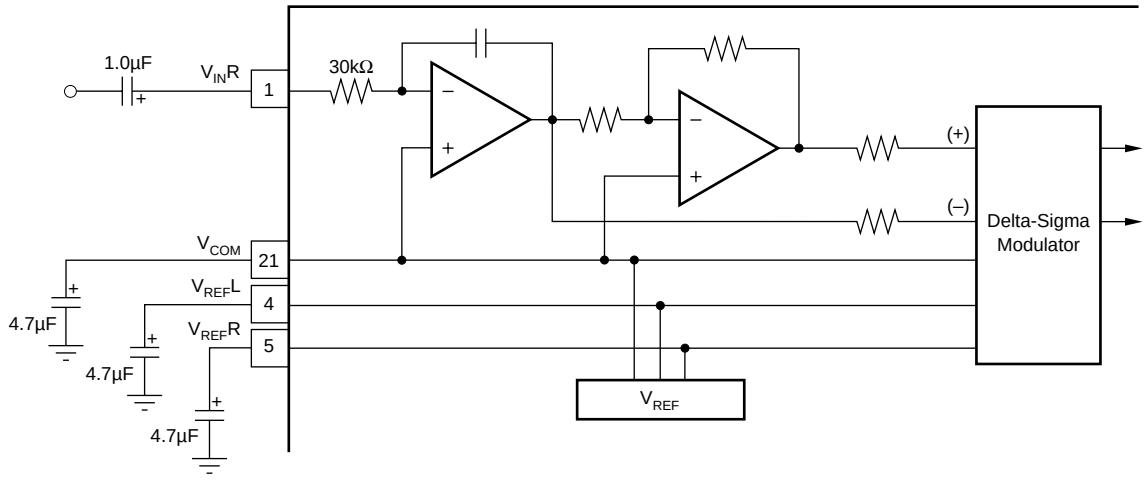


FIGURE 1. Analog Front-End (Single-Channel).

PCM AUDIO INTERFACE

The four-wire digital audio interface for PCM3002/3003 is comprised of: LRCIN (pin 10), BCKIN (pin 11), DIN (pin 15), and DOUT (pin 12). PCM3002/3003 can operate with four different data formats. The PCM3002 may be used with any of the four input/output data formats (Formats 0 - 3), while the PCM3003 may only be used with selected input/output formats (Formats 0 - 1). For PCM3002, these formats are selected through PROGRAM REGISTER 3 in the software mode. For the PCM3003, data formats are selected by 20BIT (pin 16). Figures 2, 3 and 4 illustrate audio data input/output format and timing.

PCM3002/3003 can accept 32-, 48-, or 64-bit clocks (BCKIN) in one clock of LRCIN. Only 16-bit data formats can be selected when 32-bit clocks/LRCIN are applied.

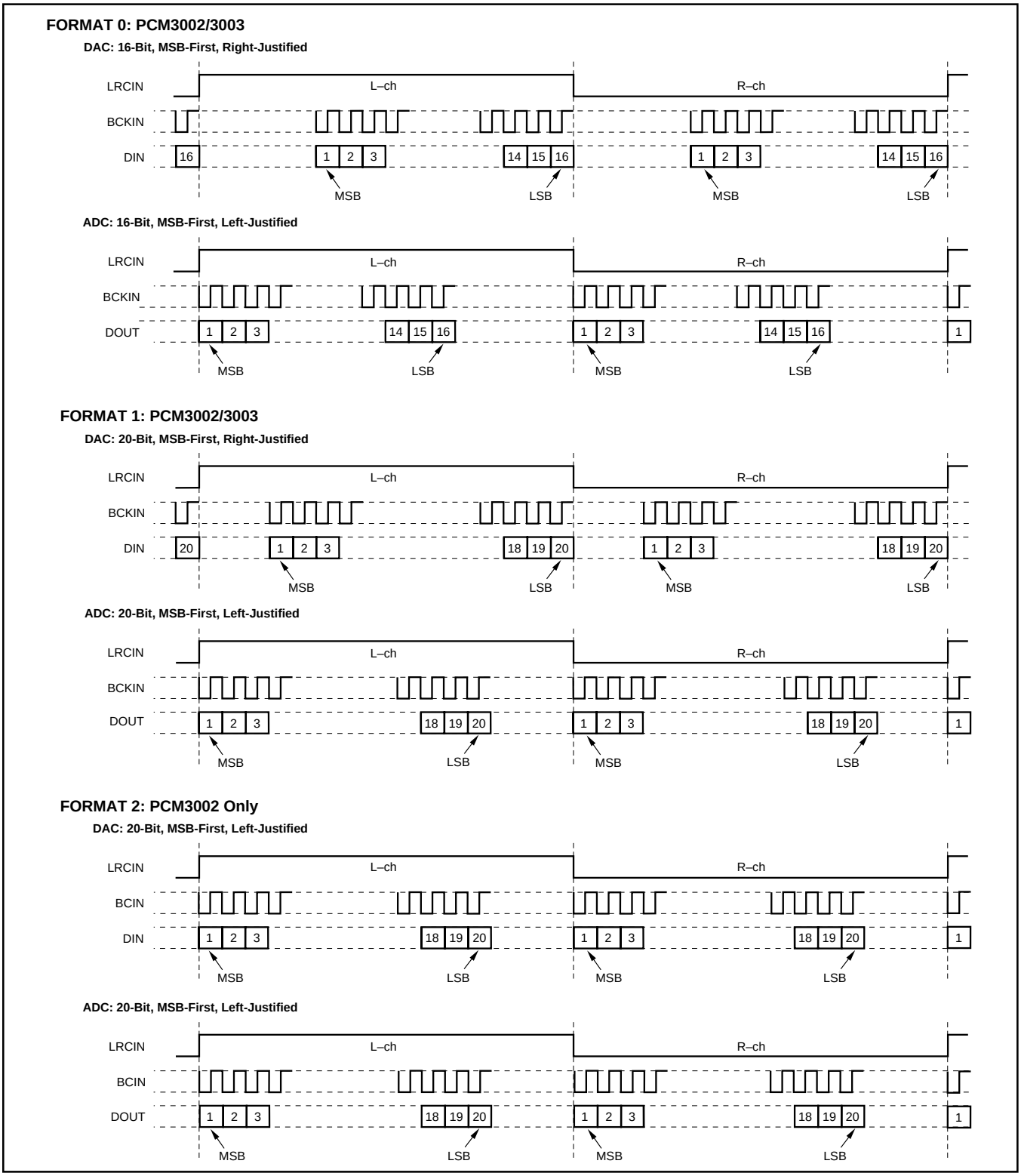


FIGURE 2. Audio Data Input/Output Format.

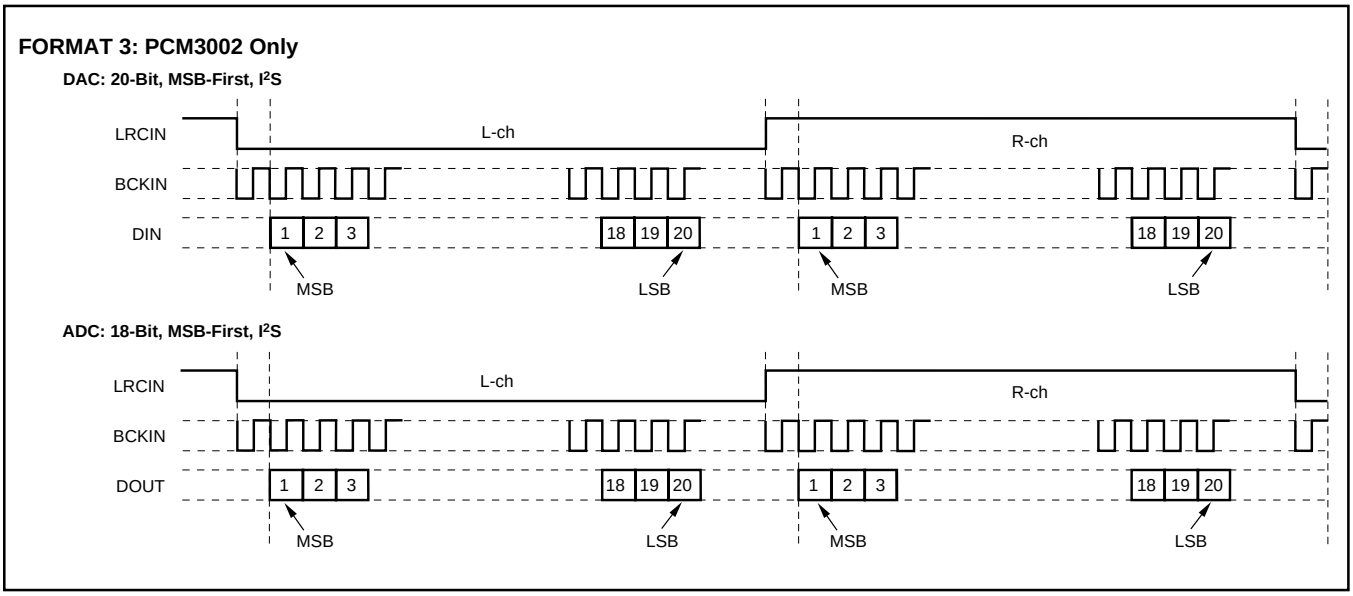
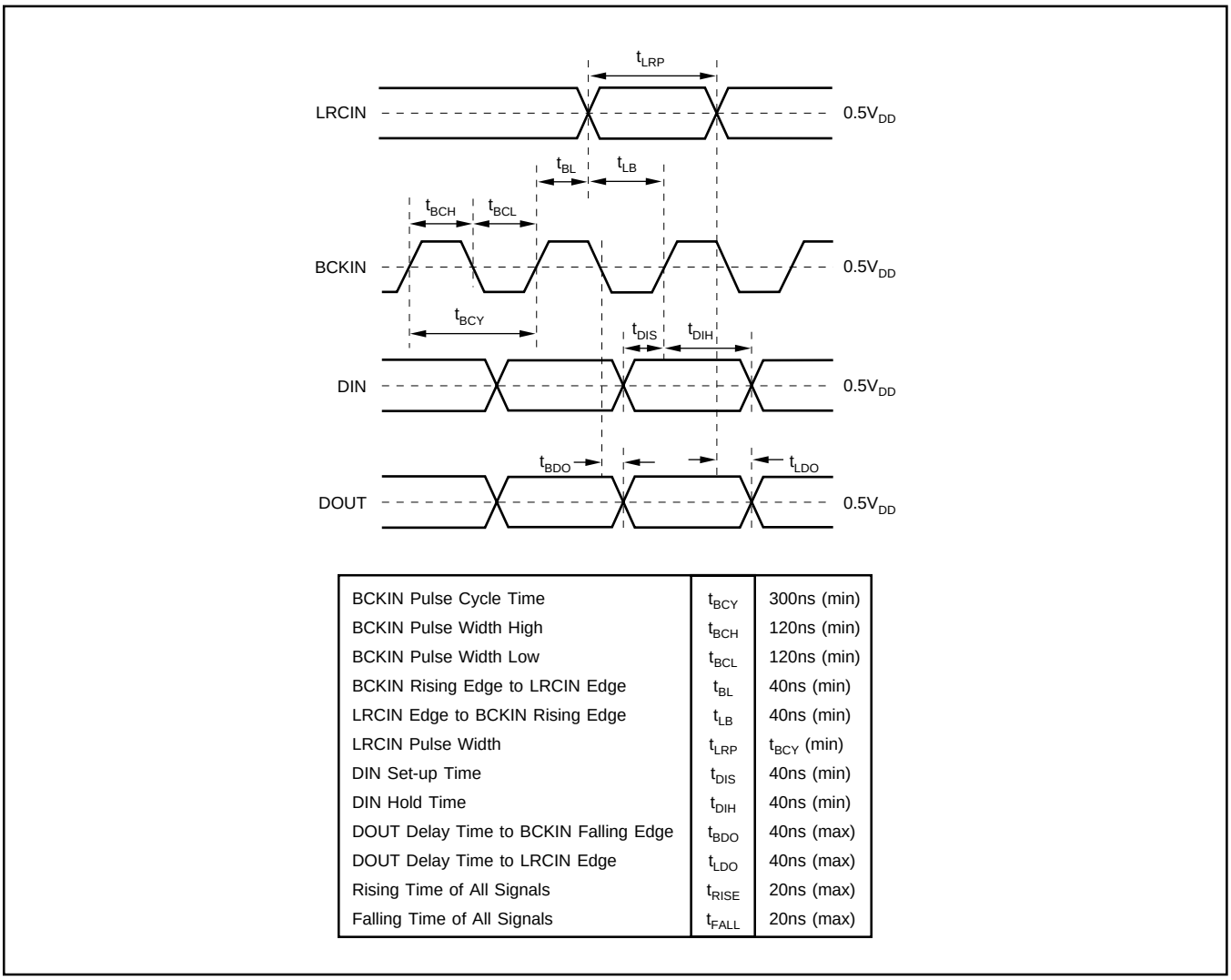


FIGURE 3. Audio Data Input/Output Format.



BCKIN Pulse Cycle Time	t_{BCY}	300ns (min)
BCKIN Pulse Width High	t_{BCH}	120ns (min)
BCKIN Pulse Width Low	t_{BCL}	120ns (min)
BCKIN Rising Edge to LRCIN Edge	t_{BL}	40ns (min)
LRCIN Edge to BCKIN Rising Edge	t_{LB}	40ns (min)
LRCIN Pulse Width	t_{LRP}	t_{BCY} (min)
DIN Set-up Time	t_{DIS}	40ns (min)
DIN Hold Time	t_{DIH}	40ns (min)
DOUT Delay Time to BCKIN Falling Edge	t_{BDO}	40ns (max)
DOUT Delay Time to LRCIN Edge	t_{LDO}	40ns (max)
Rising Time of All Signals	t_{RISE}	20ns (max)
Falling Time of All Signals	t_{FALL}	20ns (max)

FIGURE 4. Audio Data Input/Output Timing.

SYSTEM CLOCK

The system clock for PCM3002/3003 must be either $256f_S$, $384f_S$ or $512f_S$, where f_S is the audio sampling frequency. The system clock should be provided to SYSCLK (pin 9).

PCM3002/3003 also has a system clock detection circuit which automatically senses if the system clock is operating at $256f_S$, $384f_S$, or $512f_S$. When $384f_S$ or $512f_S$ system clock is used, the clock is divded into $256f_S$ automatically. The $256f_S$ clock is used to operate the digital filter and the delta-sigma modulator.

Table I lists the relationship of typical sampling frequencies and system clock frequencies and Figure 5 illustrates the system clock timing.

SAMPLING RATE FREQUENCY (kHz)	SYSTEM CLOCK FREQUENCY (MHz)		
	$256f_S$	$384f_S$	$512f_S$
32	8.1920	12.2880	16.3840
44.1	11.2896	16.9340	22.5792
48	12.2880	18.4320	24.5760

TABLE I. System Clock Frequencies.

RESET

PCM3002/3003 has an internal Power-On Reset circuit, as well as an external forced reset. The internal Power-On Reset initializes (resets) when the supply voltage V_{DD} >2.0V (typ). External forced reset occurs when $\overline{RST}$ = LOW for PCM3002, or both, $\overline{PDAD}$ = LOW and $\overline{PDDA}$ = LOW for PCM3003. During V_{CC} <2.2V and/or internal initialize state (1024 system clocks count after V_{CC} >2.2V) for Power-On Reset or during reset signal is forced to device or internal initialize state (1024 system clocks count after $\overline{PDAD}$ = HIGH or $\overline{PDDA}$ = HIGH) for external reset, the outputs of the DAC are invalid and forced to GND. The analog outputs are then forced to $0.5V_{CC}$ during $t_{DACDLY1}$ ($16384/f_S$) after reset removal. The outputs of ADC are also invalid, the digital outputs are forced to all zero during $t_{ADCDLY1}$ ($18432/f_S$) after reset removal. Figures 6 and 7 illustrate the Power-On reset timing, external reset timing and ADC, DAC output response for Reset and Power-Down ON/OFF.

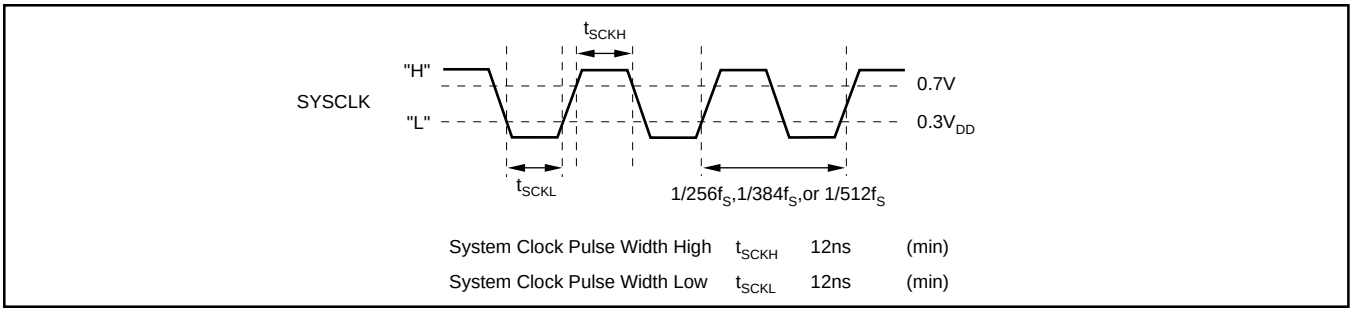


FIGURE 5. System Clock Timing.

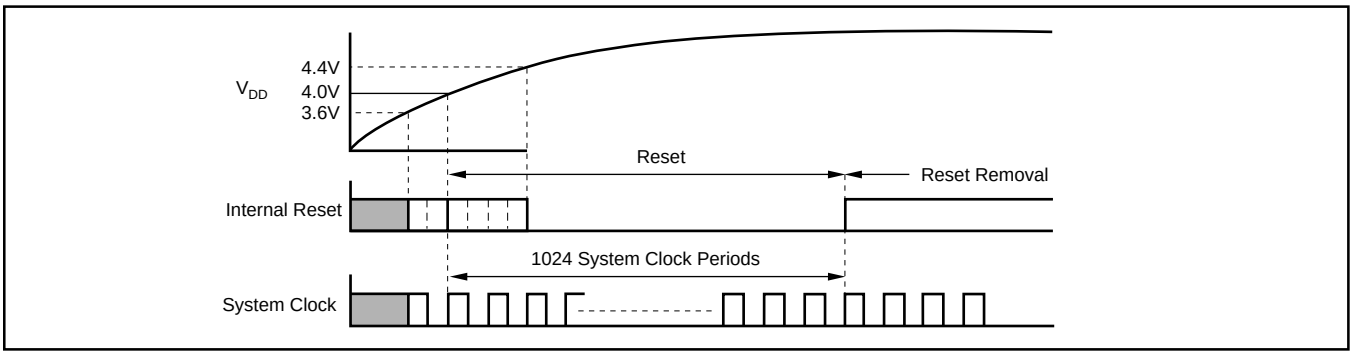


FIGURE 6. Internal Power-On Reset Timing.

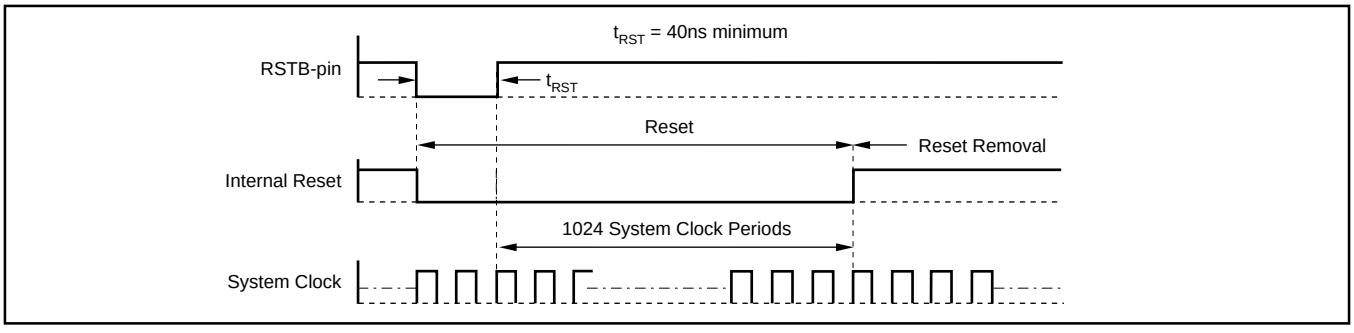


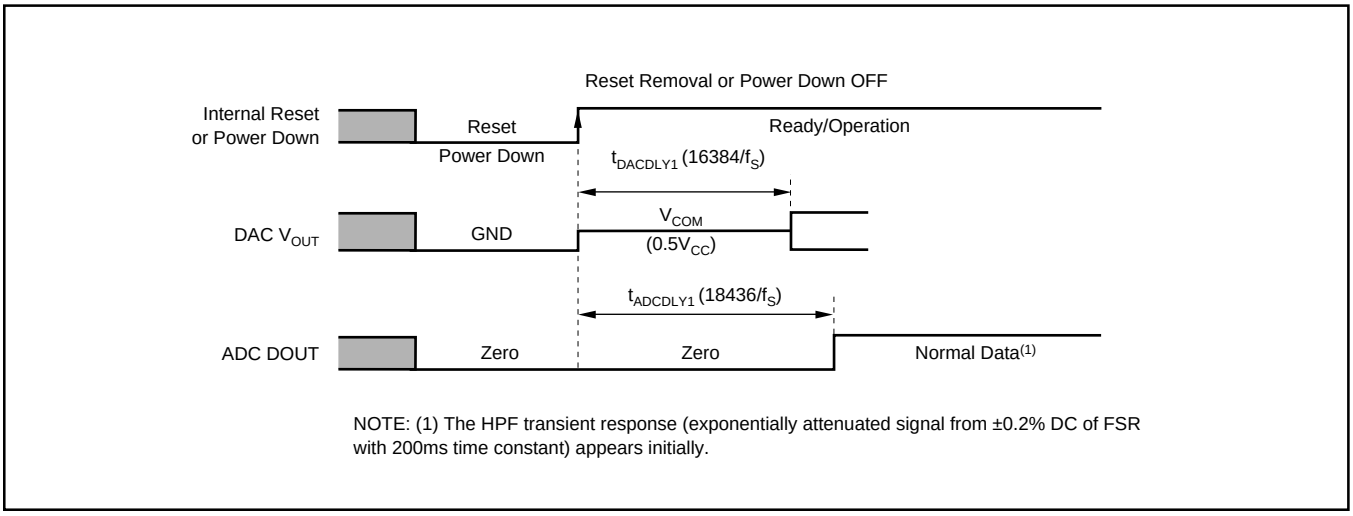
FIGURE 7. External Forced Reset Timing.

SYNCHRONIZATION WITH THE DIGITAL AUDIO SYSTEM

PCM3002/3003 operates with LRCIN synchronized to the system clock. PCM3002/3003 does not require any specific phase relationship between LRCIN and the system clock, but there must be synchronization. If the synchronization between the system clock and LRCIN changes more than 6 bit clocks (BCKIN) during one sample (LRCIN) period because of phase jitter on LRCIN, internal operation of the DAC will stop within $1/f_S$, and the analog output will be forced to bipolar zero ($0.5V_{CC}$) until the system clock is re-synchronized to LRCIN followed by $t_{DACDLY2}$ delay time. Internal operation of the ADC will also stop within $1/f_S$, and the digital output codes will be set to bipolar zero until re-synchronization occurs followed by $t_{ADCDLY2}$ delay time. If LRCIN is synchronized with 5 or less bit clocks to the system clock, operation will be normal. Figures 8 and 9 illustrate the effects on the output when synchronization is lost. Before the outputs are forced to bipolar zero ($<1/f_S$ seconds), the outputs are not defined and some noise may occur. During the transitions between normal data and undefined states, the output has discontinuities, which will cause output noise.

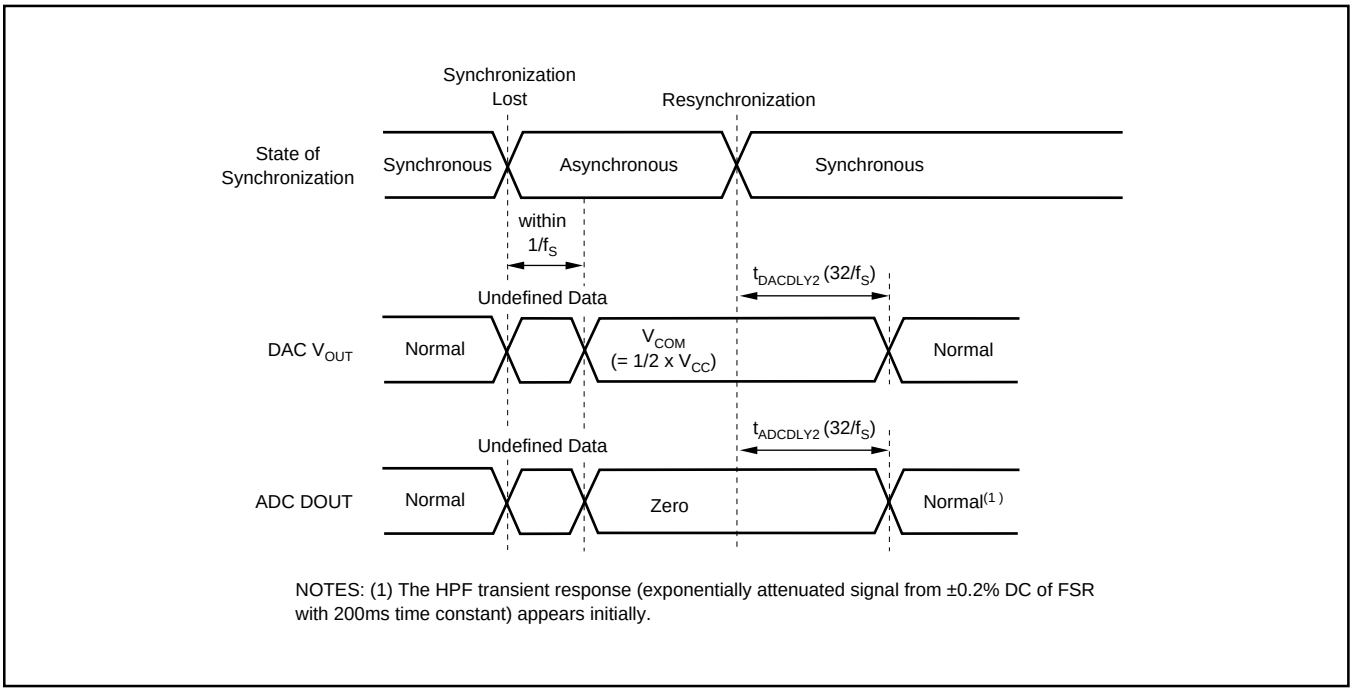
ZERO FLAG OUTPUT: PCM3002 ONLY

Pin 16 is an open-drain output for infinite zero detection flag on the PCM3002 only. When input data is continuously zero for 65,536 BCKIN cycles, $\overline{ZFLG}$ is LOW, otherwise, $\overline{ZFLG}$ is in a high-impedance state.



NOTE: (1) The HPF transient response (exponentially attenuated signal from ±0.2% DC of FSR with 200ms time constant) appears initially.

FIGURE 8. DAC Output and ADC Output for Reset and Power Down.



NOTES: (1) The HPF transient response (exponentially attenuated signal from ±0.2% DC of FSR with 200ms time constant) appears initially.

FIGURE 9. DAC Output and ADC Output for Loss of Synchronization.

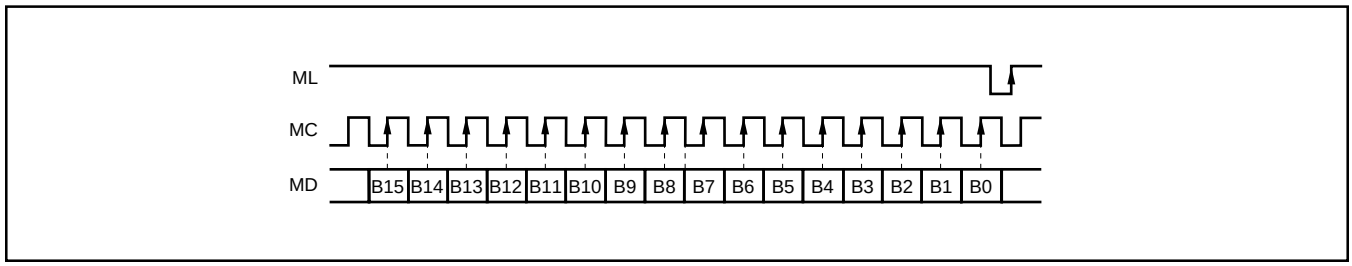
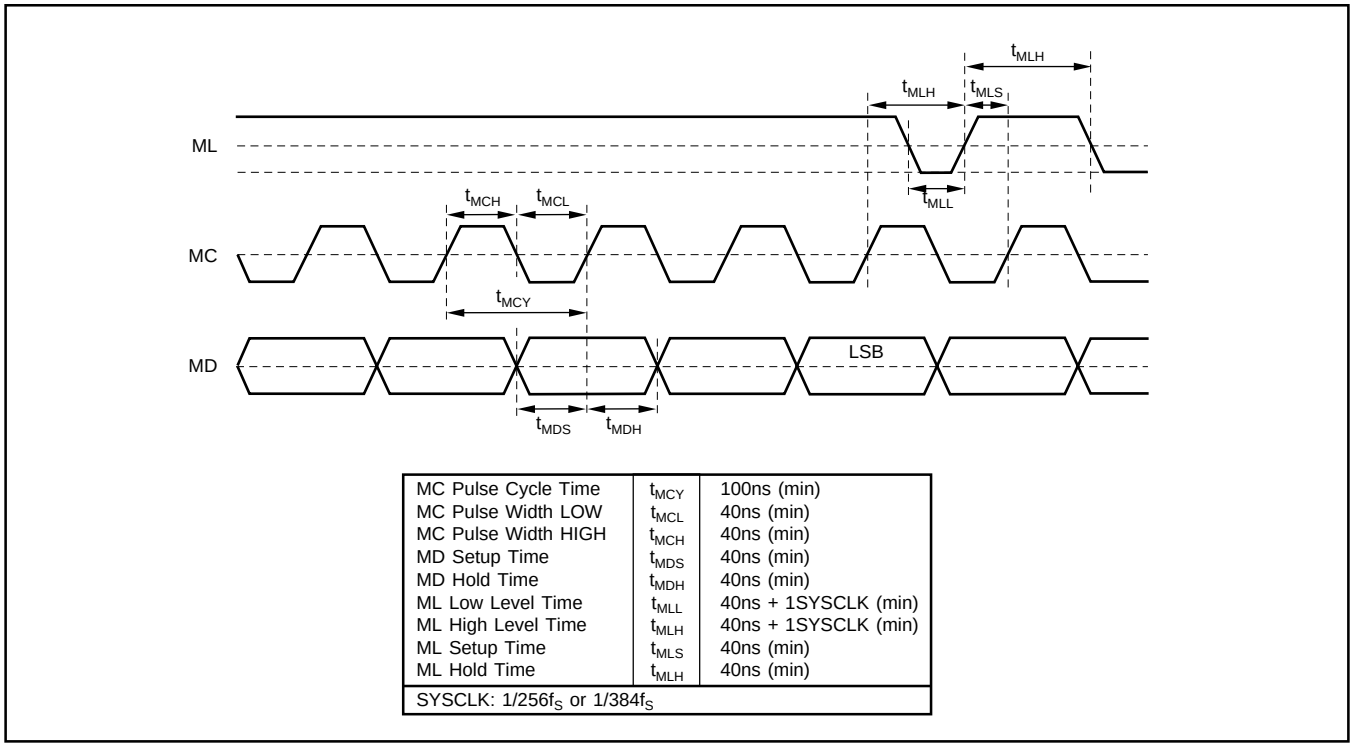


FIGURE 10. Control Data Input Format.



MC Pulse Cycle Time	t_{MCY}	100ns (min)
MC Pulse Width LOW	t_{MCL}	40ns (min)
MC Pulse Width HIGH	t_{MCH}	40ns (min)
MD Setup Time	t_{MDS}	40ns (min)
MD Hold Time	t_{MDH}	40ns (min)
ML Low Level Time	t_{MLL}	40ns + 1SYSCLK (min)
ML High Level Time	t_{MLH}	40ns + 1SYSCLK (min)
ML Setup Time	t_{MLS}	40ns (min)
ML Hold Time	t_{MLH}	40ns (min)
SYSCLK: 1/256f_S or 1/384f_S		

FIGURE 11. Control Data Input Timing.

FUNCTION	ADC/DAC	PCM3002	PCM3002
Audio Data Format	ADC/DAC	4 Selectable Formats	2 Selectable Formats
LRCIN Polarity	ADC/DAC	O	X
Loop-Back Control	ADC/DAC	O	X
Left Channel Attenuation	DAC	O	X
Right Channel Attenuation	DAC	O	X
Attenuation Control	DAC	O	X
Infinite Zero Detection	DAC	O	X
DAC Output Control	DAC	O	X
Soft Mute Control	DAC	O	X
De-Emphasis (OFF, 32kHz, 44.1kHz, 48kHz)	DAC	O	O
ADC Power-Down Control	ADC	O	O
DAC Power-Down Control	DAC	O	O
High Pass Filter Operation	ADC	O	X

TABLE II. Selectable Functions.

OPERATIONAL CONTROL

PCM3002 can be controlled in a software mode with a three-wire serial interface on MC (pin 18), MD (pin 19), and ML (pin 8). Table II indicates selectable functions, and Figure 10 illustrates control data input format and timing. PCM3003 only allows for control of 16-/20-bit data format, digital de-emphasis, and Power-Down Control by hardware pins.

MAPPING OF PROGRAM REGISTERS

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 0	res	res	res	res	res	A1	A0	LDL	AL7	AL6	AL5	AL4	AL3	AL2	AL1	AL0
REGISTER 1	res	res	res	res	res	A1	A0	LDR	AR7	AR6	AR5	AR4	AR3	AR2	AR1	AR0
REGISTER 2	res	res	res	res	res	A1	A0	$\overline{\text{PDAD}}$	BYPS	$\overline{\text{PDDA}}$	ATC	IZD	OUT	DEM1	DEM0	MUT
REGISTER 3	res	res	res	res	res	A1	A0	res	res	res	LOP	res	FMT1	FMT0	LRP	res

SOFTWARE CONTROL (PCM3002)

PCM3002's special functions are controlled using four program registers which are 16 bits long. There are four distinct registers, with bits 9 and 10 determining which register is in use. Table III describes the functions of the four registers.

REGISTER NAME	BIT NAME	DESCRIPTION
Register 0	A (1:0)	Register Address "00"
	res	Reserved, should be set to "0"
	LDL	DAC Attenuation Data Load Control for Lch
	AL (7:0)	Attenuation Data for Lch
Register 1	A (1:0)	Register Address "01"
	res	Reserved, should be set to "0"
	LDR	DAC Attenuation Data Load Control for Rch
	AR (7:0)	DAC Attenuation for Rch
Register 2	A (1:0)	Register Address "10"
	res	Reserved, should be set to "0"
	$\overline{\text{PDAD}}$	ADC Power-Down Control
	$\overline{\text{PDDA}}$	DAC Power-Down Control
	BYPS	ADC High-Pass Filter Operation Control
	ATC	DAC Attenuation Data Mode Control
	IZD	DAC Infinite Zero Detection Circuit Control
	OUT	DAC Output Enable Control
	DEM (1:0)	DAC De-emphasis Control
	MUT	Lch and Rch Soft Mute Control
Register 3	A (1:0)	Register Address "11"
	res	Reserved, should be set to "0"
	LOP	ADC/DAC Analog Loop-Back Control
	FMT (1:0)	ADC/DAC Audio Data Format Selection
	LRP	ADC/DAC Polarity of LR-clock Selection

TABLE III. Functions of the Registers.

PROGRAM REGISTER 0

A (1:0): Bit 10, 9 Register Address

These bits define the address for REGISTER 0:

A1	A0	
0	0	Register 0

res: Bit 11 : 15 Reserved

These bits are reserved and should be set to "0".

LDL: Bit 8 DAC Attenuation Data Load Control for Left Channel

This bit is used to simultaneously set analog outputs of the left and right channels. The output level is controlled by AL (7:0) attenuation data when this bit is set to "1". When set to "0", the new attenuation data will be ignored, and the output level will remain at the previous attenuation level. The LDR bit in REGISTER 1 has the equivalent function as LDL. When either LDL or LDR is set to "1", the output level of the left and right channels are simultaneously controlled.

AL (7:0): Bit 7:0 DAC Attenuation Data for Left Channel

AL7 and AL0 are MSB and LSB, respectively. The attenuation level (ATT) is given by:

$$ATT = 20 \times \log_{10} (ATT\ data/255)\ (dB)$$

AL (7:0)	ATTENUATION LEVEL
00h	–∞dB (Mute)
01h	–48.16dB
:	:
FEh	–0.07dB
FFh	0dB

PROGRAM REGISTER 1

A (1:0): Register Address

These bits define the address for REGISTER 1:

A1	A0	
0	1	Register 1

res: Bit 15:11 Reserved

These bits are reserved and should be set to "0"

LDR: Bit 8 DAC Attenuation Data Load Control for Right Channel

This bit is used to simultaneously set analog outputs of the left and right channels. The output level is controlled by AL (7:0) attenuation data when this bit is set to "1". When set to "0", the new attenuation data will be ignored, and the output level will remain at the previous attenuation level. The LDL bit in REGISTER 0 has the equivalent function as LDR. When either LDL or LDR is set to "1", the output level of the left and right channels are simultaneously controlled.

AR (7:0): Bit 7:0 DAC Attenuation Data for Left Channel

AR7 and AR0 are MSB and LSB respectively. See REGISTER 0 for the attenuation formula.

PROGRAM REGISTER 2

A (1:0): Bit 10, 9 Register Address

These bits define the address for REGISTER 2:

A1	A0	
1	0	Register 2

res: Bit 15:11, 6 Reserved

These bits are reserved and should be set to “0”.

$\overline{\text{PDAD}}$: Bit 8 ADC Power-Down Control

This bit places the ADC section in the lowest power consumption mode. The ADC operation is stopped by cutting the supply current to the ADC section, and DOUT is fixed to zero during ADC Power-down mode enable. Figure 8 illustrates the ADC DOUT response for ADC power-down ON/OFF. This does not affect the DAC operation.

$\overline{\text{PDAD}}$	DAC POWER-DOWN
0	Power Down Mode Disabled
1	Power Down Mode Enabled

BYPS: Bit 7 ADC High-Pass Filter Bypass Control

This bit determines enables or disables the high-pass filter for the ADC.

BYPS	
0	High-Pass Filter Enabled
1	High-Pass Filter Disabled (bypassed)

$\overline{\text{PDDA}}$: Bit 6 DAC Power-Down Control

This bit places the DAC section in the lowest power consumption mode. The DAC operation is stopped by cutting the supply current to the DAC section and V_{OUT} is fixed to GND during DAC Power-Down Mode enable. Figure 8 illustrates the DAC V_{OUT} response for DAC Power-Down ON/OFF. This does not affect the ADC operation.

$\overline{\text{PDDA}}$	
0	Power-Down Mode Disabled
1	Power-Down Mode Enabled

ATC: Bit 5 DAC Attenuation Channel Control

When set to “1”, the REGISTER 0 attenuation data can be used for both DAC channels. In this case, the REGISTER 1 attenuation data is ignored.

ATC	
0	Individual Channel Attenuation Data Control
1	Common Channel Attenuation Data Control

IZD: Bit 4 DAC Infinite Zero Detection Circuit Control

This bit enables the Infinite Zero Detection Circuit in PCM3002. When enabled, this circuit will disconnect the analog output amplifier from the delta-sigma DAC when the input is continuously zero for 65,536 consecutive cycles of BCKIN.

IZD	
0	Infinite Zero Detection Disabled
1	Infinite Zero Detection Enabled

OUT: Bit 3 DAC Output Enable Control

When set to “1”, the outputs are forced to $V_{CC}/2$ (bipolar zero). In this case, all registers in PCM3002 hold the present data. Therefore, when set to “0”, the outputs return to the previous programmed state.

OUT	
0	DAC Outputs Enabled (normal operation)
1	DAC Outputs Disabled (forced to BPZ)

DEM (1:0): Bit 2,1 DAC De-emphasis Control

These bits select the de-emphasis mode as shown below:

DEM1	DEM0	
0	0	De-emphasis 44.1kHz ON
0	1	De-emphasis OFF
1	0	De-emphasis 48kHz ON
1	1	De-emphasis 32kHz ON

MUT: Bit 0 DAC Soft Mute Control

When set to “1”, both left and right-channel DAC outputs are muted at the same time. This muting is done by attenuating the data in the digital filter, so there is no audible click noise when soft mute is turned on.

MUT	
0	Mute Disable
1	Mute Enable

PROGRAM REGISTER 3

A (1:0): Bit 10:9 Register Address

These bits define the address for REGISTER 3:

A1	A0	
1	1	Register 3

res: Bit 15:11, 8:6, 4:0 Reserved

These bits are reserved, and should be set to “0”.

LOP: Bit 5 ADC to DAC Loop-Back Control

When this bit is set to “1”, the ADC’s audio data is sent directly to the DAC. The data format will default to I²S. In Format 3 (I²S Frame), Loop-back is not supported.

LOP	
0	Loop-back Disable
1	Loop-back Enable

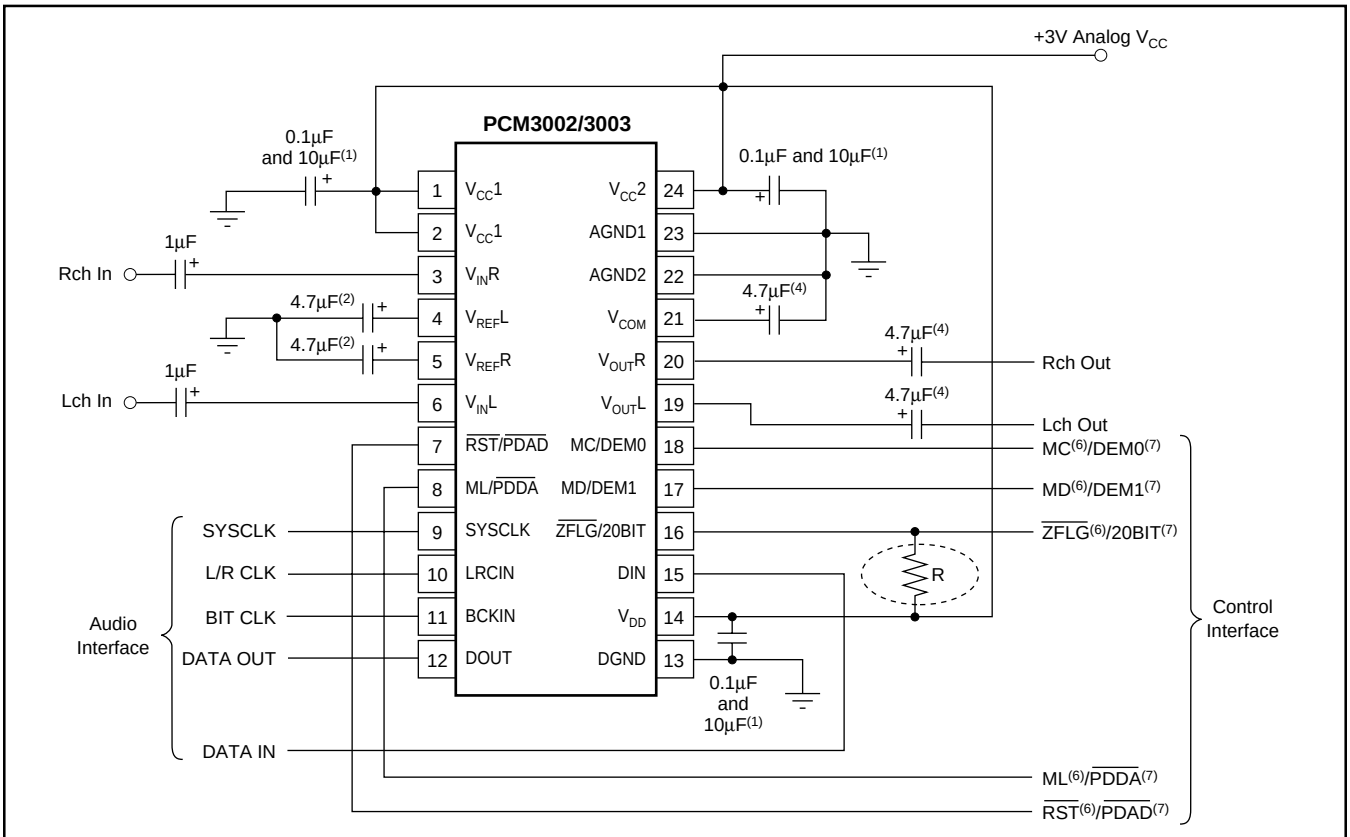
FMT (1,0) Bit 3:2 Audio Data Format Select

These bits determine the input and output audio data formats.

FMT1	FMT0	DAC Data Format	ADC Data Format	NAME
0	0	16-bit, MSB-first, Right-justified	16-bit, MSB-first, Left-justified	Format 0
0	1	20-bit, MSB-first, Right-justified	20-bit, MSB-first, Left-justified	Format 1
1	0	20-bit, MSB-first, Left-justified	20-bit, MSB-first, Left-justified	Format 2
1	1	20-bit, MSB-first, I²S	20-bit, MSB-first, I²S	Format 3

LRP: Bit 1 ADC and DAC Polarity of LR-clock Selection. Applies only to Formats 0 through 2.

LRP	
0	Left-channel is “H”, Right-channel is “L”.
1	Left-channel is “L”, Right-channel is “H”.



NOTES: (1) 0.1µF ceramic and 10µF tantalum, typical, depending on power supply quality and pattern layout. (2) 4.7µF typical, gives settling time with 30ms (4.7µF x 6.4kΩ) time constant in Power ON and Power-Down OFF period. (3) 1µF typical, gives 5.3Hz cut-off frequency of input HPF in normal operation and gives settling time with 30ms (1µF x 30kΩ) time constant in Power ON and Power -Down OFF period. (4) 4.7µF typical, gives 3.4Hz cut-off frequency of output HPF in normal operation and gives settling time with 47ms (4.7µF x 10kΩ) time constant in Power ON and Power-Down OFF period. (5) Post low pass filter with R_{IN} >10kΩ, depending on requirement of system performance. (6) MC, MD, ML, $\overline{ZFLG}$, $\overline{RST}$ and 10kΩ pull-up resistor are for the PCM3002. (7) DEM0, DEM1, 20BIT, $\overline{PDAD}$, $\overline{PDDA}$ are for the PCM3003.

FIGURE 12. Typical Connection Diagram for PCM3002/3003.

PCM3003 DATA FORMAT CONTROL

PCM3003 has hardwire functional control using $\overline{\text{PDAD}}$ (pin 7) and $\overline{\text{PDDA}}$ (pin 8) for Power-Down Control, DEM0 (pin 18) and DEM1 (pin 17) for de-emphasis and 20BIT (pin 16) for 16-/20-bit format selection.

Power-Down Control (Pin 7 and Pin 8)

Both the ADC's and DAC's Power-Down Control pins place the ADC or DAC section in the lowest power consumption mode. The ADC/DAC operation is stopped by cutting the supply current to the ADC/DAC section. DOUT is fixed to zero during ADC Power-Down Mode enable and V_{OUT} is fixed to GND during DAC Power-Down Mode enable. Figure 7 illustrates the ADC and DAC output response for Power-Down ON/OFF. This does not affect the ADC or DAC operation.

$\overline{\text{PDAD}}$	$\overline{\text{PDDA}}$	POWER DOWN
Low	Low	Reset (ADC/DAC Power-Down Enable)
Low	High	ADC Power-Down/DAC Operate
High	Low	ADC Operate/DAC Power-Down
High	High	ADC and DAC Normal Operation

De-Emphasis Control (Pin 17 and Pin 18)

DEM0 (pin 18) and DEM1 (pin 17) are used as de-emphasis control pins.

DEM1	DEM0	DE-EMPHASIS
Low	Low	De-Emphasis Enable at 44.1kHz
Low	High	De-Emphasis Disable
High	Low	De-Emphasis Enable at 48kHz
High	High	De-Emphasis Enable at 32kHz

20BIT Audio Data Selection (Pin 16)

20BIT	FORMAT
Low	ADC: 16-bit MSB-first, Left-justified DAC: 16-bit MSB-first, Right-justified
High	ADC: 20-bit MSB-first, Left-justified DAC: 20-bit MSB-first, Right-justified

APPLICATION AND LAYOUT CONSIDERATIONS

POWER SUPPLY BYPASSING

The digital and analog power supply lines to PCM3002/3003 should be bypassed to the corresponding ground pins with both 0.1µF ceramic and 10µF tantalum capacitors as close to the device pins as possible. Although PCM3002/3003 has three power supply lines to optimize dynamic performance, the use of one common power supply is generally recommended to avoid unexpected latch-up or pop noise due to power supply sequencing problems. If separate power supplies are used, back-to-back diodes are recommended to avoid latch-up problems.

GROUNDING

In order to optimize the dynamic performance of PCM3002/3003, the analog and digital grounds are not connected internally. The PCM3002/3003 performance is optimized with a single ground plane for all returns. It is recommended to tie all PCM3002/3003 ground pins with low impedance connections to the analog ground plane. PCM3002/3003 should reside entirely over this plane to avoid coupling high frequency digital switching noise into the analog ground plane.

VOLTAGE INPUT PINS

A tantalum capacitor, between 1µF and 10µF, is recommended as an AC-coupling capacitor at the inputs. Combined with the 30kΩ characteristic input impedance, a 1.0µF coupling capacitor will establish a 5.3Hz cut-off frequency for blocking DC. The input voltage range can be increased by adding a series resistor on the analog input line. This series resistor, when combined with the 30kΩ input impedance, creates a voltage divider and enables larger input ranges.

V_{REF} INPUTS

A 4.7µF to 10µF tantalum capacitor is recommended between $V_{REF}L$, $V_{REF}R$, and AGND1 to ensure low source impedance for the ADC's references. These capacitors should be located as close as possible to the reference pins to reduce dynamic errors on the ADC reference.

V_{COM} INPUTS

A 4.7µF to 10µF tantalum capacitor is recommended between V_{COM} and AGND1 to ensure low source impedance of the ADC and DAC common voltage. This capacitor should be located as close as possible to the V_{COM} pin to reduce dynamic errors on the DAC common.

SYSTEM CLOCK

The quality of the system clock can influence dynamic performance of both the ADC and DAC in the PCM3002/3003. The duty cycle and jitter at the system clock input pin must be carefully managed. When power is supplied to the part, the system clock, bit clock (BCKIN) and a word clock (LCRIN) should also be supplied simultaneously. Failure to supply the audio clocks will result in a power dissipation increase of up to three times normal dissipation and may degrade long term reliability if the maximum power dissipation limit is exceeded.

RST CONTROL

If the capacitance between V_{REF} and V_{COM} exceeds 2.2µF, an external reset control delay time circuit must be used.

EXTERNAL MUTE CONTROL

For Power-Down ON/OFF control without click noise which is generated by DAC output DC level change, the External Mute control is general required. The control sequence, which is External Mute ON, CODEC Power-Down ON, SYSCLK stop and resume if necessary, CODEC Power-down OFF, and External Mute OFF is recommended. Note that if SYSCLK is stopped when Power-Down condition for the PCM3002, all internal mode is initialized and need to re-write mode register value.

THEORY OF OPERATION

ADC SECTION

The PCM3002/3003 ADC consists of two reference circuits, a stereo single-to-differential converter, a fully differential 5th-order delta-sigma modulator, a decimation filter (including digital high pass), and a serial interface circuit. The Block Diagram in this data sheet illustrates the architecture of the ADC section, Figure 1 shows the single-to-differential converter, and Figure 14 illustrates the architecture of the 5th-order delta-sigma modulator and transfer functions.

An internal reference circuit with three external capacitors provides all reference voltages which are required by the ADC, which defines the full scale range for the converter. The internal single-to-differential voltage converter saves the design, space and extra parts needed for external circuitry required by many delta-sigma converters. The internal full-differential signal processing architecture provides a wide dynamic range and excellent power supply rejection performance. The input signal is sampled at 64X oversampling rate, eliminating the need for a sample-and-hold circuit, and simplifying anti-alias filtering requirements. The 5th-order delta-sigma noise shaper consists of five integrators which use a switched-capacitor topology, a comparator and a feedback loop consisting of a one-bit DAC. The delta-sigma modulator shapes the quantization noise, shifting it out of the audio band in the frequency domain. The high order of the modulator enables it to randomize the modulator outputs, reducing idle tone levels.

The $64f_S$ one-bit data stream from the modulator is converted to $1f_S$ 18-bit data words by the decimation filter, which also acts as a low pass filter to remove the shaped quantization noise. The DC components are removed by a high pass filter function contained within the decimation filter.

THEORY OF OPERATION

DAC SECTION

The delta-sigma DAC section of PCM3002/3003 is based on a 5-level amplitude quantizer and a 3rd-order noise shaper. This section converts the oversampled input data to 5-level delta-sigma format. A block diagram of the 5-level delta-sigma modulator is shown in Figure 14. This 5-level delta-sigma modulator has the advantage of stability and clock jitter sensitivity over the typical one-bit (2 level) delta-sigma modulator. The combined oversampling rate of the delta-sigma modulator and the internal 8X interpolation filter is $64f_S$ for a $256f_S$system clock. The theoretical quantization noise performance of the 5-level delta-sigma modulator is shown in Figure 15.

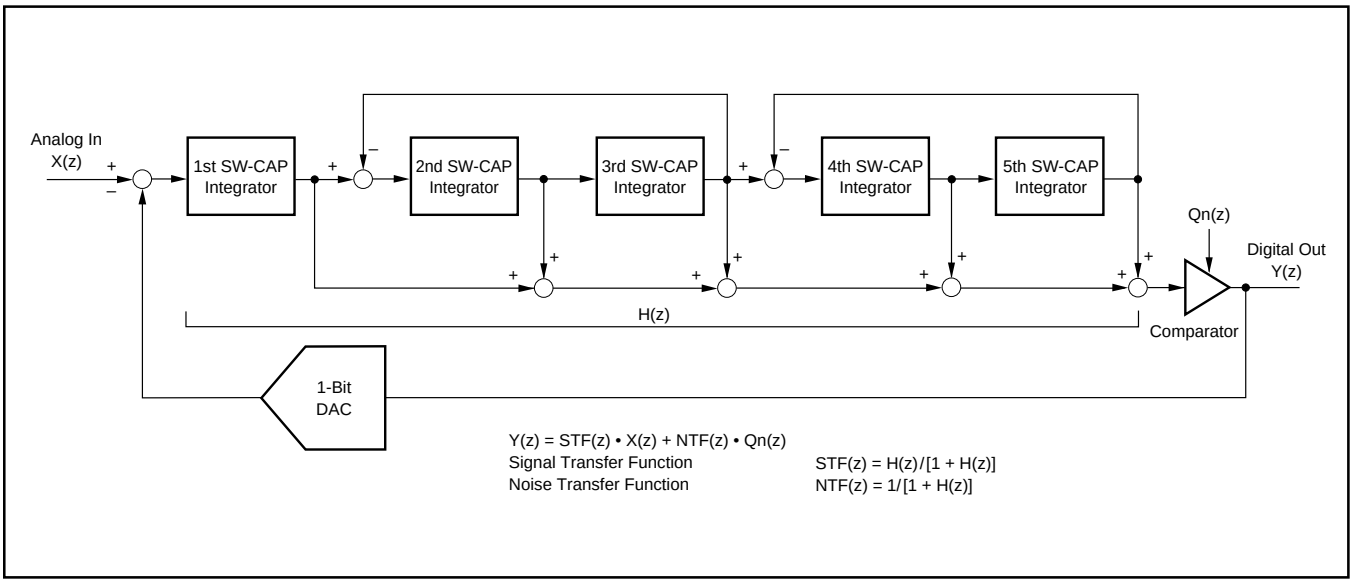


FIGURE 13. Simplified 5th-Order Delta-Sigma Modulator.

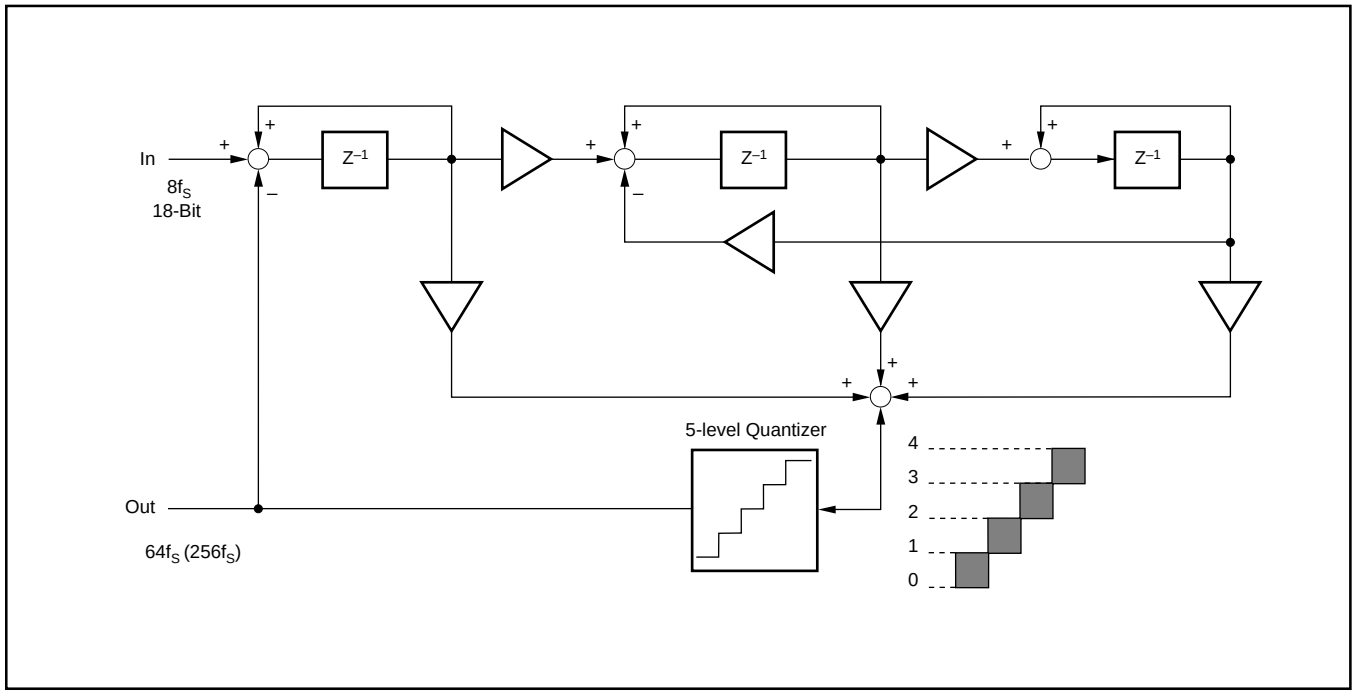


FIGURE 14. 5-Level Delta-Sigma Modulator Block Diagram.

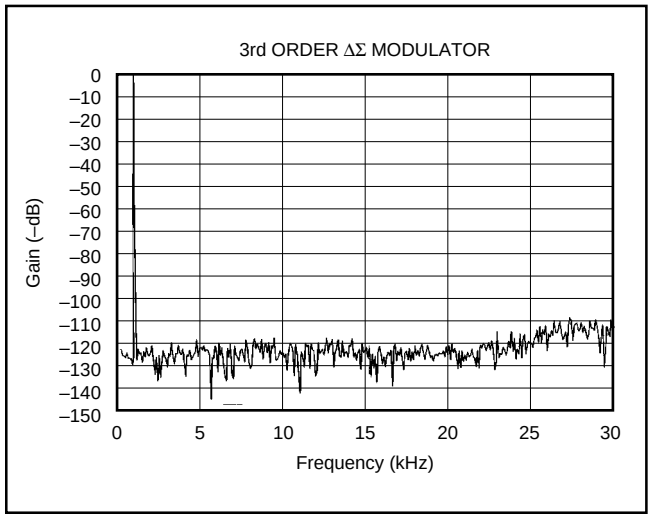


FIGURE 15. Quantization Noise Spectrum.

Multi Level
Delta Sigma