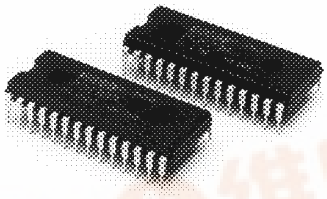
BURR-BROWN®



PCM78P

16-Bit Audio ANALOG-TO-DIGITAL CONVERTER

FEATURES

- LOW COST/HIGH PERFORMANCE 16-BIT AUDIO A/D CONVERTER
- FAST 5µs MAX CONVERSION TIME (4µs typ)
- VERY LOW THD+N (typ –88dB at FS; max –82dB)
- ±3V INPUT RANGE
- TWO SERIAL OUTPUT MODES PROVIDE VERSATILE INTERFACING
- COMPLETE WITH INTERNAL REFERENCE AND CLOCK IN 28-PIN PLASTIC DIP
- ±5V TO ±15V SUPPLY RANGE (600mW Power Dissipation)

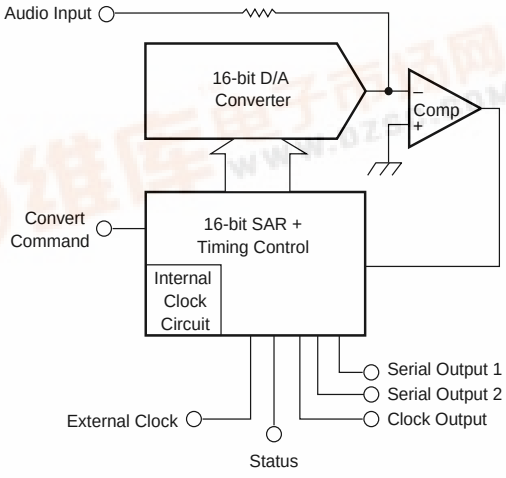
APPLICATIONS

- DSP DATA ACQUISITION
- TEST INSTRUMENTATION
- SAMPLING KEYBOARD SYNTHESIZERS
- DIGITAL AUDIO TAPE
- BROADCAST AUDIO PROCESSING
- TELECOMMUNICATIONS

DESCRIPTION

The PCM78P is a low-cost 16-bit analog-to-digital converter which is specifically designed and tested for dynamic applications. It features very fast, low distortion performance (4µs/–88dB THD+N typical) and is complete with internal clock and reference circuitry. The PCM78P is packaged in a reliable, low-cost 28-pin plastic DIP and data output is available in user-selectable serial output formats. The PCM78P is ideal for digital audio tape (DAT) recorders. Many similar applications such as digital signal processing and telecom applications are equally well served by the PCM78P.

The PCM78P uses a SAR technique. Analog and digital portions are efficiently partitioned into a high-speed, bipolar section and a low-power CMOS section. The PCM78P has been optimized for excellent dynamic performance and low cost.



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PDS-989A Printed in U.S.A. October, 1993

SPECIFICATIONS

ELECTRICAL

At T_C = +25°C, $+V_{DD}$ = +5V, and $\pm V_{CC}$ = ±12V, and one minute warm-up in convection environment, unless otherwise noted.

PARAMETER	CONDITIONS	PCM78P MIN	PCM78P TYP	PCM78P MAX	UNITS
RESOLUTION				16	Bits
INPUT/OUTPUT					
ANALOG INPUT					
Input Range		–3		+3	V
Input Impedance			1.5		kΩ
DIGITAL INPUT/OUTPUT					
Logic Family			TTL Compatible CMOS		
Logic Level: V_{IH}	I_{IH} = +40µA	+2		+5.5	V
V_{IL}	I_{IL} = –100µA	0		+0.8	V
V_{OH}	I_{OH} = 2TTL Loads	+2.4			V
V_{OL}	I_{OL} = 2TTL Loads			+0.4	V
Data Format			Serial BOB or BTC		
Convert Command			Negative Edge (1)		
Pulse Width		25	50		ns
CONVERSION TIME			4	5	µs
DYNAMIC CHARACTERISTICS					
SIGNAL-TO-NOISE RATIO (SNR)(2)	f_S = 200kHz/T_{CONV} = 4µs(3)				
f = 1kHz (0dB)	BW = 20kHz		90		dB(4)
f = 10kHz (0dB)	BW = 100kHz		80		dB
TOTAL HARMONIC DISTORTION(5)	f_S = 200kHz/T_{CONV} = 4µs				
f = 1kHz (0dB)	BW = 20kHz		–91		dB
f = 19kHz (0dB)	BW = 20kHz		–90		dB
f = 10kHz (0dB)	BW = 100kHz		–90		dB
f = 90kHz (0dB)	BW = 100kHz		–89		dB
TOTAL HARMONIC DISTORTION + NOISE(6)	f_S = 200kHz/T_{CONV} = 4µs				
f = 1kHz (0dB)	BW = 20kHz		–88	–82	dB
f = 1kHz (–20dB)	BW = 20kHz		–74	–68	dB
f = 1kHz (–60dB)	BW = 20kHz		–34		dB
f = 19kHz (0dB)	BW = 20kHz		–87		dB
f = 10kHz (0dB)	BW = 100kHz		–82		dB
f = 90kHz (0dB)	BW = 100kHz		–81		dB
TRANSFER CHARACTERISTICS					
ACCURACY					
Gain Error			±2		%
Bipolar Zero Error			±20		mV
Differential Linearity Error			±0.002		% of FSR(7)
Integral Linearity Error			±0.003		% of FSR
Missing Codes			None		14 Bits(8)
DRIFT					
Gain	0°C to +70°C		±25		ppm/°C
Bipolar Zero	0°C to +70°C		±4		ppm of FSR/°C
POWER SUPPLY SENSITIVITY					
$+V_{CC}$			±0.008		%FSR/%V_{CC}
$–V_{CC}$			±0.003		%FSR/%V_{CC}
$+V_{DD}$			±0.003		%FSR/%V_{DD}
POWER SUPPLY REQUIREMENTS					
Voltage Range: $+V_{CC}$		+4.75		+15.6	V
$–V_{CC}$		–4.75		–15.6	V
$+V_{DD}$		+4.75		+5.25	V
Current: $+V_{CC}$	$+V_{CC}$ = +12V		+15		mA
$–V_{CC}$	$–V_{CC}$ = –12V		–21		mA
$+V_{DD}$	$+V_{DD}$ = +5V		+7		mA
Power Dissipation	$\pm V_{CC}$ = ±12V		575		mW
TEMPERATURE RANGE					
Specification		0		+70	°C
Storage		–50		+100	°C
Operating		–25		+85	°C

NOTES: (1) When convert command is high, converter is in a halt/reset mode. Actual conversion begins on negative edge. See detailed text on timing for convert command description when using external clock. (2) Ratio of Noise rms/Signal rms. (3) f = input frequency; f_S = sample frequency (PCM78P and SHC702 in combination); BW = bandwidth of output (based on FFT or actual analog reconstruction using a 20kHz low-pass filter). (4) Referred to input signal level. (5) Ratio of Distortion rms/Signal rms. (6) Ratio of Distortion rms + Noise rms/Signal rms. (7) FSR: Full-Scale Range = 6Vp-p. (8) Typically no missing Codes at 14-bit resolution.

PIN ASSIGNMENTS

PIN	NAME	I/O	DESCRIPTION
1	Analog In	I	Analog Signal Input (1.5kΩ impedance).
2	$-V_{CC}$	I	Analog power supply (–5V to –15V).
3	MSB Adjust	I	Internal adjustment point to allow adjustment of MSB major carry.
4	$+V_{DD}$	I	Power connection for comparator (+5V).
5	No Connection	—	No internal connection.
6	Comparator Common	I	Comparator common connection. Connect to ground.
7	$\overline{MSB}$	O	Parallel output of bit 1 (MSB) inverted.
8	BTC/BOB Select	I	Two's complement (open) or straight binary (grounded) data output format selection.
9	Status	O	Output signal held high until conversion is complete.
10	Clock Out	O	Internal clock output generated from RC network on pins 11 and 12 (also present when external clock is used lagging external clock by ~24ns and same duty cycle).
11	R_1C_1	I	RC connection point used to generate internal clock. Sets clock high time. See text for details.
12	R_2C_2	I	RC connection point used to generate internal clock. Sets clock low time. See text for details.
13	S_{OUT2}	O	Internal shift register containing the previous conversion result. (Alternate latched data output mode).
14	$+V_{DD}$	I	Power connection for +5V logic supply.
15	S_{OUT1}	O	Primary real-time data output synchronized to clock out.
16	External Clock	I	External clock input point (internal clock must be disabled).
17	Int/Ext Clock Select	I	Selects either internal or external clock mode (low = internal; open = external).
18	Short Cycle	I	Terminates conversion at less than 16 bits (open for 16-bit mode). See text for details.
19	Convert Command	I	Starts conversion process (can optionally be generated internally).
20	S_{OUT2} Latch	I	Latches previous conversion result for readout (must be issued with the S_{OUT2} clock to initiate latch and an internal convert command).
21	S_{OUT2} Clock	I	Used to read out internally latched data from previous conversion.
22	Digital Common	I	Digital grounding pin.
23	$+V_{CC}$	I	Analog supply connection (+5V to +15V).
24	V_{POT}	O	Voltage output (~2.5V) for optional adjustment of MSB transition.
25	Reference Decouple	I	Reference decoupling point.
26	Analog Common	I	Analog grounding pin.
27	Reference Out	O	2V reference out. Should not be used except as shown in connection diagram.
28	Speed Up	I	Connection point for a capacitor to speed reference settling. See text for details.

NOTE: Analog and digital commons are connected internally.

INPUT/OUTPUT RELATIONSHIPS

ANALOG INPUT	CONDITION	DIGITAL OUTPUT	
		BTC	BOB
+2.999908V	+ Full Scale	7FFF Hex	FFFF Hex
–3.000000V	–Full Scale	8000 Hex	0000 Hex
0.000000V	Bipolar Zero	0000 Hex	8000 Hex
–0.000092V	Zero-1 LSB	FFFF Hex	7FFF Hex

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
PCM78P	28-Pin Plastic DIP	215

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

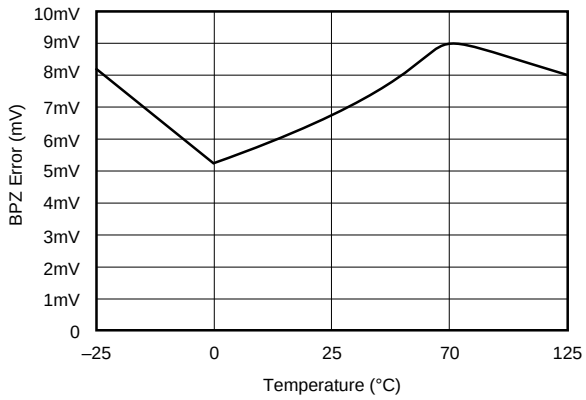
$+V_{CC}$ to Analog Common	0 to +16.5V
$-V_{CC}$ to Analog Common	0 to –16.5V
$-V_{DD}$ to Analog Common	0 to +7V
Analog Common to Digital Common	±0.5V
Logic Inputs to Digital Common	–0.3V to V_{DD} + 0.5V
Analog Inputs to Analog Common	±16.5V
Lead Temperature (soldering, 10s)	+300°C

Stresses above these ratings may permanently damage the device.

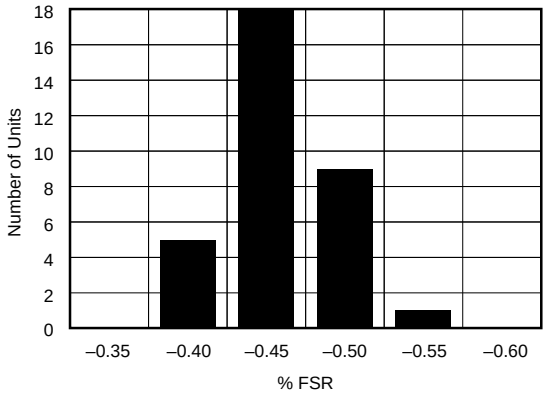
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V_{CC} = ±15V, unless otherwise noted.

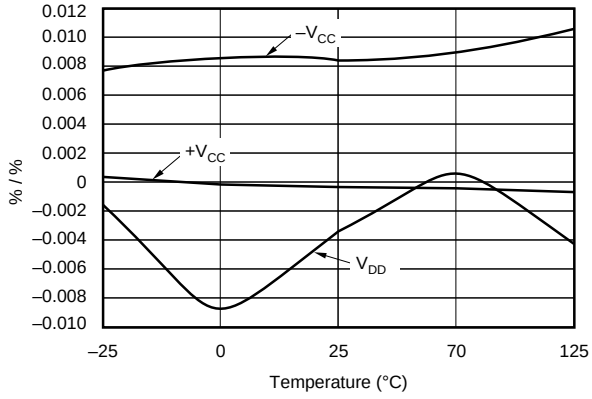
BPZ ERROR vs TEMPERATURE



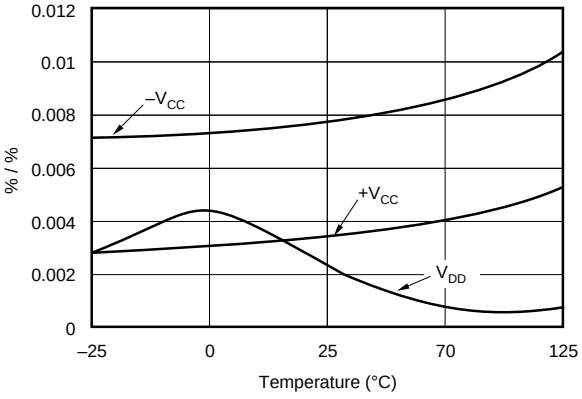
BIPOLAR GAIN ERROR as % FSR
25°C; N = 33 UNITS



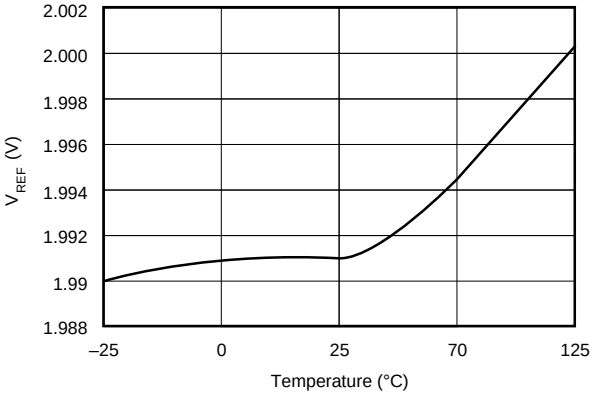
PSRR at +FS INPUT



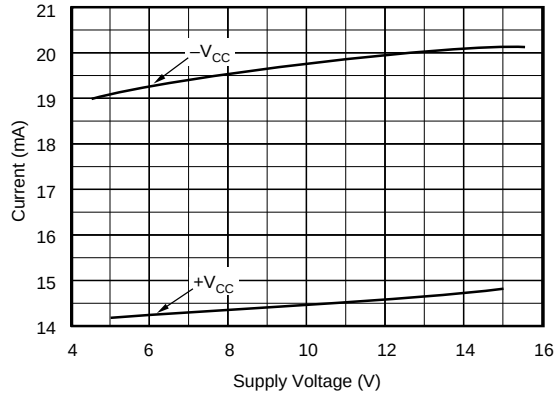
PSRR at –FS INPUT



V_{REF} vs TEMP



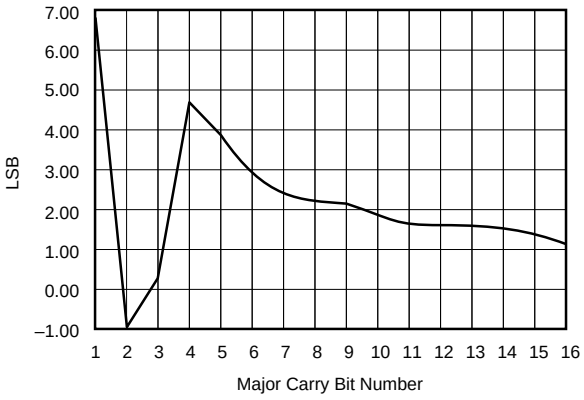
I_{SS} vs SUPPLY VOLTAGE



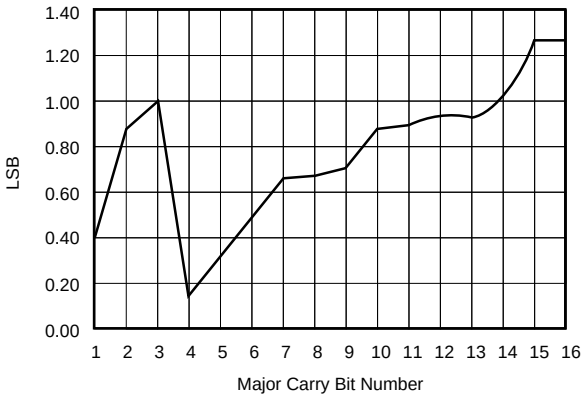
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_{CC} = ±15V, unless otherwise noted.

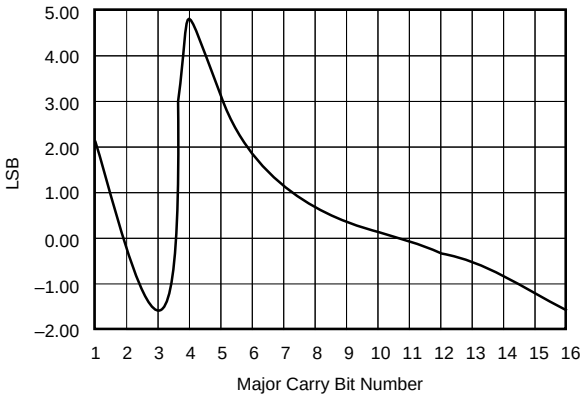
INTEGRAL NONLINEARITY
at –25°C



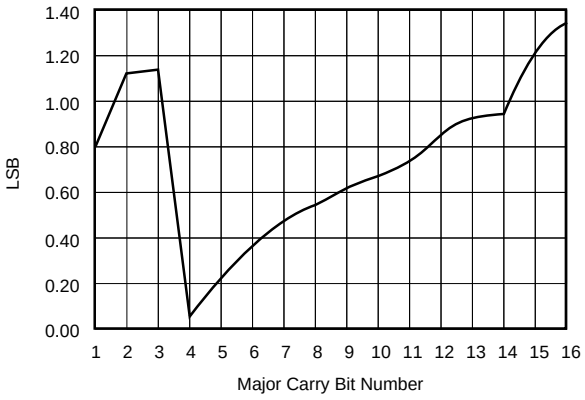
DIFFERENTIAL NONLINEARITY
at –25°C



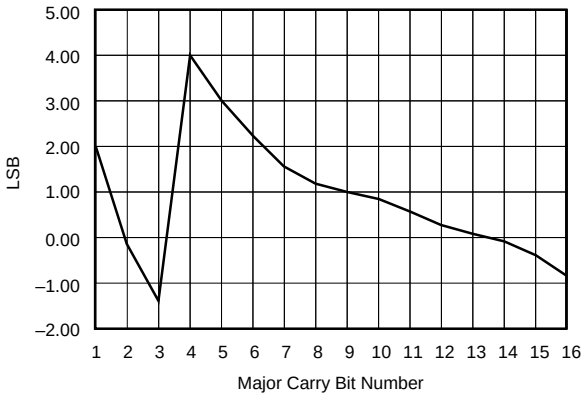
INTEGRAL NONLINEARITY
at 0°C



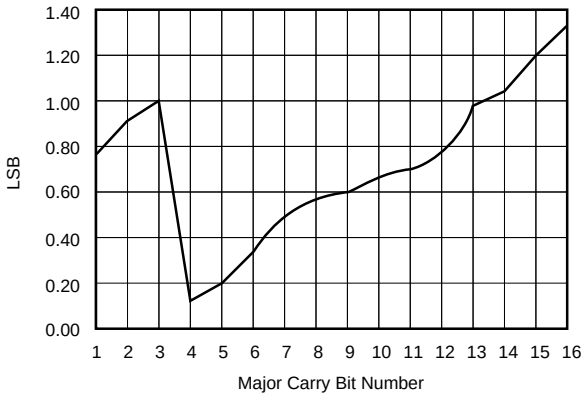
DIFFERENTIAL NONLINEARITY
at 0°C



INTEGRAL NONLINEARITY
at 25°C



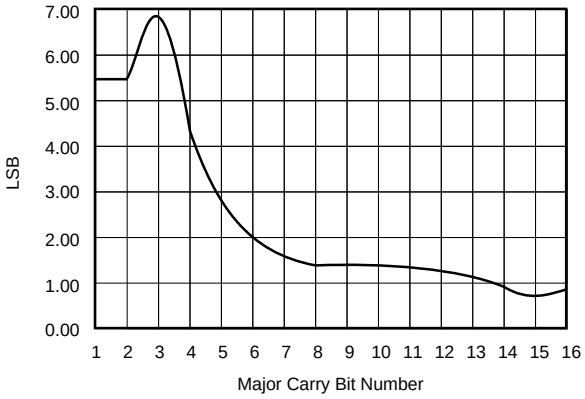
DIFFERENTIAL NONLINEARITY
at 25°C



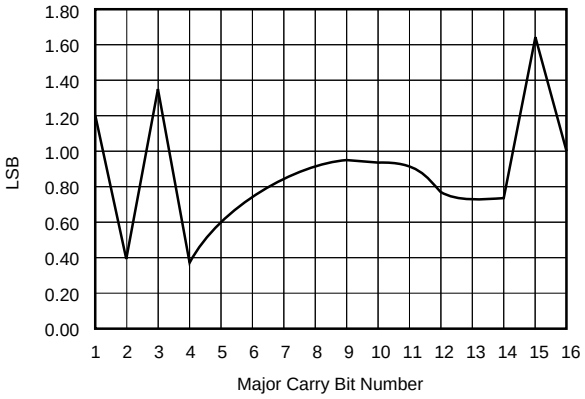
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_{CC} = ±15V, unless otherwise noted. Histograms done with conversion time = 8µs.

INTEGRAL NONLINEARITY
at 70°C



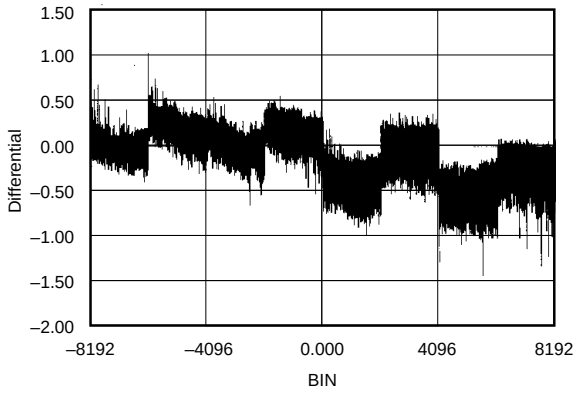
DIFFERENTIAL NONLINEARITY
at 70°C



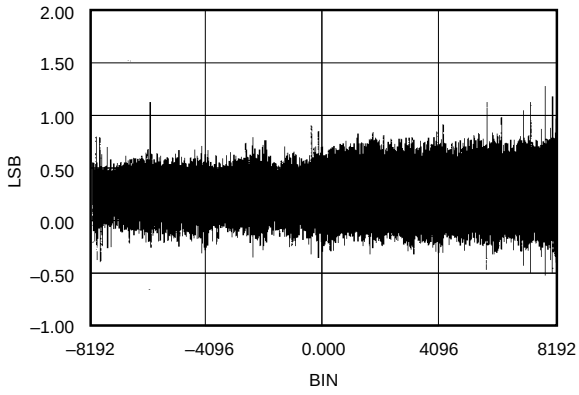
INTEGRAL NONLINEARITY
at 125°C

DIFFERENTIAL NONLINEARITY
at 125°C

INTEGRAL NONLINEARITY ERROR
(to 14-Bit LSB)



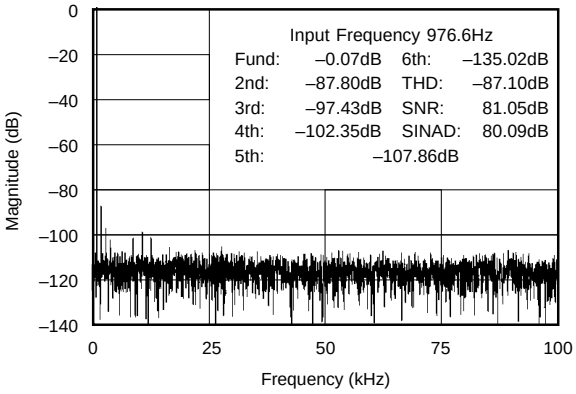
DIFFERENTIAL NONLINEARITY ERROR
(to 14-Bit LSB)



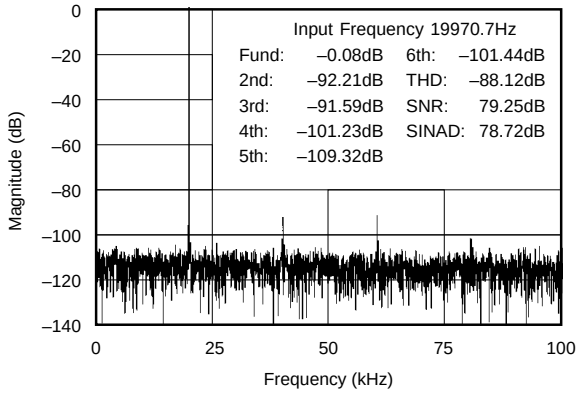
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_{CC} = ±15V, unless otherwise noted. Histograms done with Conversion Time = 8µs.

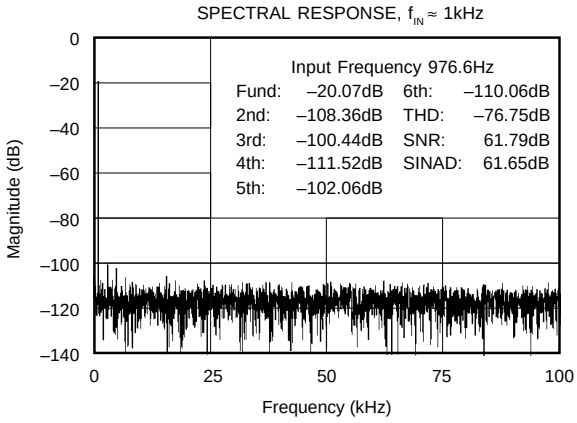
SPECTRAL RESPONSE, f_{IN} ≈ 1kHz



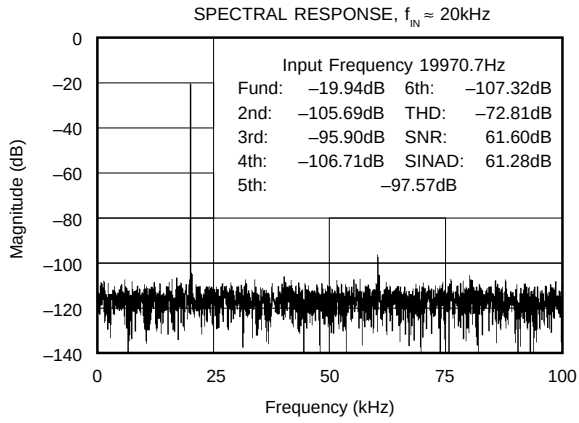
SPECTRAL RESPONSE, f_{IN} ≈ 20kHz



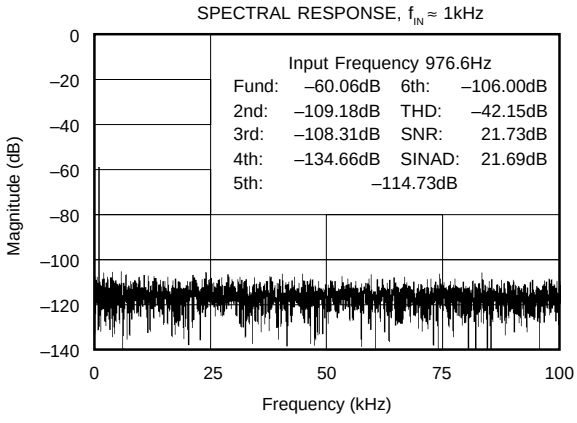
SPECTRAL RESPONSE, f_{IN} ≈ 1kHz



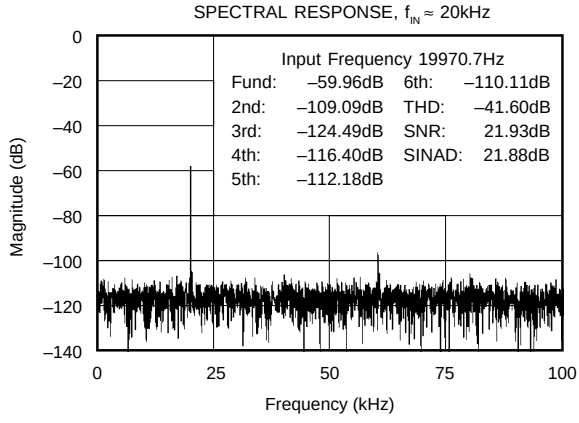
SPECTRAL RESPONSE, f_{IN} ≈ 20kHz



SPECTRAL RESPONSE, f_{IN} ≈ 1kHz

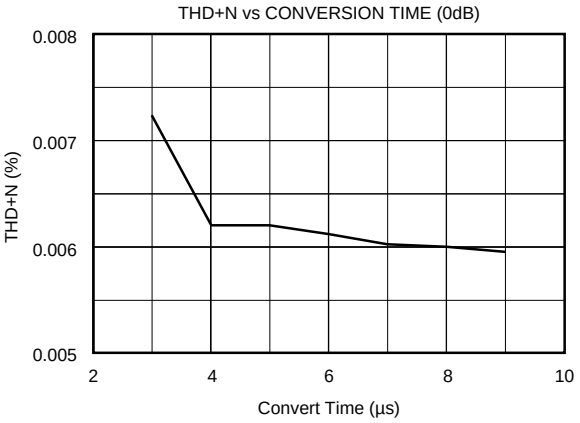


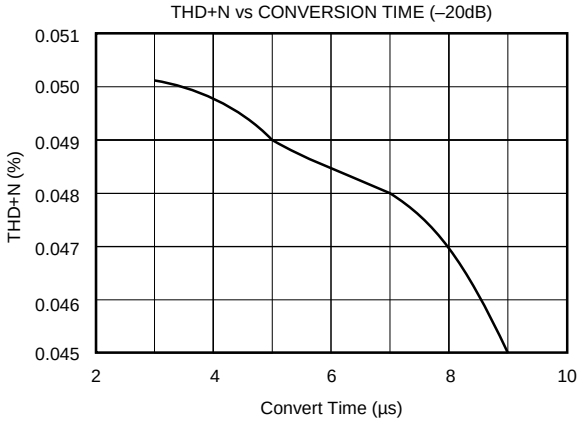
SPECTRAL RESPONSE, f_{IN} ≈ 20kHz

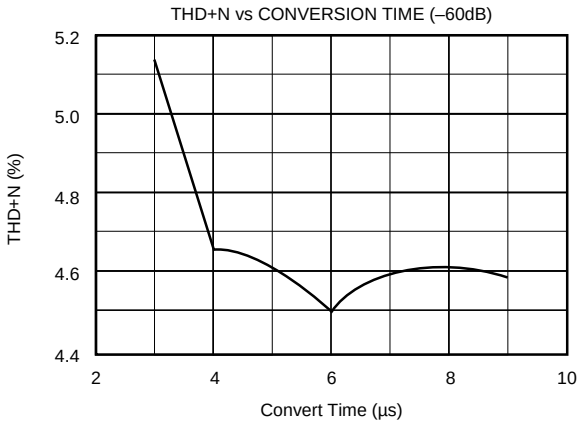


TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_{CC} = ±15V, unless otherwise noted.







THEORY OF OPERATION

The PCM78P is a successive approximation A/D converter; this type of converter is well suited to high speed and resolution. The accuracy of a successive approximation converter is described by the transfer function shown in Figure 1. All successive-approximation A/D converters have an inherent quantization error of ±1/2LSB. The remaining errors in the A/D converter are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, power supply rejection, and reference errors. In summary, these errors consist of initial errors including Gain, Offset, Linearity, Differential Linearity, and Power Supply Sensitivity. Gain drift over temperature rotates the line (Figure 1) about zero, and Offset drift shifts the line left or right over the operating temperature range. Total Harmonic Distortion + Noise (THD+N) is a measure of the magnitude and distribution of the Linearity Error, Differential Linearity Error, and Noise, as well as quantization errors. The THD+N specification is most useful in audio or dynamic signal processing applications. To be useful, THD+N should be specified for both high level and low level input signals. This error is unadjustable and is the most meaningful indicator of A/D converter accuracy for dynamic applications.

DYNAMIC RANGE

Dynamic range is a measure of the ratio of the smallest signals the converter can resolve to the full scale range and is usually expressed in decibels. The theoretical dynamic range of a converter is approximately 6 x *n*, where *n* is the number of bits of resolution. A 16-bit converter would thus have a theoretical dynamic range of 96dB. The actual useful dynamic range is limited by noise and linearity errors and is therefore somewhat less than the theoretical limit.

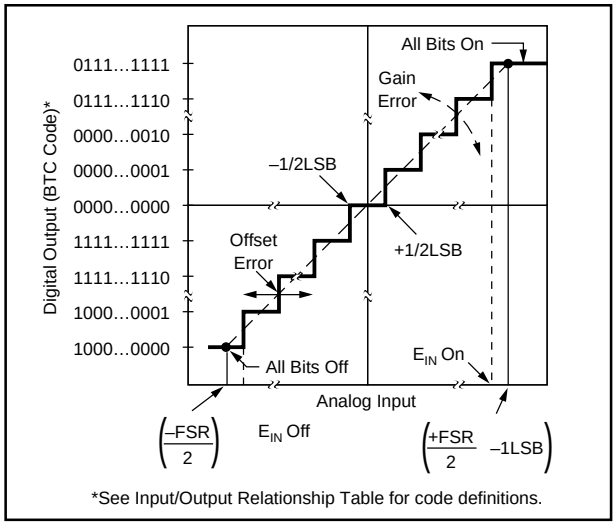


FIGURE 1. Input vs Output for Ideal Bipolar A/D Converter.

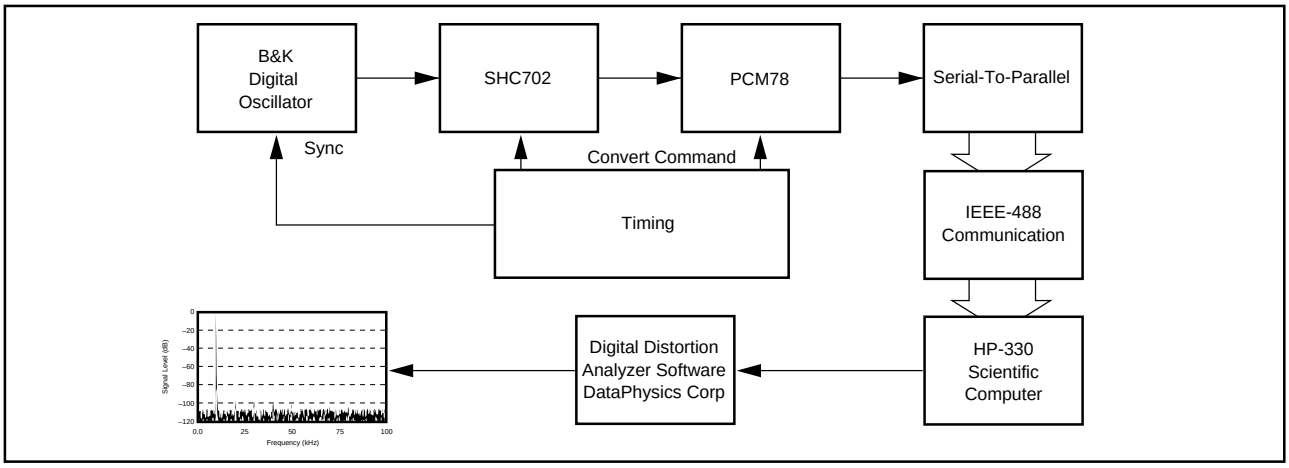


FIGURE 2. Block Diagram of Distortion Test Circuit.

DISCUSSION OF SPECIFICATIONS

TOTAL HARMONIC DISTORTION

Evaluating distortion specifications can be a difficult task, as distortion is often specified in different ways. Total Harmonic Distortion (THD) is defined as the ratio of the square root sum of the squares of the value of rms harmonics to the value of the rms fundamental and is expressed in percent or dB. Note that this measurement only includes energy present in those frequencies which would contain harmonics, and therefore is less than Total Harmonic Distortion plus Noise.

The Total Harmonic Distortion plus Noise (THD+N) is defined as the ratio of the square root of the sum of the squares of the value of the rms harmonics and rms noise to the value of the rms fundamental and is expressed in percent or dB. This is the most meaningful measurement of a dynamic converter's performance because it includes all energy present in the signal that is not fundamental. A block diagram of the test circuit used to measure the THD and THD+N of the PCM78 is shown in Figure 2. This digital system is capable of differentiating harmonic energy and noise; conventional distortion analyzers which operate on a tracking notch filter principle cannot distinguish this energy, and therefore only measure THD+N. Unfortunately, in the past, these systems were used for measuring distortion performance of converters, and the distortion was often simply specified as "THD", when in fact it was really THD+N. For this reason, it is often confusing to compare specifications of converters unless one knows exactly what was being measured.

If we assume that the error due to the test circuit of Figure 2 is negligible, then the rms value of the PCM78 error referred to the input can be shown to be

$$\text{THD+N} = \frac{\sqrt{\frac{1}{N}\sum_{i=1}^{N}\left[E_L(i) + E_Q(i) + E_N(i)\right]^2}}{E_{rms}} \text{ X } 100\%$$

where N is the number of samples, $E_L(i)$ is the linearity error at each sample, $E_Q(i)$ is the quantization error at each

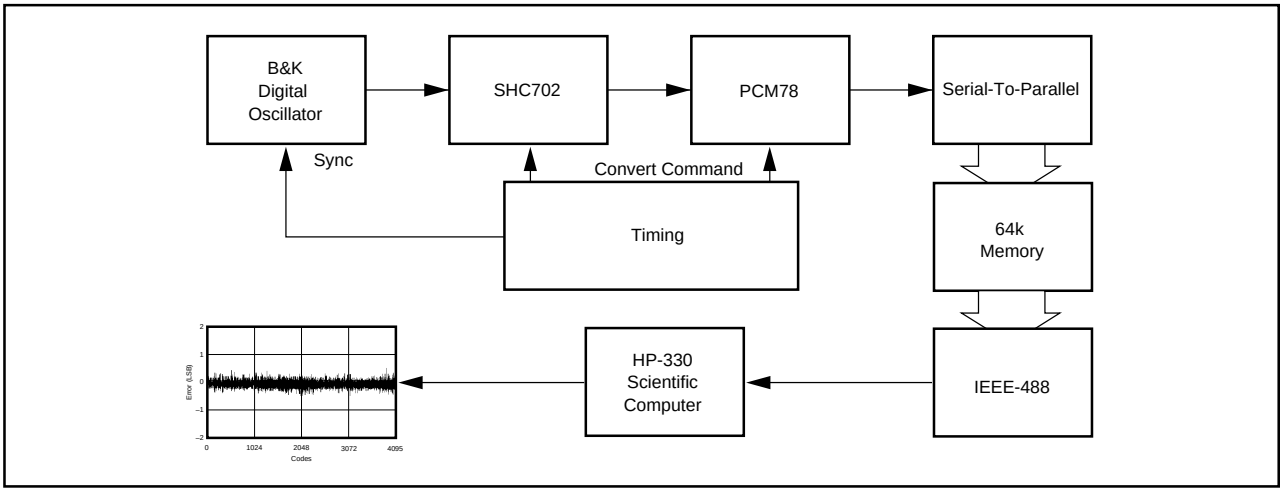


FIGURE 3. Block Diagram of Histogram Test.

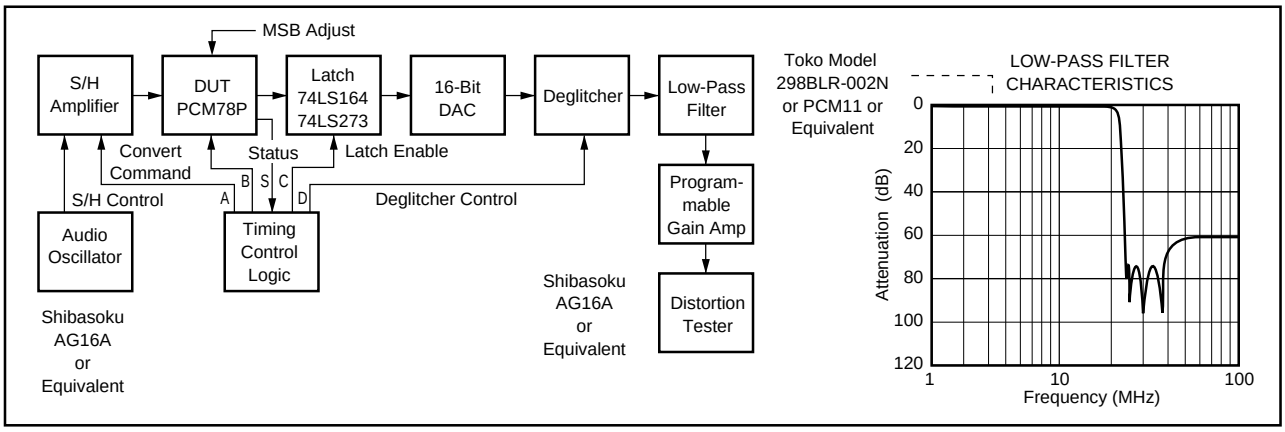


FIGURE 4. Production Distortion + Noise Test System Block Diagram.

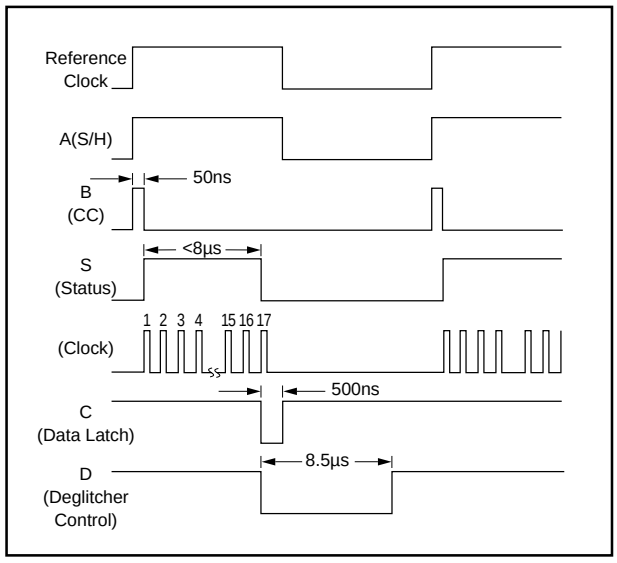


FIGURE 5. Timing Diagram for Figure 4.

sample, and $E_N(i)$ is the residual noise energy present at each sample. Similarly, THD alone can be expressed as

$$THD = \frac{\sqrt{\frac{1}{N}\sum_{i=1}^{N}\left[E_L(i)\right]^2}}{E_{rms}} X\ 100\%$$

These expressions indicate that there is a correlation between THD+N and the square root of the sum of the squares of the linearity errors at each digital word of interest. In order to find this error at each code, a histogram test must be performed on the PCM78, as illustrated in Figure 3. The histogram for every converter is unique, as the linearity errors from converter to converter will vary in their placement along the transfer function. Typical histogram data is shown in the Typical Curves.

However, this expression for THD+N does not mean that the worst case linearity error of the A/D is directly correlated to the THD+N because the digital output words from theA/D vary according to the amplitude and frequency of the sine wave input as well as the sampling frequency.

For the PCM78 the test sampling frequency was chosen to be 200kHz, near the PCM78's fastest rate of conversion. The test frequencies used vary within the audio range, and are stepped in amplitude from 0dB, to –20dB, to –60dB.

In manufacturing the PCM78, the test system shown in Figure 4 is used to test for guaranteed THD+N.

ACCURACY VS CONVERSION TIME AND INPUT SIGNAL LEVEL

The relationship of THD vs input signal level and THD vs conversion time is shown is the typical curves. Slowing the conversion time to more than 8µs results in little added benefit in terms of THD+N.

For applications which are not as concerned with dynamic performance but require DC accuracy and linearity, it is best to use the PCM78 at the longest conversion time possible for the system requirements. Slowing the PCM78 to 8µs-10µs conversion time results in a substantial improvement in linearity. The typical curves show DNL and INL plots for a typical device, at an 8µs conversion time. Due to the segmented architecture of the internal DAC used in the successive approximation conversion technique, significant differential linearity errors occur near bits 3 and 4. Allowing more settling time for the DAC (by slowing the conversion speed) will improve this differential linearity error and give equivalent performance to more costly DC-specified 12-bit to 14-bit A/D converters.

SYSTEM DESIGN CONSIDERATIONS

DIGITAL CIRCUIT CONNECTIONS

The PCM78 comes complete with an internal clock circuit, or it may be clocked by an external clock. Choosing which mode to operate with depends upon the application for which the PCM78 will be used. In an application where the sample rate may not be fixed (transient recording, etc.), using the internal clock set to give a very fast conversion may be the best solution. In systems where the sample rate is fixed, an external clock is probably the better choice since it will allow the digital system design to be synchronous.

In either case, the PCM78 requires 17 clock cycles to complete a conversion. To calculate the clock frequency necessary for a given conversion time, the following equation may be used:

$$f_{CLOCK} = \frac{17}{\text{Conversion Time}}$$

The internal clock operates only during a conversion, and is gated on by the falling edge of the convert command. See Figure 6. The internal clock is available on pin 10, Clock Out. The high and low time of this clock is set by R_1C_1 and R_2C_2 respectively. The duty cycle of the clock should be between 20% to 80%, and may be set to 50% for simplicity.

$$\text{Clock High Time (in ns)} = 1.32R_1C_1$$

$$\text{Clock Low Time (in ns)} = 1.32R_2C_2$$

$$\text{R in k}\Omega\text{; C in pF.}$$

These equations are approximate (±5%); they should be used for determining an initial part value which will then need to be "tweaked" for accurate timing. If highly accurate time bases are required, use of an external clock is recommended.

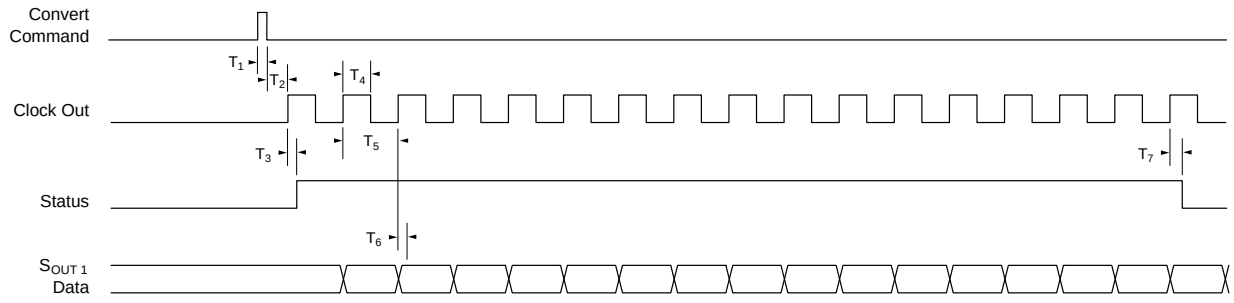
The external clock is applied at pin 16, and the Int/Ext Clock select (pin 17) should be left open (an internal pull-up resistor assures that the logical state of an open pin is "1"). Using the external clock requires careful placement in time of the convert command. Figure 7 diagrams the recommended timing with an external clock. A simple circuit which assures the proper timing of the convert command is shown in Figure 8.

Due to the design of the Clock/Logic chip in the PCM78, a conversion is begun inside the PCM78 by an asynchronous state machine. This places stringent requirements on the timing of the convert command, as improper timing can cause metastable states within this state machine. Using the circuitry shown in Figure 8, the user is assured of consistent operation, and these invalid states within the state machine are entirely avoided. (Note that this is not a consideration when using an internal clock, as nothing is being clocked when a convert command is presented to the PCM78).

The Clock Out function is a gated form of the external clock, i.e. the 17 clock cycles used in the conversion are present on this pin during conversion. This allows use of a continuous external clock, with Clock Out being the clock that the converter is actually using for conversion. Note that this is simply a delayed (~24ns) version of the external clock, and will have the same frequency and duty cycle.

The S_{OUT2} Latch enables the user to latch data from the previous conversion and read it out at a higher speed than the convert clock. This feature allows the converter to easily interface to digital filtering necessary for oversampling. See Figure 9 for timing information in this mode.

In this mode, the PCM78 generates its own internal convert command when the S_{OUT2} Clock goes high within ±50ns of S_{OUT2} Latch going low; the external convert command may not be used, and pin 19 must be grounded. The timing diagram shows the recommended timing for using this mode. After the S_{OUT2} Latch control signal goes low, data from the SAR is loaded into the S_{OUT2} latch on the next rising edge of the S_{OUT2} Clock. This clock edge should occur prior to the next rising edge of the conversion clock (internal or external), since the SAR will reset itself prior to the latching

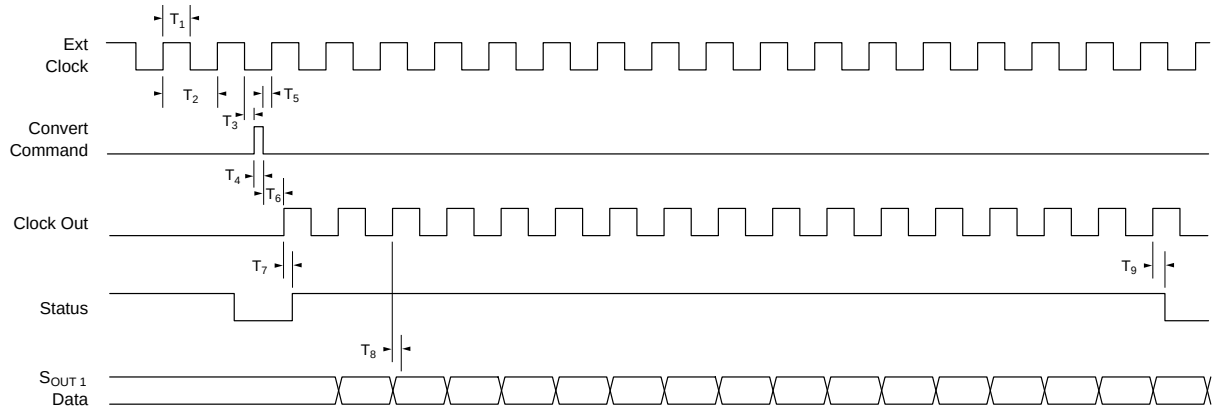


T_A = +25°C, V_{DD} = +5V, guaranteed by sample testing; these parameters are not 100% tested in production.

TIME	DESCRIPTION	TIME (ns) MIN	TYP	MAX
T_1	CONVERT COMMAND pulse width	25	50	(1)
T_2	Delay from falling edge of CONVERT COMMAND to rising edge of CLOCK OUT	60	70	85
T_3	Delay from rising edge of CLOCK OUT to rising edge of STATUS	8	10	30
T_4	INTERNAL CLOCK pulse width	50	125	450
T_5	INTERNAL CLOCK period	140	290	500
T_6	Delay from rising edge of CLOCK OUT to bit data valid	17	20	50
T_7	Delay from rising edge of 17th clock pulse to falling edge of STATUS	10	15	30

NOTE: (1) When using the internal clock, the clock does not operate until the Convert Command is low. It is therefore possible to keep the convert command high indefinitely, thereby keeping the PCM78 in a halt mode. The conversion cycle begins on the falling edge of convert command, and convert command must remain low during the entire conversion cycle in order to make the PCM78 operate properly.

FIGURE 6. Conversion Timing when using Internal Clock.



T_A = +25°C, V_{DD} = +5V, guaranteed by sample testing; these parameters are not 100% tested in production.

TIME	DESCRIPTION	TIME (ns) MIN	TYP	MAX
T_1	EXTERNAL CLOCK pulse width	50	125	(1)
T_2	EXTERNAL CLOCK period	140	290	(1)
T_3	Delay from falling edge of EXTERNAL CLOCK to rising edge of CONVERT COMMAND	–30	0	420
T_4	CONVERT COMMAND pulse width	10	50	200
T_5	Delay from falling edge of CONVERT COMMAND to rising edge of EXTERNAL CLOCK	20	50	430
T_6	Delay from falling edge of CONVERT COMMAND to rising edge of CLOCK OUT	40	75	460
T_7	Delay from rising edge of CLOCK OUT to rising edge of STATUS	6	10	30
T_8	Delay from rising edge of CLOCK OUT to bit data valid	15	17	20
T_9	Delay from rising edge of 17th clock pulse to falling edge of STATUS	8	10	30

NOTE: (1) The PCM78 does not contain dynamic digital circuitry, and can be clocked as slowly as the user wishes. In typical applications, the longest clock period may be as long as 1µs.

FIGURE 7. Conversion Timing when using External Clock.

if the convert clock rises before the S_{OUT2} Clock. This condition is avoided as long as the frequency of S_{OUT2} Clock is at least 1.5 times that of the conversion clock.

The internal convert command is generated upon S_{OUT2} Latch going low, and its falling edge occurs upon the first falling edge of S_{OUT2} Clock after S_{OUT2} Latch goes low. S_{OUT2} Latch should remain low for at least 2 cycles of S_{OUT2} Clock to insure proper latching. In many applications, the S_{OUT2} Latch can be the $2f_S$ signal present in many digital audio systems, typically known as WDCK. Figure 10 includes an example of this application.

The data read out on S_{OUT2} is from the conversion previously performed, while the data that is present on S_{OUT1} is the real time readout of the successive approximation as it occurs.

SHORT CYCLE

The PCM78 has the ability to be short cycled to a resolution less than 16 bits. This is accomplished by driving the Short Cycle pin (pin 18) low when the conversion is to be terminated, and holding it low until the next convert command is given. The circuit in Figure 11 will accomplish this function.

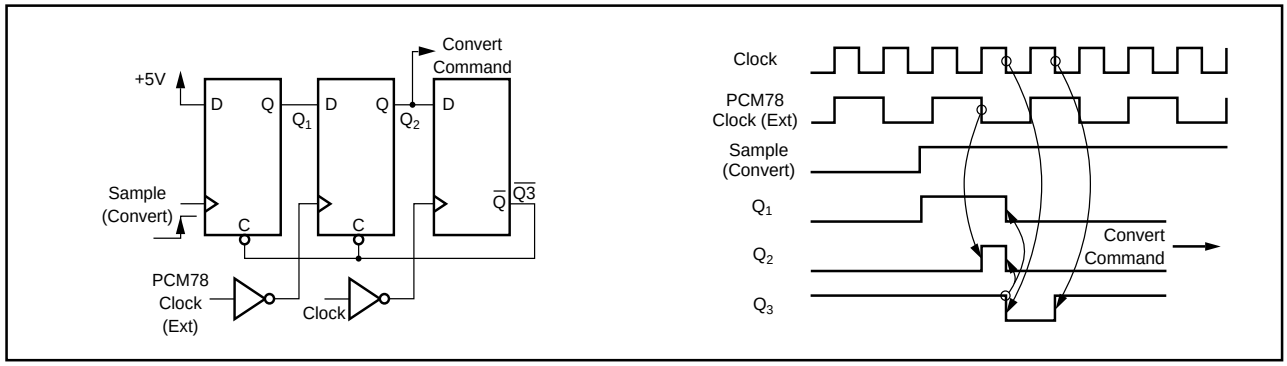
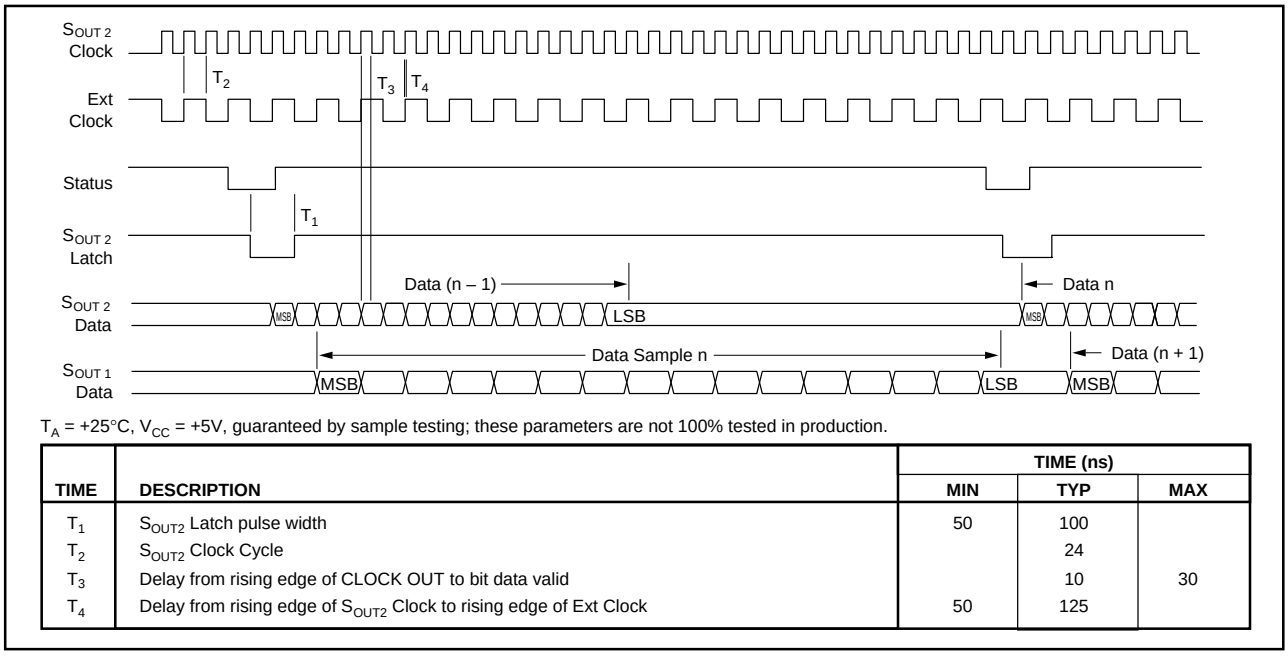


FIGURE 8. Convert Command Timing Circuit for Use with External Clock.



T_A = +25°C, V_{CC} = +5V, guaranteed by sample testing; these parameters are not 100% tested in production.

TIME	DESCRIPTION	TIME (ns) MIN	TYP	MAX
T_1	S_{OUT2} Latch pulse width	50	100	
T_2	S_{OUT2} Clock Cycle		24	
T_3	Delay from rising edge of CLOCK OUT to bit data valid		10	30
T_4	Delay from rising edge of S_{OUT2} Clock to rising edge of Ext Clock	50	125	

FIGURE 9. Timing when using S_{OUT2} Latch.

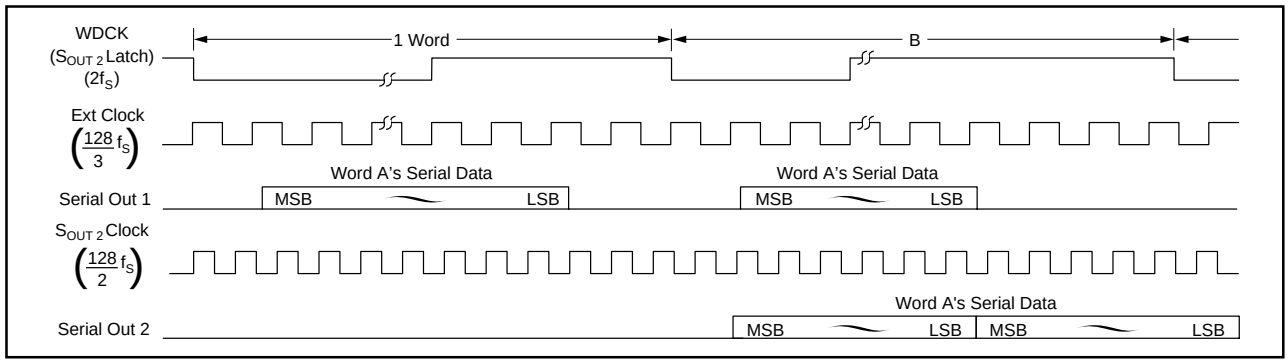
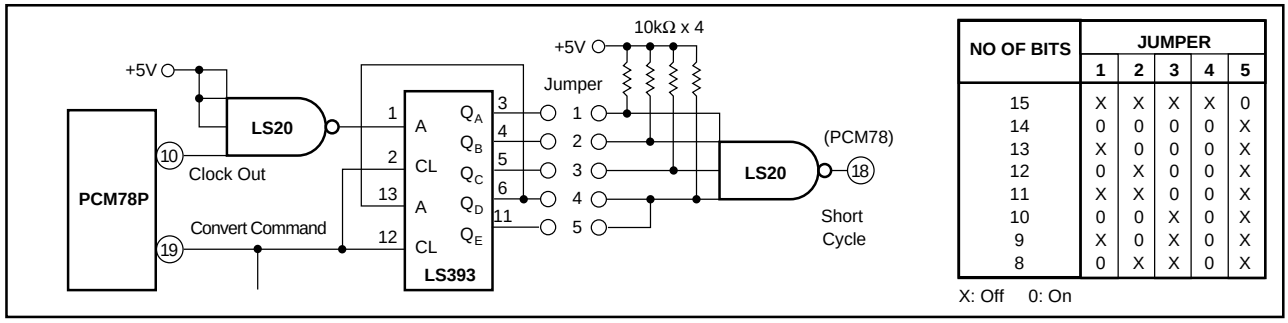


FIGURE 10. Application Example of $S_{OUT 2}$ Operation.



NO OF BITS	JUMPER 1	2	3	4	5
15	X	X	X	X	0
14	0	0	0	0	X
13	X	0	0	0	X
12	0	X	0	0	X
11	X	X	0	0	X
10	0	0	X	0	X
9	X	0	X	0	X
8	0	X	X	0	X

X: Off 0: On

FIGURE 11 . Short Cycle Circuit.

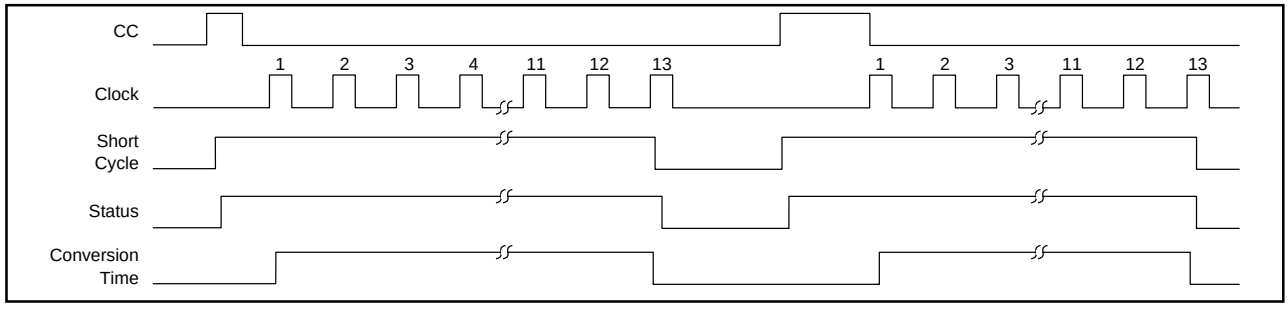


FIGURE 12. Short Cycle Operation Timing.

If Short Cycle is not held low until the next convert command is issued, the Status line will go high in synchronization with Short Cycle. This is because the operation of the Status line becomes invalid after Short Cycle is asserted. An example of the Short Cycle operation is shown in Figure 12.

In those systems where a user may not be using a continuous external clock, it is necessary to assure that a falling edge of external clock occurs after short cycle goes low. This is because conversion actually stops on the first falling edge of external clock after Short Cycle goes low.

ANALOG CIRCUIT CONSIDERATIONS

Layout Precautions

Analog and Digital Common are connected internally in the PCM78, and should be connected together as close to the unit as possible, preferably to a large ground plane under the ADC. Low impedance analog and digital common returns are essential for low noise performance. Coupling between analog inputs and digital lines should be minimized by careful layout. The input pin (pin 1) and the MSB adjust pin (pin 3) are both extremely sensitive to noise; digital lines should be kept away from these pins to avoid coupling digital noise into the sensitive analog circuitry.

Contact factory for a recommended PCB layout for the PCM78.

Power Supply Decoupling

The power supplies should be bypassed with tantalum or electrolytic capacitors as shown in Figure 13 to obtain noise free operation. These capacitors should be located as close to the ADC as possible. Bypass the 1µF electrolytic capacitors with 0.01µF ceramic or polystyrene capacitors for improved high frequency performance.

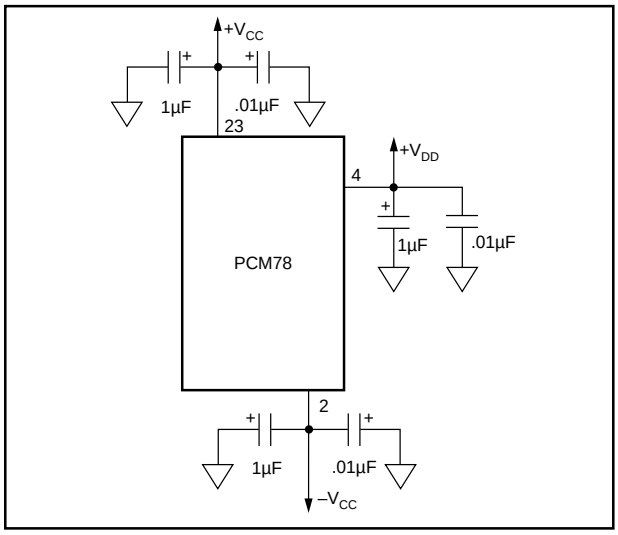


FIGURE 13. Recommended Power Supply Decoupling.

Reference Decoupling and Speed Up

In order to assure the lowest noise operation of the PCM78, the reference may be bypassed by three different capacitors. Pin 25 is a decoupling point for the reference to $-V_{CC}$. The decoupling capacitor should range from 0.1µF to 4.7µF; larger values can cause reference settling problems which may manifest themselves as missing codes. This capacitor should be as close to the PCM78 as possible, to minimize the potential for coupling noise into the device; with a good board layout it may be best to leave this capacitor out of the circuit altogether, as the extra lead length may only cause more noise in the reference.

Pin 27 is a decoupling point to ground, as well as the output of the 2V reference. This point should not be used to supply reference voltage to external circuitry unless it is buffered. A 2.2µF capacitor is recommended, and the capacitor used here should not exceed 4.7µF.

Pin 28, the Speed Up pin, allows a capacitor to be connected to ground to facilitate reference settling. This does not speed up the conversion time, but it does reduce odd order harmonic distortion. As with the decoupling capacitor on pin 25, this may also contribute to noise; if harmonic content is most important in an application, this capacitor (0.1µF - 10µF) should be connected. In all other cases, it is best to leave the capacitor out of the circuit.

Input Scaling

The analog input should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. The DAC inside the PCM78 has a ±2mA range, and the nominal ±3V input is scaled by a 1.5kΩ resistor. In order to scale to other ranges, see Table I for recommended scaling resistor values, connected as shown in Figure 14.

INPUT RANGE	R
±10V	8.2kΩ
±5V	3.3kΩ
NOTE: R values shown assume use of 1k trim pot to adjust for scale accuracy.	

TABLE I. PCM78 Input Scaling Resistor Values.

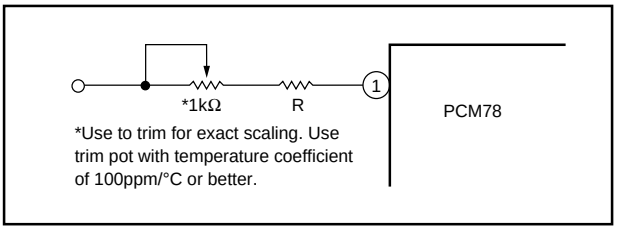


FIGURE 14. PCM78 Input Scaling Circuit.

INPUT IMPEDANCE

The input signal to the PCM78 should come from a low impedance source, such as the output of an op amp, to avoid any errors due to the dynamic input impedance that a successive-approximation converter presents to the outside world because of the changing currents in this circuit during conversion as the converter steps through its approximations.

If the driving circuit output impedance is not low, a buffer amplifier should be added between the input signal and the direct input to the PCM78 as shown in Figure 15.

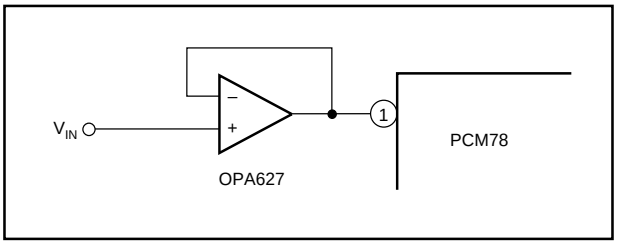


FIGURE 15. Buffer Amplifier for PCM78 Input.

MSB Adjustment

Differential Linearity errors at bipolar zero and THD are guaranteed to meet data sheet specifications without any external adjustment. However, a provision has been made for an optional adjustment of the MSB linearity point which makes it possible to eliminate DLE error at BPZ. This is important when the signal level is very low, because zero crossing noise (DLE at BPZ) becomes very significant when compared to the small codes changes occurring in the LSB portion of the converter.

The PCM78 is laser trimmed for best performance at the factory without the MSB adjust circuitry installed; if better performance can be obtained it would be by the addition of the MSB adjust circuitry shown in Figure 16.

The best method of adjusting the MSB is by using a real time FFT routine to monitor the levels of odd order harmonics when a sine-wave is being digitized by the PCM78. Adjusting the potentiometer in Figure 16 will allow the user to reduce the magnitude of odd-order harmonics.

An alternate method is to reconstruct the data out of the PCM78 through a DAC, and measure THD+N on a conventional distortion analyzer. Adjust the potentiometer for minimum THD+N.

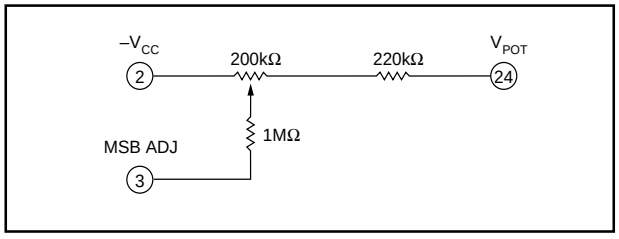


FIGURE 16. MSB Adjust Circuit.

APPLICATIONS INFORMATION

A typical digitization circuit, used on the demonstration board available for the PCM78, is shown in Figure 20. The connections and part values shown in this circuit have been optimized for the best THD+N performance at a 200kHz sample rate.

The PCM78 may be interfaced to many popular digital signal processors, such as the TMS320, DSP56001, and the DSP32. Suggested interface circuits for these processors are shown in Figures 17-19.

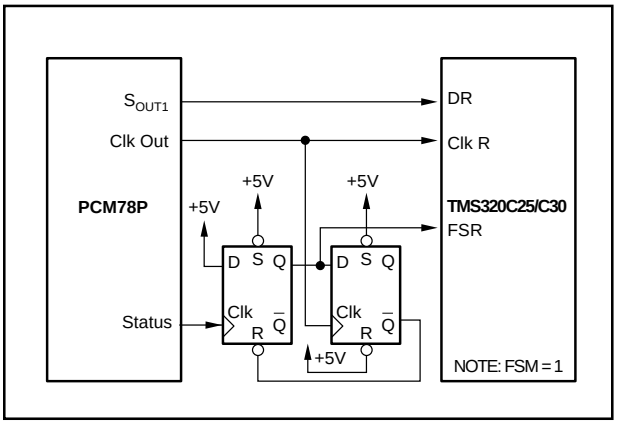


FIGURE 17. PCM78 Interface to TMS320C25/C30 DSP Processors.

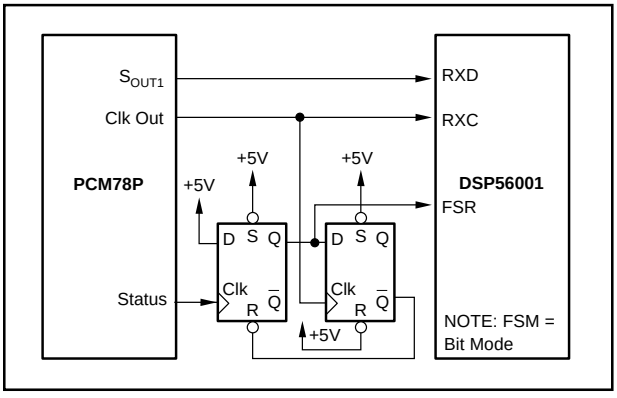


FIGURE 18. PCM78 Interface to Motorola DSP56001 DSP Processor.

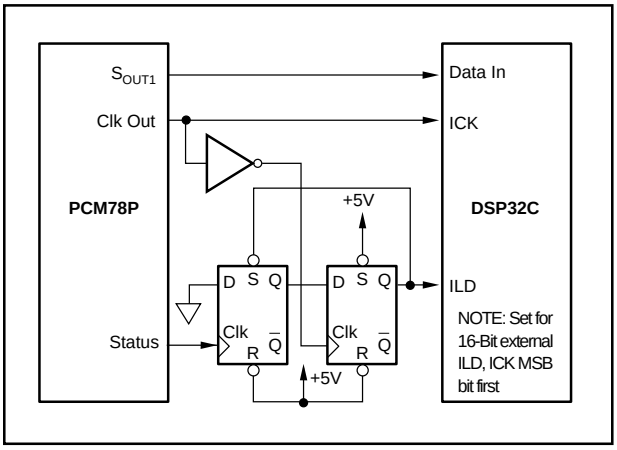


FIGURE 19. PCM78 Interface to AT&T DSP16 & DSP32C Processors.

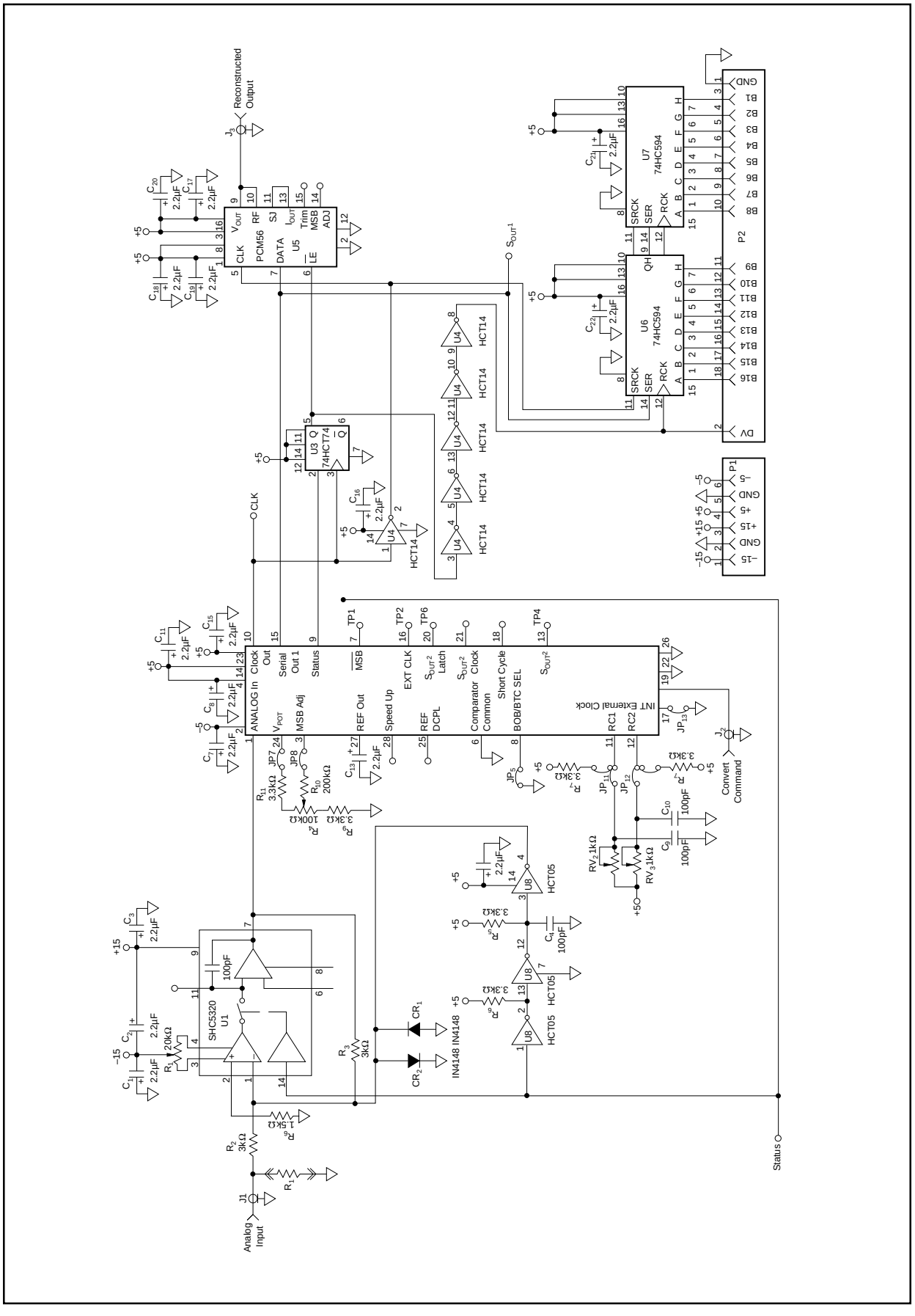


FIGURE 20. Schematic for Demonstration Board (DEM1122).