

Designer's™ Data Sheet

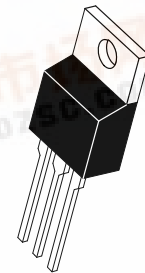
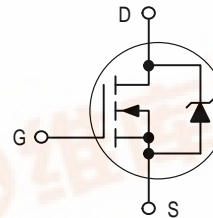
TMOS IV

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate

MTP10N10E

TMOS POWER FETs
10 AMPERES
100 VOLTS
RDS(on) = 0.25 OHM



CASE 221A-06, Style 5
TO-220AB

This advanced "E" series of TMOS power MOSFETs is designed to withstand high energy in the avalanche and commutation modes. These new energy efficient devices also offer drain-to-source diodes with fast recovery times. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating area are critical, and offer additional safety margin against unexpected voltage transients.

- Internal Source-to-Drain Diode Designed to Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode — Unclamped Inductive Switching (UIS) Energy Capability Specified at 100°C
- Commutating Safe Operating Area (CSOA) Specified for Use in Half and Full Bridge Circuits
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|-----------------------------------|------------|---------------|
| Drain-Source Voltage | V _{DSS} | 100 | Vdc |
| Drain-Gate Voltage (R _{GS} = 1.0 MΩ) | V _{DGR} | 100 | Vdc |
| Gate-Source Voltage | V _{GS} | ±20 | Vdc |
| Drain Current — Continuous | I _D | 10 | Adc |
| — Pulsed | I _{DM} | 25 | |
| Total Power Dissipation Derate above 25°C | P _D | 75 0.6 | Watts W/°C |
| Operating and Storage Temperature Range | T _J , T _{stg} | -65 to 150 | °C |

THERMAL CHARACTERISTICS

| | | | |
|---|------------------|------|------|
| Thermal Resistance — Junction to Case | R _{θJC} | 1.67 | °C/W |
| — Junction to Ambient | R _{θJA} | 62.5 | |
| Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds | T _L | 275 | °C |

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

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MOTOROLA

MTP10N10E

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

| Characteristic | Symbol | Min | Max | Unit |
|--|---------------|--------|----------|---------------|
| OFF CHARACTERISTICS | | | | |
| Drain–Source Breakdown Voltage ($V_{GS} = 0$, $I_D = 0.25\text{ mA}$) | $V_{(BR)DSS}$ | 100 | — | Vdc |
| Zero Gate Voltage Drain Current ($V_{DS} = \text{Rated } V_{DSS}$, $V_{GS} = 0$) ($V_{DS} = 0.8 \text{ Rated } V_{DSS}$, $V_{GS} = 0$, $T_J = 125^\circ\text{C}$) | I_{DSS} | — — | 10 80 | μA |
| Gate–Body Leakage Current, Forward ($V_{GSF} = 20\text{ Vdc}$, $V_{DS} = 0$) | I_{GSSF} | — | 100 | nAdc |
| Gate–Body Leakage Current, Reverse ($V_{GSR} = 20\text{ Vdc}$, $V_{DS} = 0$) | I_{GSSR} | — | 100 | nAdc |

ON CHARACTERISTICS*

| | | | | |
|---|--------------|------------|------------|------|
| Gate Threshold Voltage ($V_{DS} = V_{GS}$, $I_D = 1.0\text{ mA}$) $T_J = 100^\circ\text{C}$ | $V_{GS(th)}$ | 2.0 1.5 | 4.5 4.0 | Vdc |
| Static Drain–Source On–Resistance ($V_{GS} = 10\text{ Vdc}$, $I_D = 5.0\text{ Adc}$) | $R_{DS(on)}$ | — | 0.25 | Ohm |
| Drain–Source On–Voltage ($V_{GS} = 10\text{ V}$) ($I_D = 10\text{ Adc}$) ($I_D = 5.0\text{ Adc}$, $T_J = 100^\circ\text{C}$) | $V_{DS(on)}$ | — — | 2.7 2.4 | Vdc |
| Forward Transconductance ($V_{DS} = 15\text{ V}$, $I_D = 5.0\text{ A}$) | g_{FS} | 4.0 | — | mhos |

DRAIN–TO–SOURCE AVALANCHE CHARACTERISTICS

| | | | | |
|---|-----------|-------------|-----------------|----|
| Unclamped Drain–to–Source Avalanche Energy See Figures 14 and 15 ($I_D = 25\text{ A}$, $V_{DD} = 25\text{ V}$, $T_C = 25^\circ\text{C}$, Single Pulse, Non–repetitive) ($I_D = 10\text{ A}$, $V_{DD} = 25\text{ V}$, $T_C = 25^\circ\text{C}$, P.W. $\leq 200\text{ }\mu\text{s}$, Duty Cycle $\leq 1\%$) ($I_D = 4.0\text{ A}$, $V_{DD} = 25\text{ V}$, $T_C = 100^\circ\text{C}$, P.W. $\leq 200\text{ }\mu\text{s}$, Duty Cycle $\leq 1\%$) | W_{DSR} | — — — | 60 100 40 | mJ |
|---|-----------|-------------|-----------------|----|

DYNAMIC CHARACTERISTICS

| | | | | | |
|------------------------------|--|-----------|---|-----|----|
| Input Capacitance | $(V_{DS} = 25\text{ V}$, $V_{GS} = 0$, $f = 1.0\text{ MHz}$ See Figure 16) | C_{iss} | — | 600 | pF |
| Output Capacitance | | C_{oss} | — | 400 | |
| Reverse Transfer Capacitance | | C_{rss} | — | 100 | |

SWITCHING CHARACTERISTICS* ($T_J = 100^\circ\text{C}$)

| | | | | | |
|---------------------|---|--------------|-----------|-----|----|
| Turn–On Delay Time | $(V_{DD} = 25\text{ V}$, $I_D = 5.0\text{ A}$, $R_G = 50\text{ }\Omega$) See Figure 9 | $t_{d(on)}$ | — | 50 | ns |
| Rise Time | | t_r | — | 80 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | — | 100 | |
| Fall Time | | t_f | — | 80 | |
| Total Gate Charge | $(V_{DS} = 0.8 \text{ Rated } V_{DSS}$, $I_D = \text{Rated } I_D$, $V_{GS} = 10\text{ V}$) See Figures 17 and 18 | Q_g | 15 (Typ) | 30 | nC |
| Gate–Source Charge | | Q_{gs} | 8.0 (Typ) | — | |
| Gate–Drain Charge | | Q_{gd} | 7.0 (Typ) | — | |

SOURCE–DRAIN DIODE CHARACTERISTICS*

| | | | | | |
|-----------------------|---|----------|-----------------------------|-----|-----|
| Forward On–Voltage | $(I_S = \text{Rated } I_D$ $V_{GS} = 0)$ | V_{SD} | 1.4 (Typ) | 1.7 | Vdc |
| Forward Turn–On Time | | t_{on} | Limited by stray inductance | | |
| Reverse Recovery Time | | t_{rr} | 70 (Typ) | — | ns |

INTERNAL PACKAGE INDUCTANCE

| | | | | |
|--|-------|------------------------|--------|----|
| Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die) | L_d | 3.5 (Typ) 4.5 (Typ) | — — | nH |
| Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad) | L_s | 7.5 (Typ) | — | |

* Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2.0\%$.

TYPICAL ELECTRICAL CHARACTERISTICS

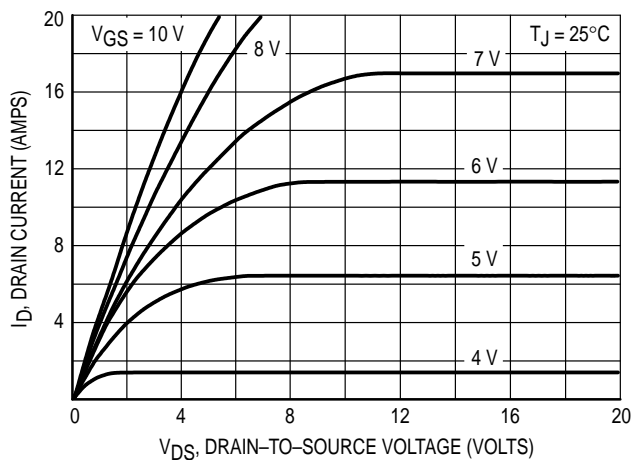


Figure 1. On-Region Characteristics

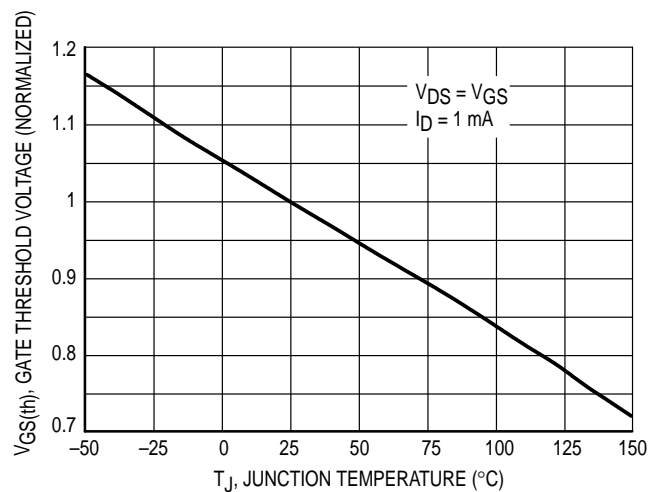


Figure 2. Gate-Threshold Voltage Variation With Temperature

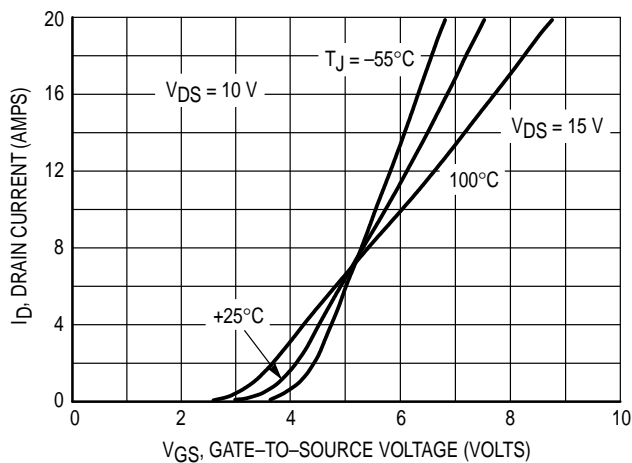


Figure 3. Transfer Characteristics

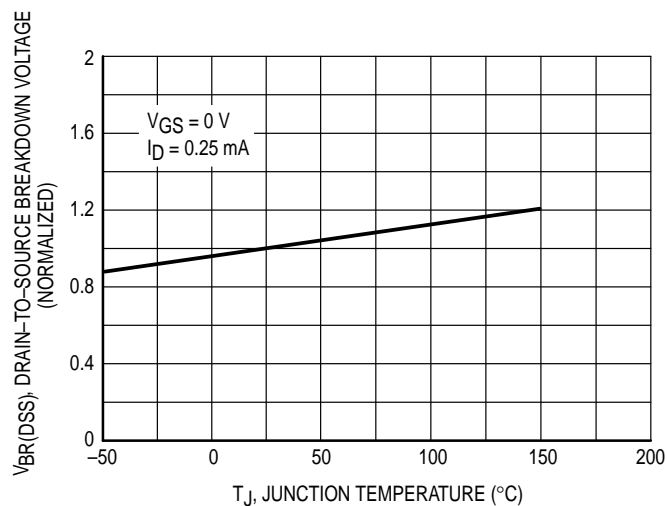


Figure 4. Breakdown Voltage Variation With Temperature

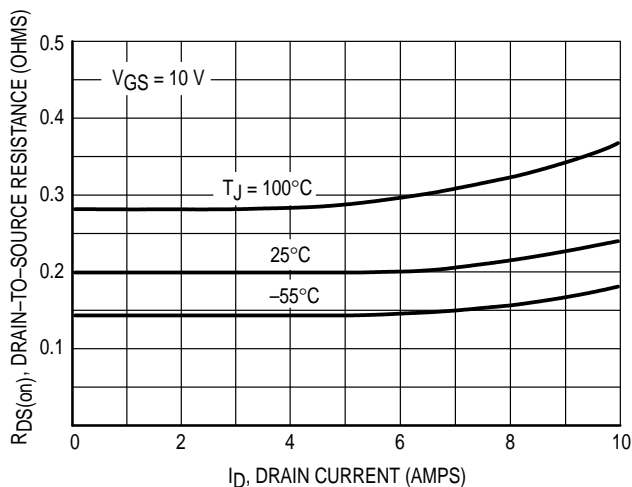


Figure 5. On-Resistance versus Drain Current

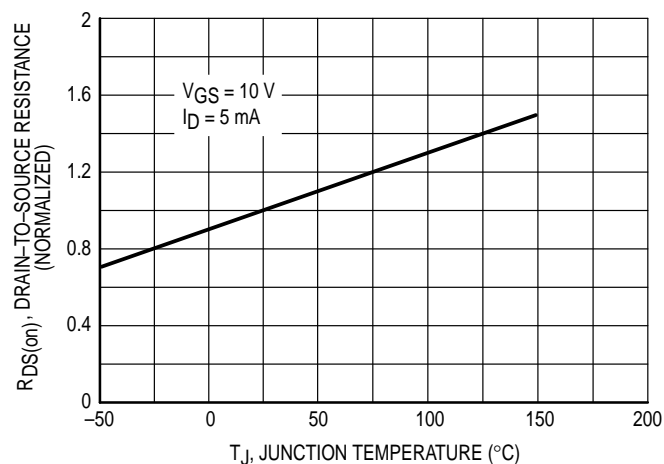


Figure 6. On-Resistance Variation With Temperature

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SAFE OPERATING AREA INFORMATION

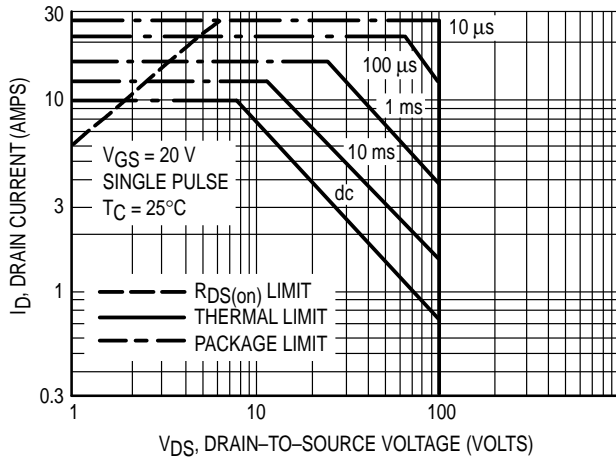


Figure 7. Maximum Rated Forward Biased Safe Operating Area

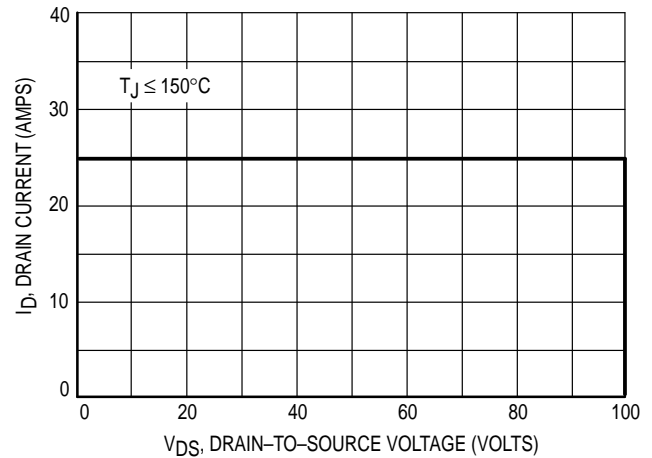


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance—General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

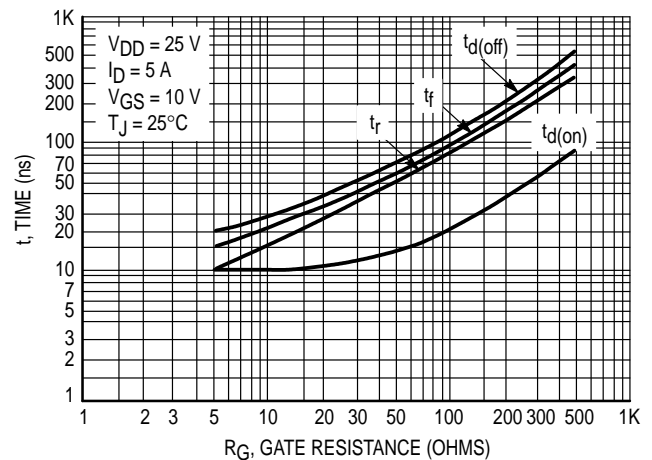


Figure 9. Resistive Switching Time versus Gate Resistance

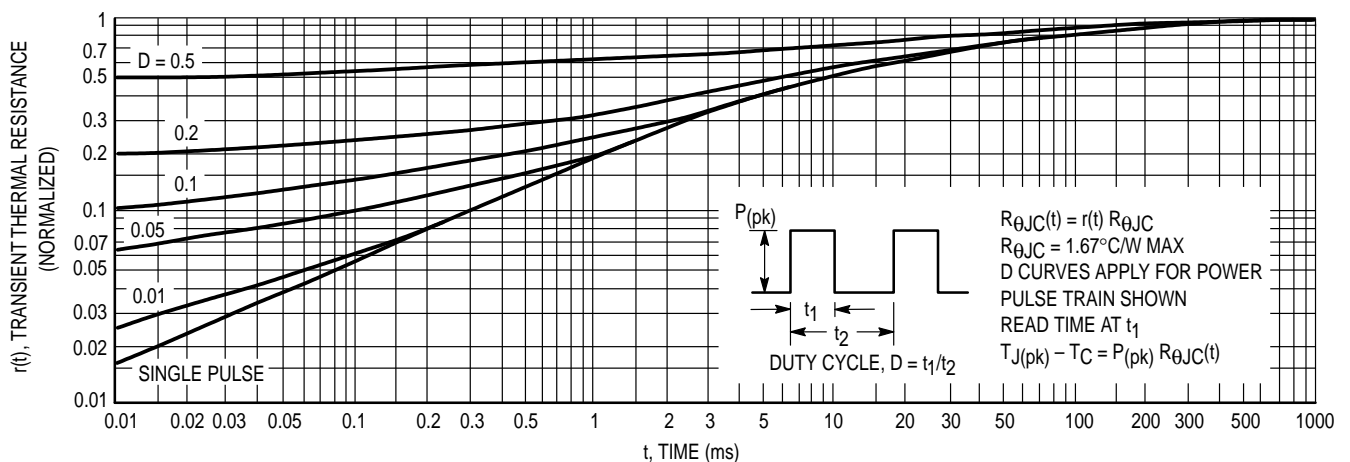


Figure 10. Thermal Response

COMMUTATING SAFE OPERATING AREA (CSOA)

The Commutating Safe Operating Area (CSOA) of Figure 12 defines the limits of safe operation for commutated source-drain current versus re-applied drain voltage when the source-drain diode has undergone forward bias. The curve shows the limitations of I_{FM} and peak V_{DS} for a given rate of change of source current. It is applicable when waveforms similar to those of Figure 11 are present. Full or half-bridge PWM DC motor controllers are common applications requiring CSOA data.

Device stresses increase with increasing rate of change of source current so di_s/dt is specified with a maximum value. Higher values of di_s/dt require an appropriate derating of I_{FM} , peak V_{DS} or both. Ultimately di_s/dt is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during t_{rr} as the diode goes from conduction to reverse blocking.

$V_{DS(pk)}$ is the peak drain-to-source voltage that the device must sustain during commutation; I_{FM} is the maximum forward source-drain diode current just prior to the onset of commutation.

V_R is specified at 80% of $V_{(BR)DSS}$ to ensure that the CSOA stress is maximized as I_S decays from I_{RM} to zero.

R_{GS} should be minimized during commutation. T_J has only a second order effect on CSOA.

Stray inductances in Motorola's test circuit are assumed to be practical minimums. dV_{DS}/dt in excess of 10 V/ns was attained with di_s/dt of 400 A/ μ s.

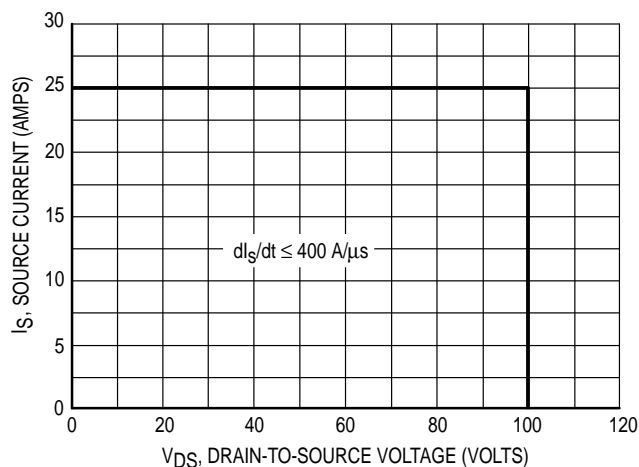


Figure 12. Commutating Safe Operating Area (CSOA)

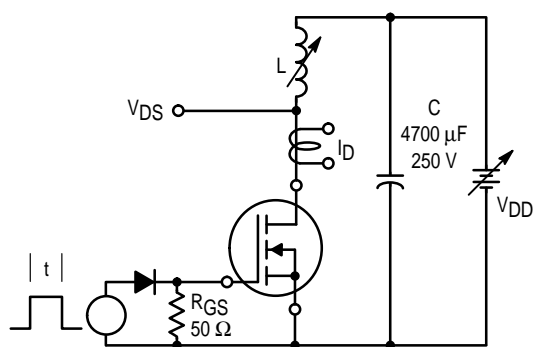


Figure 14. Unclamped Inductive Switching Test Circuit

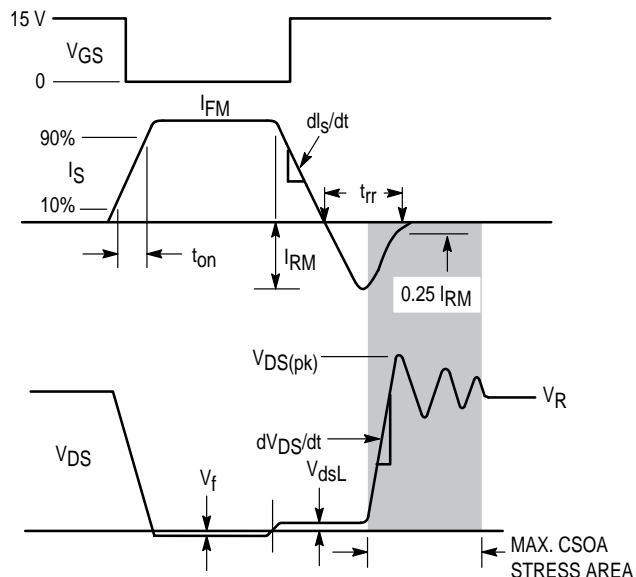


Figure 11. Commutating Waveforms

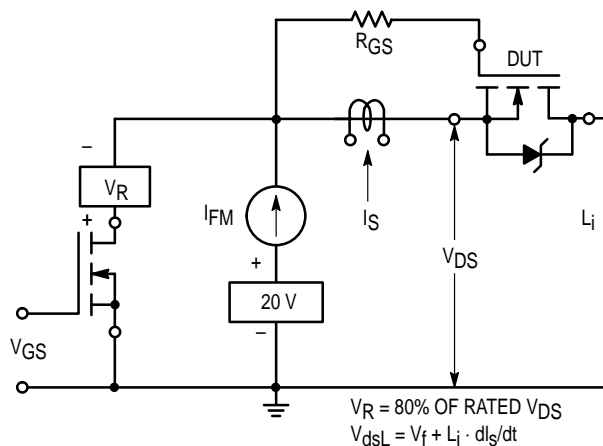


Figure 13. Commutating Safe Operating Area Test Circuit

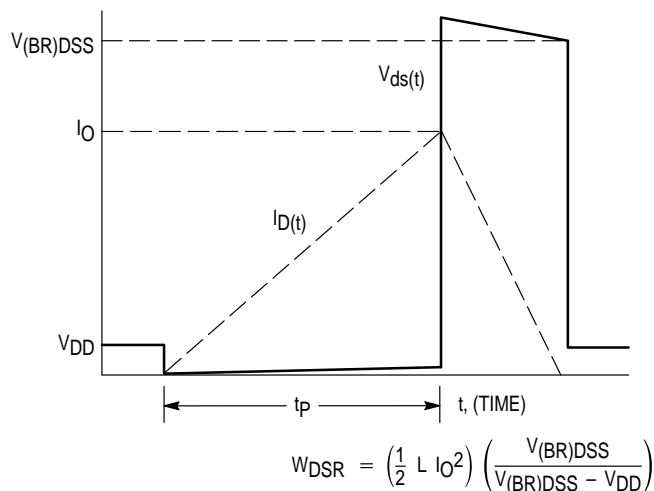


Figure 15. Unclamped Inductive Switching Waveforms

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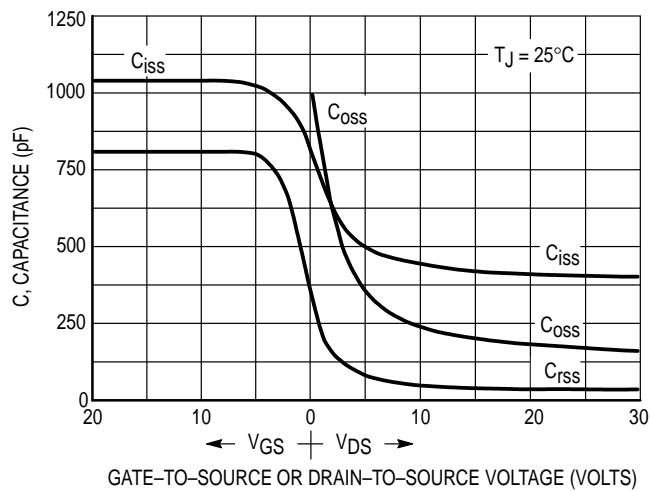


Figure 16. Capacitance Variation

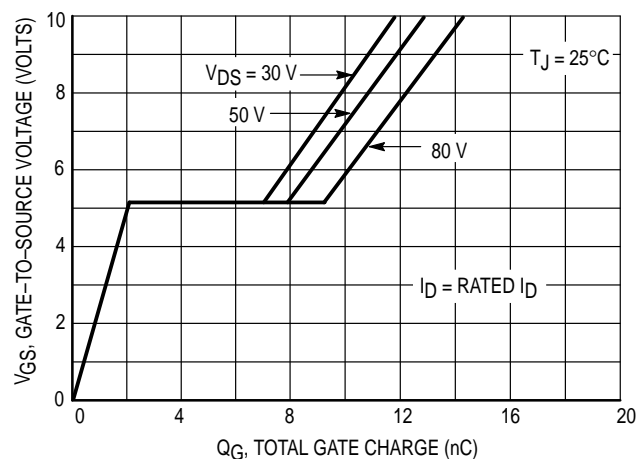
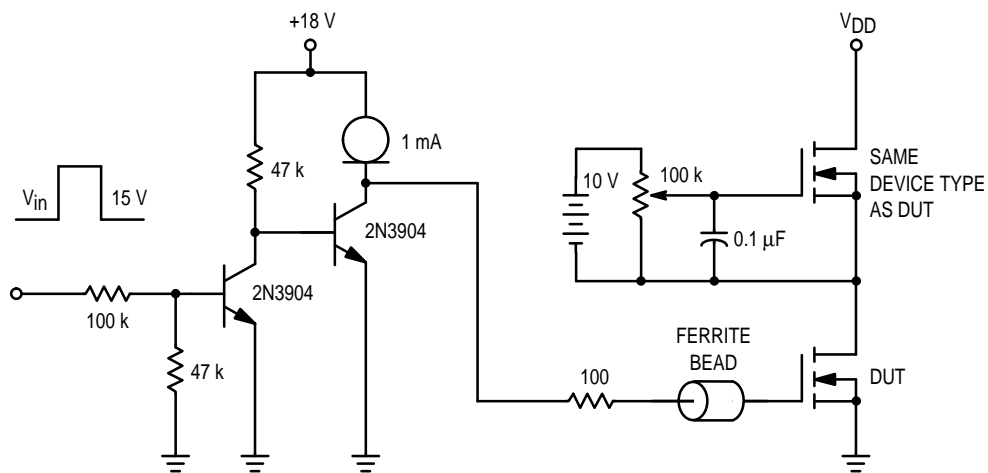


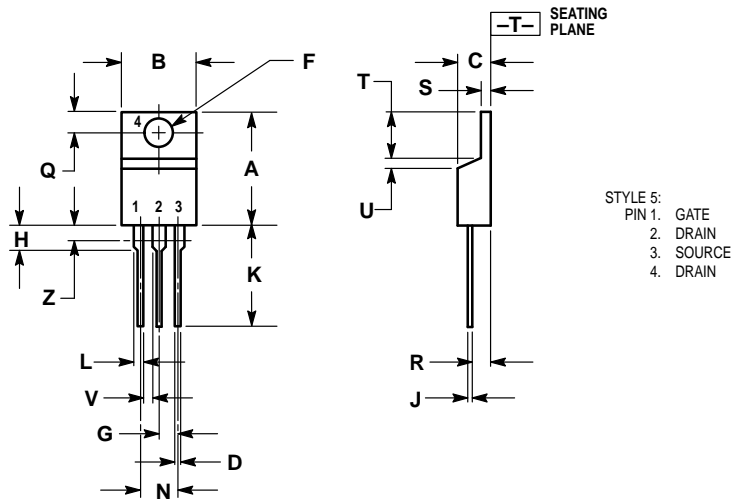
Figure 17. Gate Charge versus Gate-To-Source Voltage



$V_{in} = 15\text{ V}_{pk}$; PULSE WIDTH $\leq 100\text{ }\mu\text{s}$, DUTY CYCLE $\leq 10\%$

Figure 18. Gate Charge Test Circuit

PACKAGE DIMENSIONS




- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

| DIM | INCHES | | MILLIMETERS | |
|-----|--------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.570 | 0.620 | 14.48 | 15.75 |
| B | 0.380 | 0.405 | 9.66 | 10.28 |
| C | 0.160 | 0.190 | 4.07 | 4.82 |
| D | 0.025 | 0.035 | 0.64 | 0.88 |
| F | 0.142 | 0.147 | 3.61 | 3.73 |
| G | 0.095 | 0.105 | 2.42 | 2.66 |
| H | 0.110 | 0.155 | 2.80 | 3.93 |
| J | 0.018 | 0.025 | 0.46 | 0.64 |
| K | 0.500 | 0.562 | 12.70 | 14.27 |
| L | 0.045 | 0.060 | 1.15 | 1.52 |
| N | 0.190 | 0.210 | 4.83 | 5.33 |
| Q | 0.100 | 0.120 | 2.54 | 3.04 |
| R | 0.080 | 0.110 | 2.04 | 2.79 |
| S | 0.045 | 0.055 | 1.15 | 1.39 |
| T | 0.235 | 0.255 | 5.97 | 6.47 |
| U | 0.000 | 0.050 | 0.00 | 1.27 |
| V | 0.045 | — | 1.15 | — |
| Z | — | 0.080 | — | 2.04 |

CASE 221A-06
ISSUE Y

MTP10N10E

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