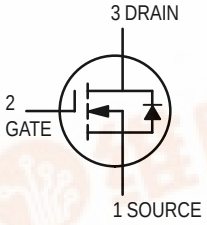
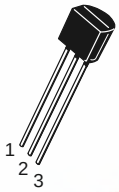
TMOS FET Transistor
N–Channel — Enhancement



VN2410L



CASE 29–04, STYLE 22
TO–92 (TO–226AA)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	240	Vdc
Drain–Gate Voltage	V_{DGR}	60	Vdc
Gate–Source Voltage – Continuous – Non–repetitive ($t_p \leq 50$ µs)	 V_{GS} V_{GSM}	 ± 20 ± 40	 Vdc Vpk
Continuous Drain Current	I_D	200	mAdc
Pulsed Drain Current	I_{DM}	500	mAdc
Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	350 2.8	mW mW/°C
Operating and Storage Temperature	T_J, T_{stg}	—	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	312.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/16″ from case for 10 seconds	T_L	300	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

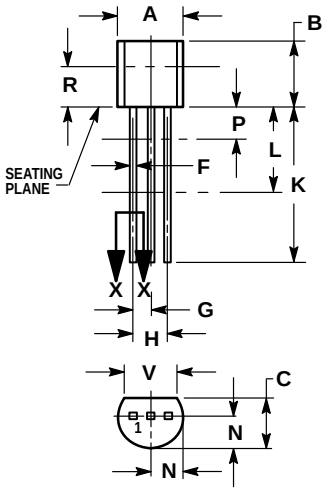
Characteristic	Symbol	Min	Max	Unit
STATIC CHARACTERISTICS				
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 100 µA)	$V_{(BR)DSS}$	240	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 120 Vdc, V_{GS} = 0) (V_{DS} = 120 Vdc, V_{GS} = 0, T_A = 125°C)	I_{DSS}	 — —	 10 500	µAdc
Gate– Body Leakage (V_{DS} = 0, V_{GS} = ±15 V)	I_{GSS}	—	±100	nAdc
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1.0 mA)	$V_{GS(th)}$	0.8	2.0	Vdc
On–State Drain Current(1) (V_{GS} = 10 V, $V_{DS} \geq 2.0\ V_{DS(on)}$)	$I_{D(on)}$	1.0	—	Adc
Drain–Source On Resistance(1) (V_{GS} = 2.5 V, I_D = 0.1 A) (V_{GS} = 10 V, I_D = 0.5 A)	$r_{DS(on)}$	 — —	 10 10	Ω
Forward Transconductance(1) (V_{DS} = 10 V, I_D = 0.5 A)	g_{fs}	300	—	mS

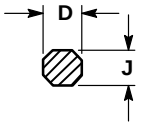
1. Pulse Test; Pulse Width < 300 µs, Duty Cycle ≤ 2.0%.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) (Continued)

Characteristic		Symbol	Min	Max	Unit
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	125	pF
Output Capacitance		C_{oss}	—	50	pF
Reverse Transfer Capacitance		C_{rss}	—	20	pF
SWITCHING CHARACTERISTICS					
Turn–On Time	(V_{DD} = 60 Vdc, I_D = 0.4 A, R_L = 150 Ω, R_G = 25 Ω)	$t_{(on)}$	—	8.0	ns
		$t_{(r)}$	—	8.0	ns
Turn–Off Time		$t_{(off)}$	—	23	ns
		$t_{(f)}$	—	34	ns

PACKAGE DIMENSIONS





SECTION X–X

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. DIMENSION F APPLIES BETWEEN P AND L. DIMENSION D AND J APPLY BETWEEN L AND K MINIMUM. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.175	0.205	4.45	5.20
B	0.170	0.210	4.32	5.33
C	0.125	0.165	3.18	4.19
D	0.016	0.022	0.41	0.55
F	0.016	0.019	0.41	0.48
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.015	0.020	0.39	0.50
K	0.500	—	12.70	—
L	0.250	—	6.35	—
N	0.080	0.105	2.04	2.66
P	—	0.100	—	2.54
R	0.115	—	2.93	—
V	0.135	—	3.43	—

CASE 029–04
(TO–226AA)
ISSUE AD

STYLE 22:
PIN 1. SOURCE
2. GATE
3. DRAIN

How to reach us:

USA / EUROPE / Locations Not Listed: Motorola Literature Distribution;
P.O. Box 5405, Denver, Colorado 80217. 303–675–2140 or 1–800–441–2447

Mfax™: RMFAX0@email.sps.mot.com – TOUCHTONE 602–244–6609
– US & Canada ONLY 1–800–774–1848

INTERNET: http://motorola.com/sps

JAPAN: Nippon Motorola Ltd.: SPD, Strategic Planning Office, 4–32–1,
Nishi–Gotanda, Shinagawa–ku, Tokyo 141, Japan. 81–3–5487–8488

ASIA / PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298