# Clock generator for video CD systems
## BU2173F

The BU2173F is an IC that generates the CPU clock signal, system clock signal and video clock signal used in video CD systems. A single crystal resonator can generate three different oscillation frequencies.
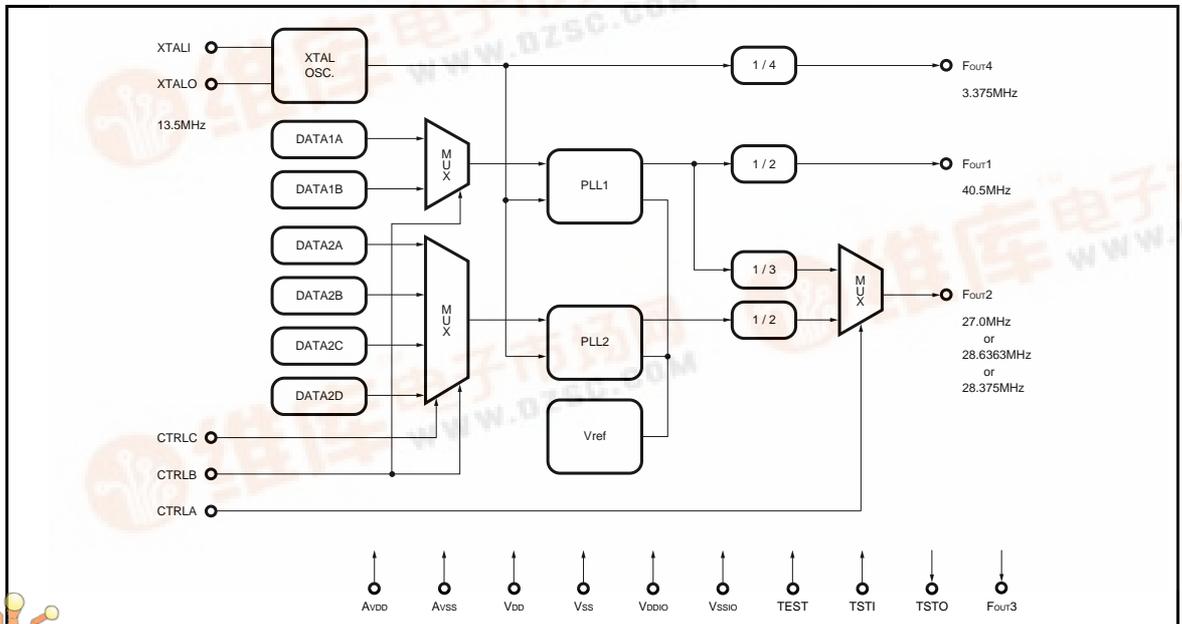
●Applications
Video CD systems

●Features
1) Three frequency clock signals can be generated with a single attached crystal resonator.
2) Two internal PLL channels.
3) Internal loop filter, eliminating the need to attach a loop.
4) Single 5.0V power supply.
5) SOP 18-pin package.

●Block diagram

●Pin description

| Pin No. | Pin name | Function | Type |
|---------|----------|----------|------|
| 1 | $V_{DD}$ | Digital $V_{DD}$ | — |
| 2 | TSTO | Open in the normal mode (used for testing) | B |
| 3 | XTALI | Reference oscillation input | C |
| 4 | XTALO | Reference oscillation output | C |
| 5 | CTRLA | GD-G / VCD clock switching | A |
| 6 | CTRLB | Stays at the high level when the IC is in the normal mode | A |
| 7 | CTRLC | CD-G PAL / NTSC clock switching | A |
| 8 | TSTI | Connect to Vss when the IC is in the normal mode (used for testing) | A |
| 9 | $V_{SS}$ | Digital ground | — |
| 10 | $A_{VSS}$ | Analog ground | — |
| 11 | $F_{OUT}3$ | Not used (open when the IC is in the normal mode) | B |
| 12 | $V_{SSIO}$ | I / O ground | — |
| 13 | $F_{OUT}2$ | Clock output 2 | B |
| 14 | TEST | Setting the test mode (connect to Vss when the IC is in the normal mode) | A |
| 15 | $F_{OUT}1$ | Clock output 1 | B |
| 16 | $V_{DDIO}$ | I / O $V_{DD}$ | — |
| 17 | $F_{OUT}4$ | Clock output 4 | B |
| 18 | $A_{VDD}$ | Analog $V_{DD}$ | — |

●Absolute maximum ratings (Ta = 25°C)

| Parameter | Symbol | Limits | Unit |
|-----------|--------|--------|------|
| Power supply voltage | $V_{DD}$ | − 0.3 ~ + 7.0 | V |
| Power dissipation | Pd | 450 | mW |
| Operating temperature | Topr | − 5 ~ + 70 | °C |
| Storage temperature | Tstg | − 25 ~ + 125 | °C |

＊ Reduced by 4.5 mW for each increase in Ta of 1°C over 25°C.

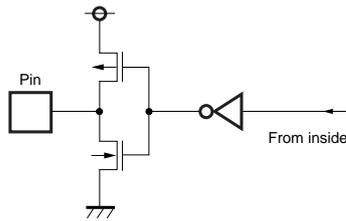●Recommended operating conditions (Ta = 25°C)

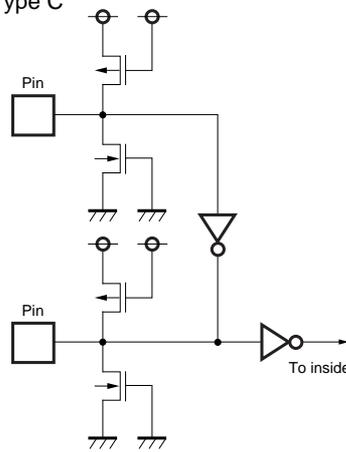| Parameter | Symbol | Limits | Unit |
|-----------|--------|--------|------|
| Power supply voltage | $V_{DD}$, $A_{VDD}$, $V_{DDIO}$ | 4.75 ~ 5.25 | V |
| Input high level voltage | $V_{IH}$ | $0.8V_{DD}$ ~ $V_{DD}$ | V |
| Input low level voltage | $V_{IL}$ | 0.0 ~ $0.2V_{DD}$ | V |
| Operating temperature | Topr | − 5 ~ + 70 | °C |

● Input / output circuits

Type A
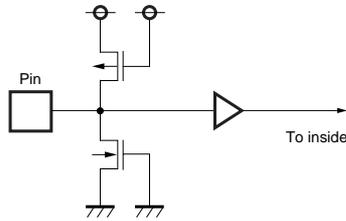


Type B



Type C



● Electrical characteristics (unless otherwise noted, Ta = 25°C, $V_{DD}$ = 5.0V, $A_{VDD}$ = 5.0V, $IO_{VDD}$ = 5.0V)

| Parameter | | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| Input current, low level | | $I_{IL}$ | − 300.0 | 0.0 | 300.0 | µA | — |
| Input current, high level | | $I_{IH}$ | − 300.0 | 0.0 | 300.0 | µA | — |
| Input voltage, low level | | $V_{IL}$ | — | — | 1.0 | V | — |
| Input voltage, high level | | $V_{IH}$ | 4.0 | — | — | V | — |
| Output voltage, low level | | $V_{OL}$ | — | — | 0.5 | V | $I_{OL}$ = 4.0mA |
| Output voltage, high level | | $V_{OH}$ | 2.4 | — | — | V | $I_{OH}$ = − 4.0mA |
| Operating supply current | | $I_{DD}$ | — | 30 | 50 | mA | $f_{XTAL}$ = 13.5 MHz, no load |
| Reference frequency | | $f_{REF}$ | — | 13.5 | — | MHz | Use with CTRLB at the high level |
| Output frequency | (1) | $f_1$ | — | 40.5 | — | MHz | $f_1 = f_{REF} \times 96 / 16 / 2$ |
| Output frequency | (2) | $f_{2A}$ | — | 27.000 | — | MHz | $f_{2A} = f_{REF} \times 96 / 16 / 3$<br>CTRLA = H, CTRLB = H, CTRLC = H |
| | | $f_{2B}$ | — | 28.375 | — | MHz | $f_{2B} = f_{REF} \times 227 / 54 / 2$<br>CTRLA = L, CTRLB = H, CTRLC = L |
| | | $f_{2C}$ | — | 28.636 | — | MHz | $f_{2C} = f_{REF} \times 140 / 33 / 2$<br>CTRLA = L, CTRLB = H, CTRLC = H |
| Output frequency | (4) | $f_4$ | — | 3.375 | — | MHz | $f_4 = f_{REF} \times 1 / 4$ |
| Jitter | | | — | 1.0 | — | ns | Measure at $f_{2A}$, $f_{2B}$, $f_{2C}$ (reference) |
| Reference frequency | (2) | $f_{REF2}$ | — | 14.318 | — | MHz | Use with CTRLB at the low level |
| Output frequency | (1) | $f_{1B}$ | — | 40.5 | — | MHz | $f_{1B} = f_{REF2} \times 98 / 35 / 2$ |
| Output frequency | (2) | $f_{2D}$ | — | 27.000 | — | MHz | $f_{2D} = f_{REF2} \times 98 / 35 / 3$<br>CTRLA = H, CTRLB = L, CTRLC = H |
| | | $f_{2E}$ | — | 28.636 | — | MHz | $f_{2E} = f_{REF2} \times 80 / 20 / 2$<br>CTRLA = L, CTRLB = L, CTRLC = H |
| Output frequency | (4) | $f_{4B}$ | — | 3.579 | — | MHz | $f_{4B} = f_{REF2} \times 1 / 4$ |

●Measurement circuit
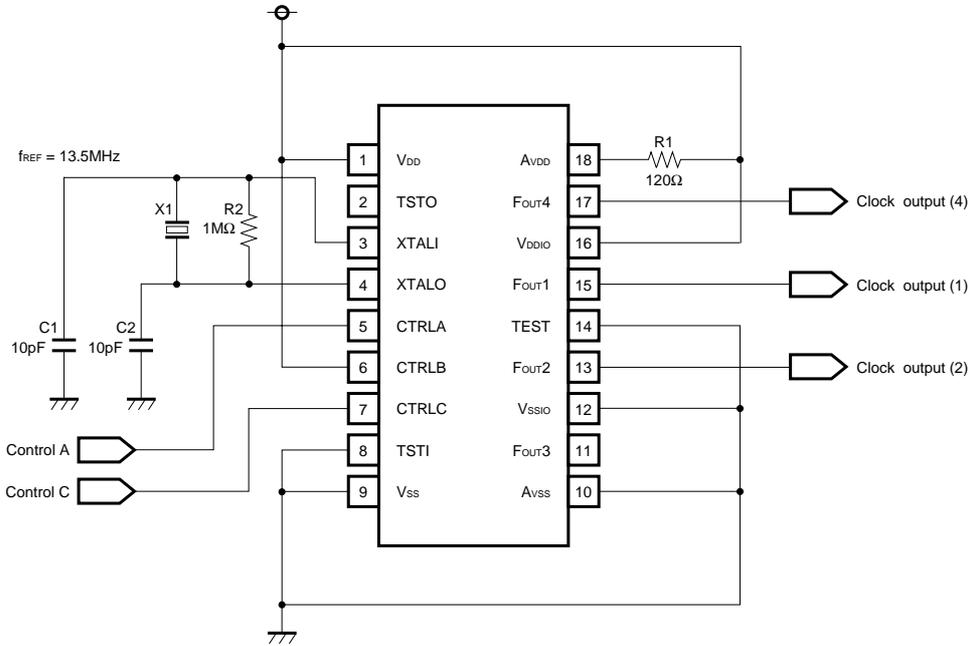


Note: Certain crystal resonators may require setting
XTALI and XTALO to the optimum allowable values.

●Application example
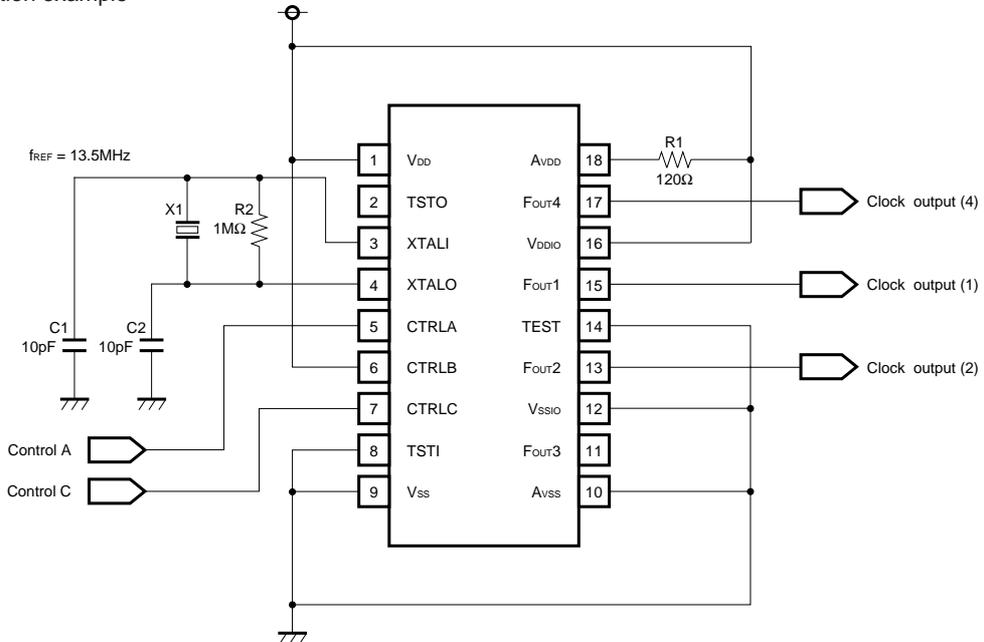


Note: Certain crystal resonators may require setting
XTALI and XTALO to the optimum allowable values.

＊ This IC should be used mounted on a PC board. If mounted in
a socket, characteristics of the IC may be adversely affected.

●Attached components

R1: To keep the voltage of $A_{VDD}$ effectively low, and to enhance signal stability by separating $A_{VDD}$ and $D_{VDD}$ with an impedance. Be sure to attach.

R2: Needed to provide a feedback resistance for the crystal resonator

C1 / C2: When $f_0$ must be adjusted according to the crystal resonator used, or when the crystal resonator results in unnecessary oscillation points, attach a PF and adjust according to the value for this capacitor.

X1: Use a crystal resonator with an oscillation frequency of 13.5 MHz or 14.318 MHz.

●External dimensions (Units: mm)

SOP18