ID ROM for CRT displays supporting plug & play

BU9881 / BU9881F

The BU9881 / BU9881F is a 1k bit EEPROM conforming to the standardized interface that enables Plug & Play on CRT displays.

●Applications

Desktop CRT displays
Desktop LCD displays
Other desktop PC displays
External CRT displays for notebook computers

●Features

1) 1kbit serial EEPROM with configuration of 128 words × 8 bits.
2) Supports I^2C bus.
3) Supports DDC1™/ DDC2™ interfaces for monitor IDs.

∗ DDC is a registered trademark of VESA.

4) Supports clock frequencies of 100kHz and 400kHz.
5) Switching from DDC2 to DDC1 enabled using mode pin.

●Absolute maximum ratings (Ta = 25°C)

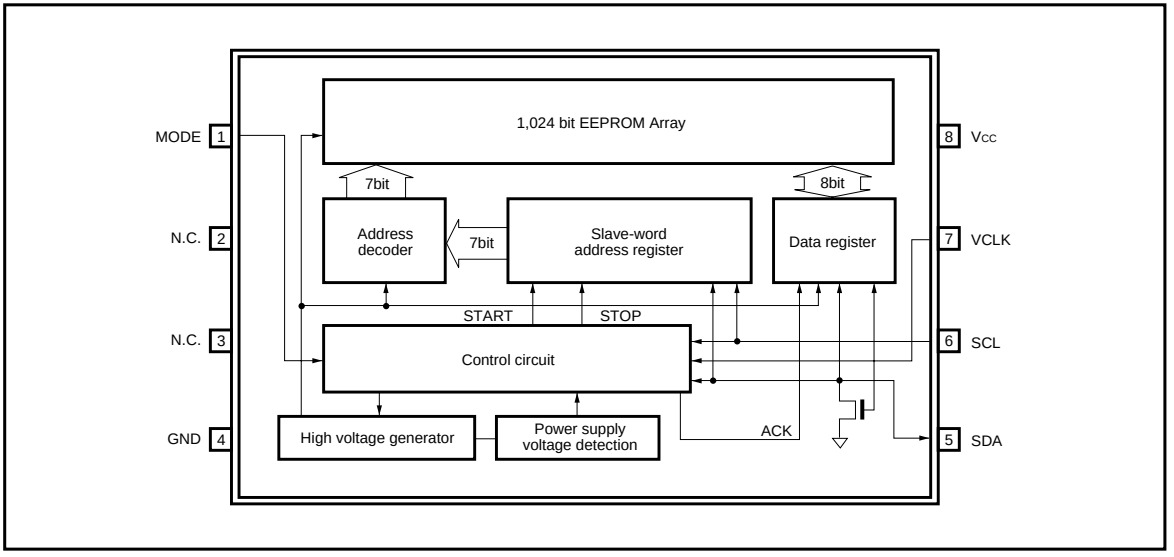
Parameter		Symbol	Limits	Unit
Applied voltage		V_{CC}	– 0.3 ~ + 6.5	V
Power dissipation	BU9881	Pd	500∗1	mW
	BU9881F		350∗2	
Storage temperature		Tstg	– 65 ~ + 125	°C
Operating temperature		Topr	– 40 ~ + 85	°C
Voltage for various pins		—	– 0.3 ~ V_{CC} + 0.3	V

∗1 Reduced by 5.0mW for each increase in Ta of 1°C over 25°C.
∗2 Reduced by 3.5mW for each increase in Ta of 1°C over 25°C.
∗ If input exceeds the absolute maximum ratings, the device may break down.

●Recommended operating conditions

Parameter	Symbol	Limits	Unit
Power supply voltage	V_{CC}	2.7 ~ 5.5	V
Input voltage	V_{IN}	0 ~ V_{CC}	V

●Block diagram



●Pin descriptions

Pin No.	Pin name	I / O	Function
1	MODE	I	Transmit-only mode switching pin (pulled down when used in open state)
2, 3	N.C.	—	Not connected
4	GND	—	Reference voltage of 0V for all input / output
5	SDA	I / O	Slave and word address serial data input / output
6	SCL	I	Serial clock input pin for I^2C mode
7	VCLK	I	Clock input pin for transmit-only mode
8	Vcc	—	Connect the power supply

○The SDA pin is Nch open drain output, and should be used with an external pull-up resistor added.

●Electrical characteristics (unless otherwise noted, Ta = – 40 to + 85°C, Vcc = 2.7V to 5.5V)

Parameter	Symbol	Min.	Max.	Unit	Conditions	Measurement Circuit
Input high level voltage 1	V_{IH1}	0.7V_{CC}	—	V	(SCL, SDA)	—
Input low level voltage 1	V_{IL1}	—	0.3V_{CC}	V	(SCL, SDA)	—
Input high level voltage 2	V_{IH2}	2.0	—	V	(VCLK)	—
Input low level voltage 2	V_{IL2}	— —	0.8 0.4	V	V_{CC} = 4.5 ~ 5.5V (VCLK) V_{CC} = 2.7 ~ 4.5V (VCLK)	—
Input high level voltage 3	V_{IH3}	0.8V_{CC}	—	V	(MODE)	—
Input low level voltage 3	V_{IL3}	—	0.4	V	(MODE)	—
Output low level voltage	V_{OL}	—	0.4	V	I_{OL} = 3.0mA(SDA)	Fig.1
Input leakage current 1	I_{LI1}	– 1	1	µA	V_{IN} = 0V ~ V_{CC} (SCL · SDA · VCLK)	Fig.2
Input leakage current 2	I_{LI2}	– 1	15	µA	V_{IN} = 0V ~ V_{CC} (MODE)	Fig.2
Output leakage current	I_{LO}	– 1	1	µA	V_{OUT} = 0V ~ V_{CC} (SDA)	Fig.2
Operating current consumption	I_{CC}	—	3	mA	V_{CC} = 5.5V, tWR = 10ms	Fig.3
Standby current	I_{SB}	—	30	µA	V_{CC} = 5.5V, MODE = GND VCLK · SDA · SCL = V_{CC}	Fig.4

●Measurement circuits

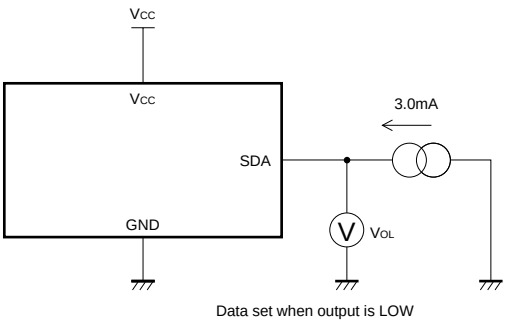


Fig. 1 LOW output voltage measurement circuit

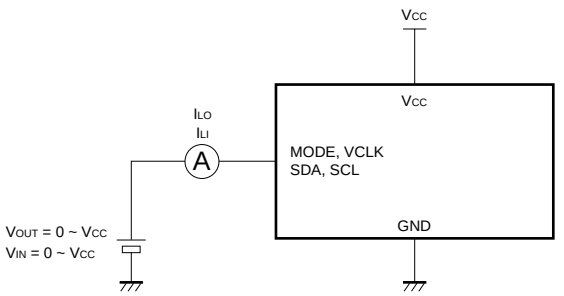


Fig. 2 Input / output leakage current measurement circuit

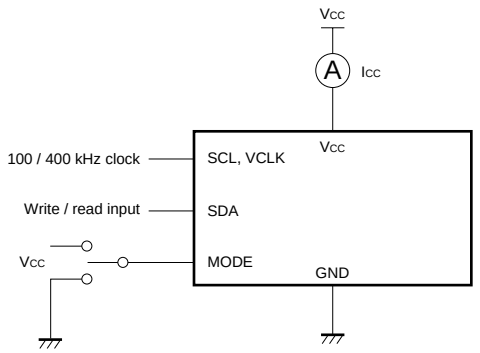


Fig. 3 Current consumption measurement circuit

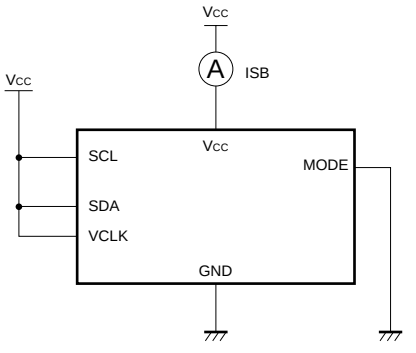


Fig. 4 Standby current measurement circuit

●Operation timing characteristics (unless otherwise noted, Ta = – 40 to + 85°C)

Parameter	Symbol	Standard Mode V_{CC} = 2.7 ~ 5.5V		High-speed Mode V_{CC} = 4.5 ~ 5.5V		Unit
		Min.	Max.	Min.	Max.	
Clock frequency	f SCL	0	100	0	400	kHz
Data clock HIGH time	t HIGH	4.0	—	0.6	—	µs
Data clock LOW time	t LOW	4.7	—	1.3	—	µs
SDA / SCL rise time	t R	—	1.0	—	0.3	µs
SDA / SCL fall time	t F	—	1.0	—	0.3	µs
Start condition hold time	t HD:STA	4.0	—	0.6	—	µs
Start condition setup time	t SU:STA	4.7	—	0.6	—	µs
Input data hold time	t HD:DAT	0	—	0	—	ns
Input data setup time	t SU:DAT	250	—	100	—	µs
Output data delay time	t PD	0	3.5	0	0.9	µs
Output data hold time	t DH	0	—	0	—	µs
Stop condition setup time	t SU:STO	4.7	—	0.6	—	µs
Bus release time prior to start of transfer	t BUF	4.7	—	1.3	—	µs
Internal write cycle time	t WR	—	10	—	10	ms
Effective noise elimination interval (SCL, SDA pins)	t I	—	—	—	50	ns

●Transmit – only MODE

Parameter	Symbol	Standard Mode V_{CC} = 2.7 ~ 5.5V		High-speed Mode V_{CC} = 4.5 ~ 5.5V		Unit
		Min.	Max.	Min.	Max.	
VCLK output delay time	TVAA	—	500	—	500	ns
VCLK HIGH time	TVHIGH	4.0	—	0.6	—	µs
VCLK LOW time	TVLOW	4.7	—	1.3	—	µs
★Mode transition time	TVHZ	—	500	—	500	ns
★Power up time for transmission	TVPU	0	—	0	—	ns

●Circuit operation

○Basic operation

The BU9881 / BU9881F is equipped with two modes, a normal I²C bus mode (bi-directional mode) and a transmit-only mode.

- The transmit-only mode can be accessed by turning on the power supply to the IC, or by using the software to control the mode. In this mode, operation is synchronized to the clock input to VCLK, and it is possible to read the contents of the EEPROM memory from the SDA pin.
- To switch from the transmit-only mode to the I²C bus mode, the clock signal that recognizes the switching of HIGH to LOW is input to the SCL pin. The I²C bus mode is effective following the edge of that clock.
- To switch from the I²C bus mode to the transmit-only mode, the software can be used to control the mode, or the power supply to the IC can be turned off and then on again. This switches back to the transmit-only mode.

(1) Description of mode pin functions

As shown in the illustration below, the software can be used to control the mode pin, enabling switching from the I²C bus mode to the transmit-only mode.

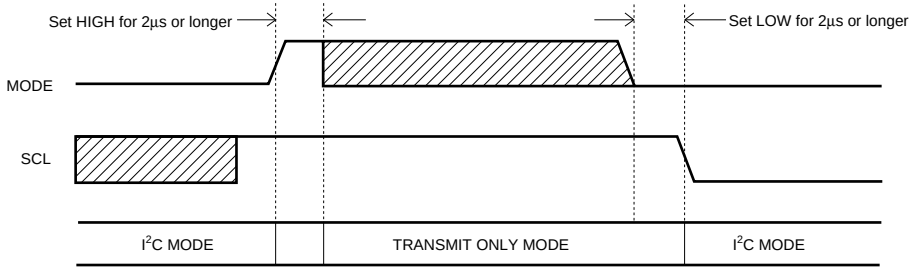


Fig. 5

1)Transmit-only mode

- This command causes all of the data written to the EEPROM to be read. After the transmit-only mode is entered, inputting the VCLK clock causes the data to be read from the SDA pin.
- The SDA pin is in the "Hi-Z" state for the first nine clock signals input, and data is output sequentially, timed to the rise of the clock starting with the tenth clock.
- Addresses are incremented automatically as clock pulses continue to be input to VCLK, with the data from the next address being read in sequence. While this is being done, the null bit (HIGH data) is output between the data of one address and that of the next address.
- When the power supply is turned on, and when the mode is switched from the I²C bus mode to the transmit-only mode, the output data for the transmit-only mode is synchronized to VCLK as follows:

  Last address data→0h address data→1h address data→→→

  and is incremented in sequence.

  (Following the last address, processing shifts to the 0h address.)

Note: Reading in the transmit-only mode should not be done until the power supply has stabilized. When switching from the transmit-only mode to the I²C bus mode, assure the TVHZ time before beginning communications.

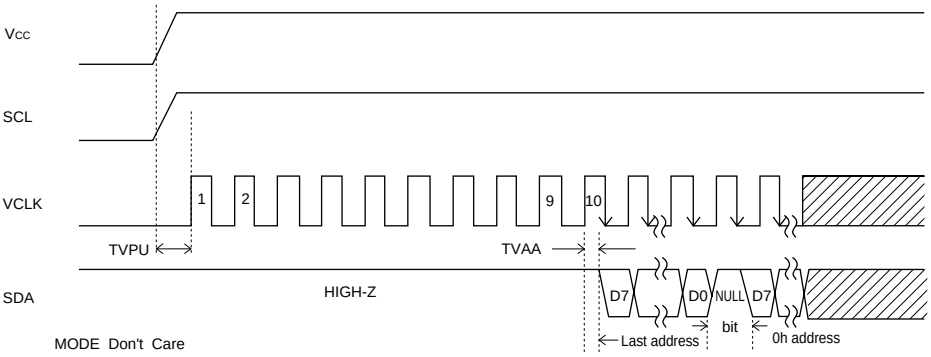


Fig. 6

2) I²C bus mode

1. Start condition (start bit recognition)
   - Before executing the various commands, if SDA is HIGH, a start condition (start bit) must be in effect such that SDA changes from HIGH to LOW.
   - This IC constantly detects whether or not the start condition (start bit) is fulfilled for the SDA and SCL lines. If this condition is not fulfilled, no commands will be executed. (Refer to the section on synchronized data input / output timing.)

2. Stop condition (stop bit recognition)
   - When the various commands have been completed, a stop condition (stop bit) can be used to terminate the commands by raising SDA from LOW to HIGH if SCL is HIGH. (Refer to the section on synchronized data input / output timing.)

3. Precautions concerning the write command

∗ The stop bit cannot be executed in the write mode, so data that has been transmitted cannot be written to the memory.

4. Write protect

In the I²C bus mode, the VCLK pin can be used as a write protect control pin. When the VCLK pin is HIGH, the byte write and page write commands function, but when the VCLK pin is LOW, these two writing commands are canceled.

(2) Device addressing

- The master address should be output first, followed by the start condition, and then the slave address.
- The first four bits of the slave address are used to recognize the device type. The device code for this IC is fixed at "1010".
- The next three bits of the slave address may be either HIGH or LOW.
- The last bit of the slave address ($\overline{R}$ / W: READ / $\overline{WRITE}$) is used to specify either writing or reading, and is as shown below.

R / $\overline{W}$ set to 0: Writing
(0 is also set in order to specify a word address for random reading.)

R / $\overline{W}$ set to 1: Reading

1010	×	×	×	R / $\overline{W}$

×: Don't Care

(3) ACK signal

- This acknowledge signal (ACK signal) is determined by the software, and indicates whether or not the data has been correctly transmitted. Regardless of whether the address is a master or slave address, the device on the transmitter (sending signal) side (the µ-com when a slave address is input for a write command or a read command, and this IC when read command data is output) opens the bus after this 8-bit data is output.
- With a device on the receiving (reception) side (this IC when a slave address is input for a read command or write command, and a microcomputer when data is output for a read command), SDA is set to LOW during the nine-clock cycle, and the acknowledge signal (ACK signal) is output when 8-bit data is received.
- This IC output the acknowledge signal (ACK signal) in the LOW state after a start condition and a slave address (8 bits) have been recognized.
- For other writing operations, the acknowledge signal (ACK signal) is output in the LOW state each time that 8-bit data (word address or write data) is received.
- In the various reading operations, 8-bit data (read data) is output, and then the acknowledge signal (ACK signal) in the LOW state is detected. If the acknowledge signal (ACK signal) is detected and no stop condition is sent from the master (microcomputer) side, this IC continues to output data. If the acknowledge signal (ACK signal) is not detected, this IC interrupts the transmission of data, recognizes a stop condition (stop bit), and terminates the reading operation. The IC then enters the standby mode. (Refer to "Fig. 7 acknowledge signal (ACK signal) response.")

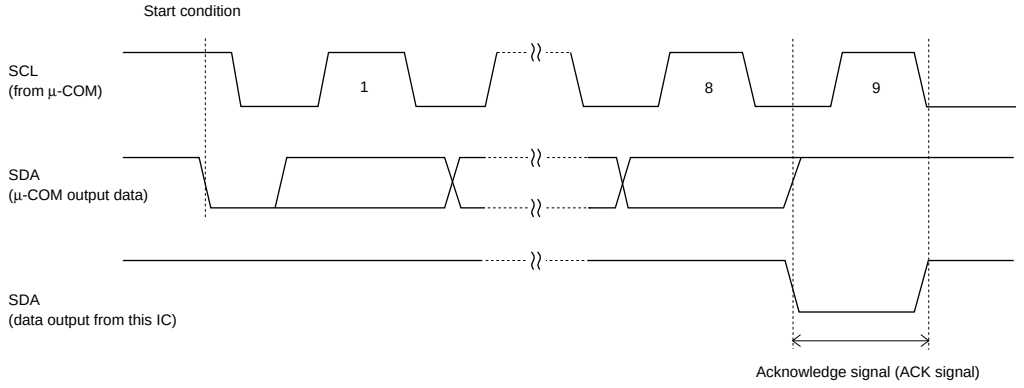


Fig. 7 Acknowledge signal (ACK signal) response

●I²C synchronous data input / output timing

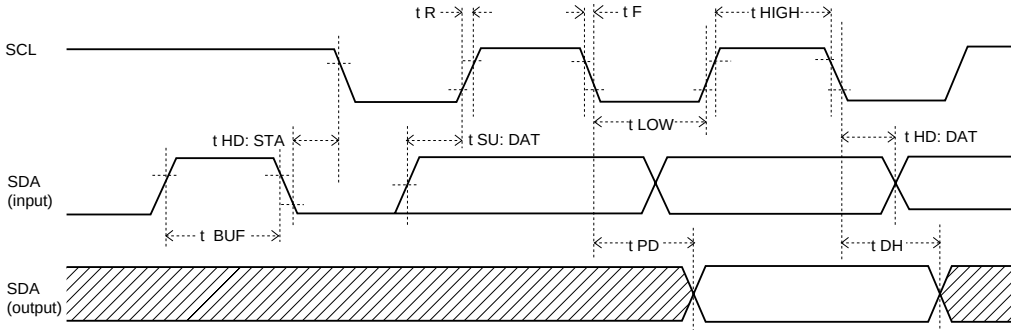


Fig. 8

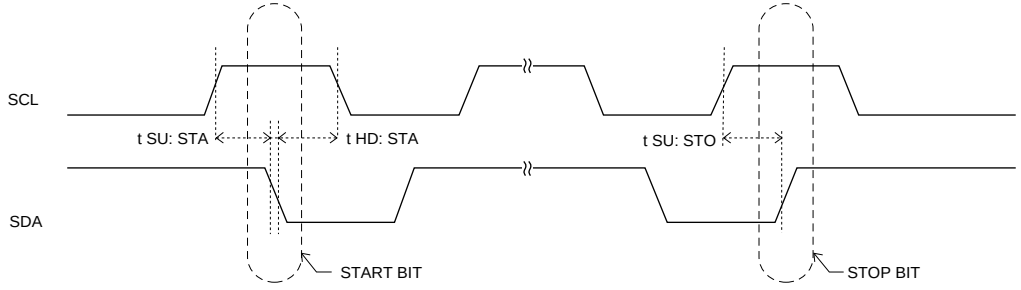


Fig. 9

- Reading of input is done at the rising edge of SCL.
- Output of data is synchronized to the falling edge of SCL.

●Write cycle timing

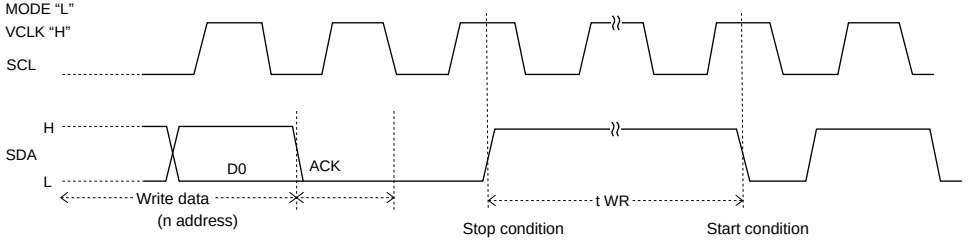


Fig. 10 Write cycle timing

●Timing charts

(1) Write cycle

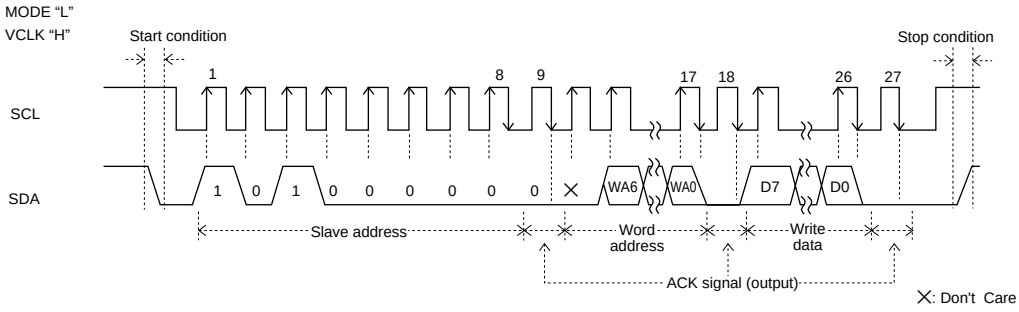


Fig. 11 Byte write cycle

1) Data is written to the address specified by the word address (n address).
2) After 8 bits of data are input, a stop bit is generated. This initiates writing of the data to the memory cell.

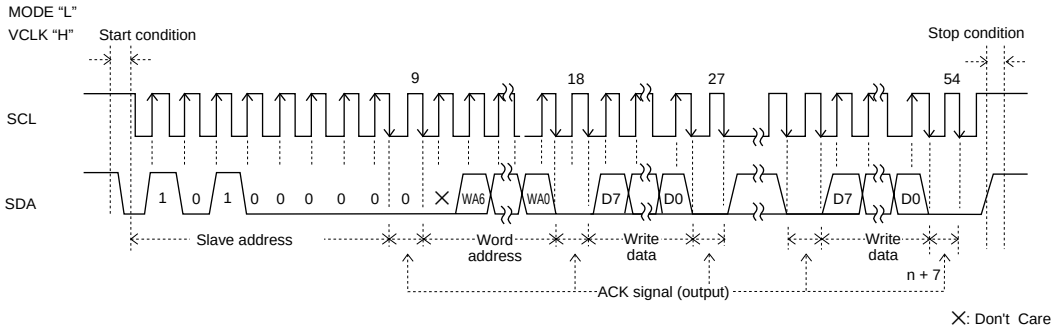


Fig. 12 Page write cycle

3) This command enables writing of 8 bytes of data.
4) This page write command is used to specify any of the first four bits (WA6 to WA3) of the word address. The address is incremented internally, and up to 8 bytes of data can be written to the last three bits (WA2 to WA0).

(2) Read cycle

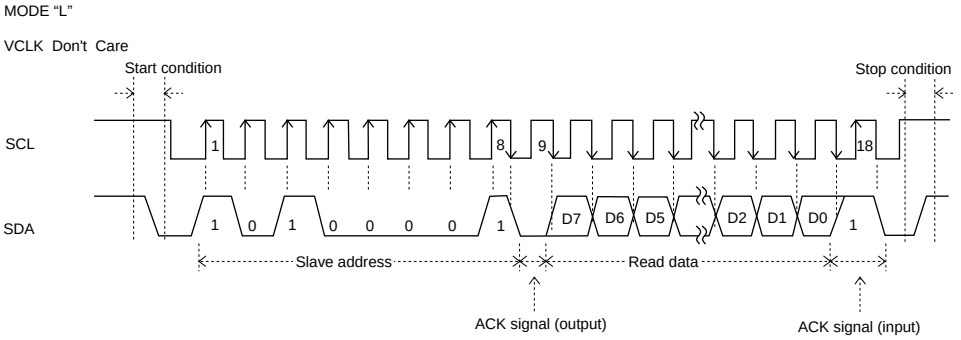


Fig. 13 Current read cycle

1) With this IC, an internal address counter circuit increments the address one address at a time, and stores in memory the last word address (n address) for which the Write or read command was executed.
2) This command reads only the data of the word address (n +1 address) following the last word address to be written after the previous command has been executed.
3) If the ACK signal LOW following D0 is detected and no stop condition is sent from the master (microcomputer) side, reading can be continued sequentially to the data of the next word address.
   [The entire 1 kilobit (128 words) can be read.]
   (Refer to "Fig. 15 Sequential read cycle.")
4) To terminate this command, HIGH is input for the ACK signal following D0, and the SDA signal rises at the HIGH state of the SCL signal (stop condition), terminating the command.

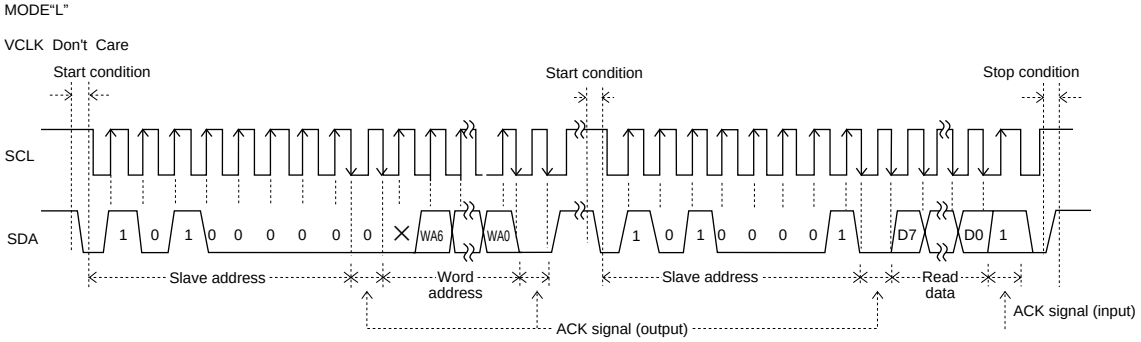


Fig. 14 Random read cycle

5) This command enables reading of the data at the specified word address.
6) If the ACK signal LOW following D0 is detected and no stop condition is sent from the master (microcomputer) side, reading can be continued sequentially to the data of the next word address.
   [The entire 1 kilobit (128 words) can be read.]
   (Refer to "Fig. 15 Sequential read cycle.")
7) To terminate this command, HIGH is input for the ACK signal following D0, and the SDA signal rises at the HIGH state of the SCL signal (stop condition), terminating the command.

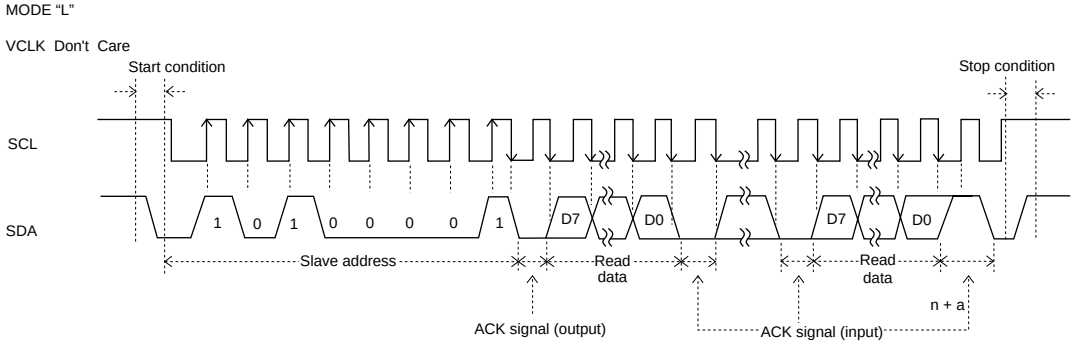


Fig. 15 Sequential read cycle
(Example: For current reading)

8) If the ACK signal LOW following D0 is detected and no stop condition is sent from the master (microcomputer) side, reading can be continued sequentially to the data of the next word address.
[The entire 1 kilobit (128 words) can be read.]
9) To terminate this command, HIGH is input for the ACK signal following any D0, and the SDA signal rises at the HIGH state of the SCL signal (stop condition), terminating the command.
10) Sequential reading is also possible with random reading.
11) With earlier ICs, switching from the DDC1 (transmit-only) mode to the DDC2 (I^2C bus) mode was possible only by turning off the power supply and then turning it on again. With the BU9881 / BU9881F, however, switching between the normal I^2C bus mode and the transmit-only mode can be done by controlling the mode pin (pin 1).

1. Controlling the mode pin (pin 1) from the main controller

As shown in the figure below, the mode pin can be controlled through the software to switch from the I^2C bus mode to the transmit-only mode.

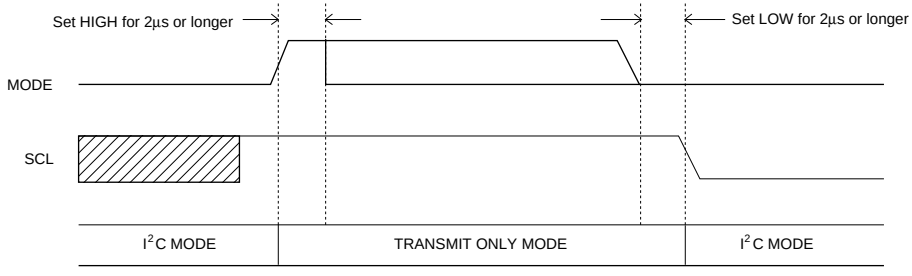


Fig. 16

2. Controlling the mode pin (pin 1) through an attachment

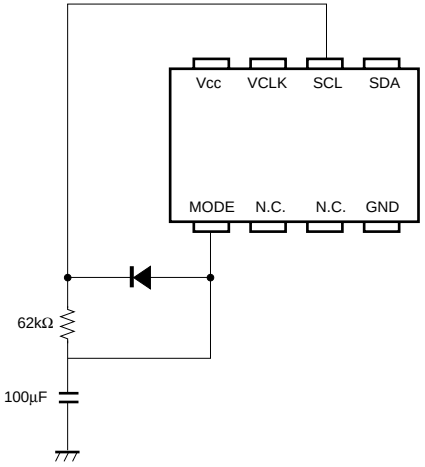
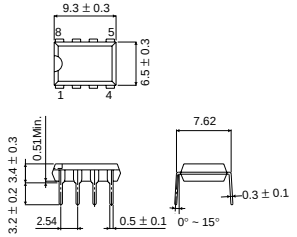


Fig.17

As shown at the left, if there is no SCL input for approximately 2 seconds (min.) to 6 seconds (max.) after the DDC2 (I^2C bus) mode has been terminated with the diode, resistor, and capacitor, the mode changes automatically to the DDC1 (transmit-only) mode.

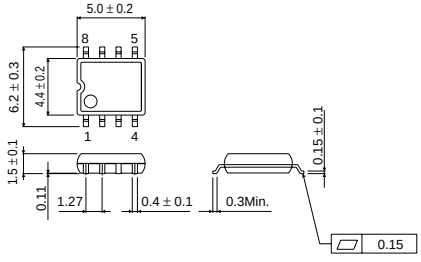
●External dimensions (Units: mm)

BU9881



DIP8

BU9881F



SOP8