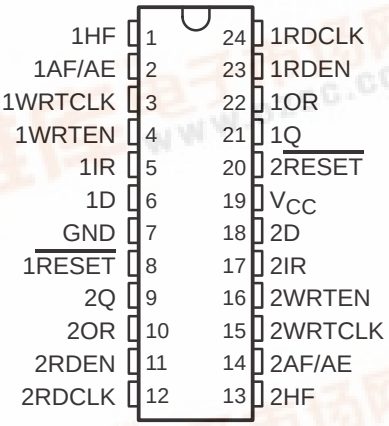
- **Dual Independent FIFOs Organized as:**
  64 Words by 1 Bit Each – SN74ACT2226
  256 Words by 1 Bit Each – SN74ACT2228
- **Free-Running Read and Write Clocks Can Be Asynchronous or Coincident on Each FIFO**
- **Input-Ready Flags Synchronized to Write Clocks**
- **Output-Ready Flags Synchronized to Read Clocks**
- **Half-Full and Almost-Full/Almost-Empty Flags**
- **Support Clock Frequencies up to 22 MHz**
- **Access Times of 20 ns**
- **Low-Power Advanced CMOS Technology**
- **Packaged in 24-Pin Small-Outline Integrated-Circuit Package**

DW PACKAGE
(TOP VIEW)



description

The SN74ACT2226 and SN74ACT2228 are dual FIFOs suited for a wide range of serial-data buffering applications, including elastic stores for frequencies up to T2 telecommunication rates. Each FIFO on the chip is arranged as 64 × 1 (SN74ACT2226) or 256 × 1 (SN74ACT2228) and has control signals and status flags for independent operation. Output flags for each FIFO include input ready (1IR or 2IR), output ready (1OR or 2OR), half full (1HF or 2HF), and almost full/almost empty (1AF/AE or 2AF/AE).

Serial data is written into a FIFO on the low-to-high transition of the write-clock (1WRTCLK or 2WRTCLK) input when the write-enable (1WRTEN or 2WRTEN) input and input-ready flag (1IR or 2IR) output are both high. Serial data is read from a FIFO on the low-to-high transition of the read-clock (1RDCLK or 2RDCLK) input when the read-enable (1RDEN or 2RDEN) input and output-ready flag (1OR or 2OR) output are both high. The read and write clocks of a FIFO can be asynchronous to one another.

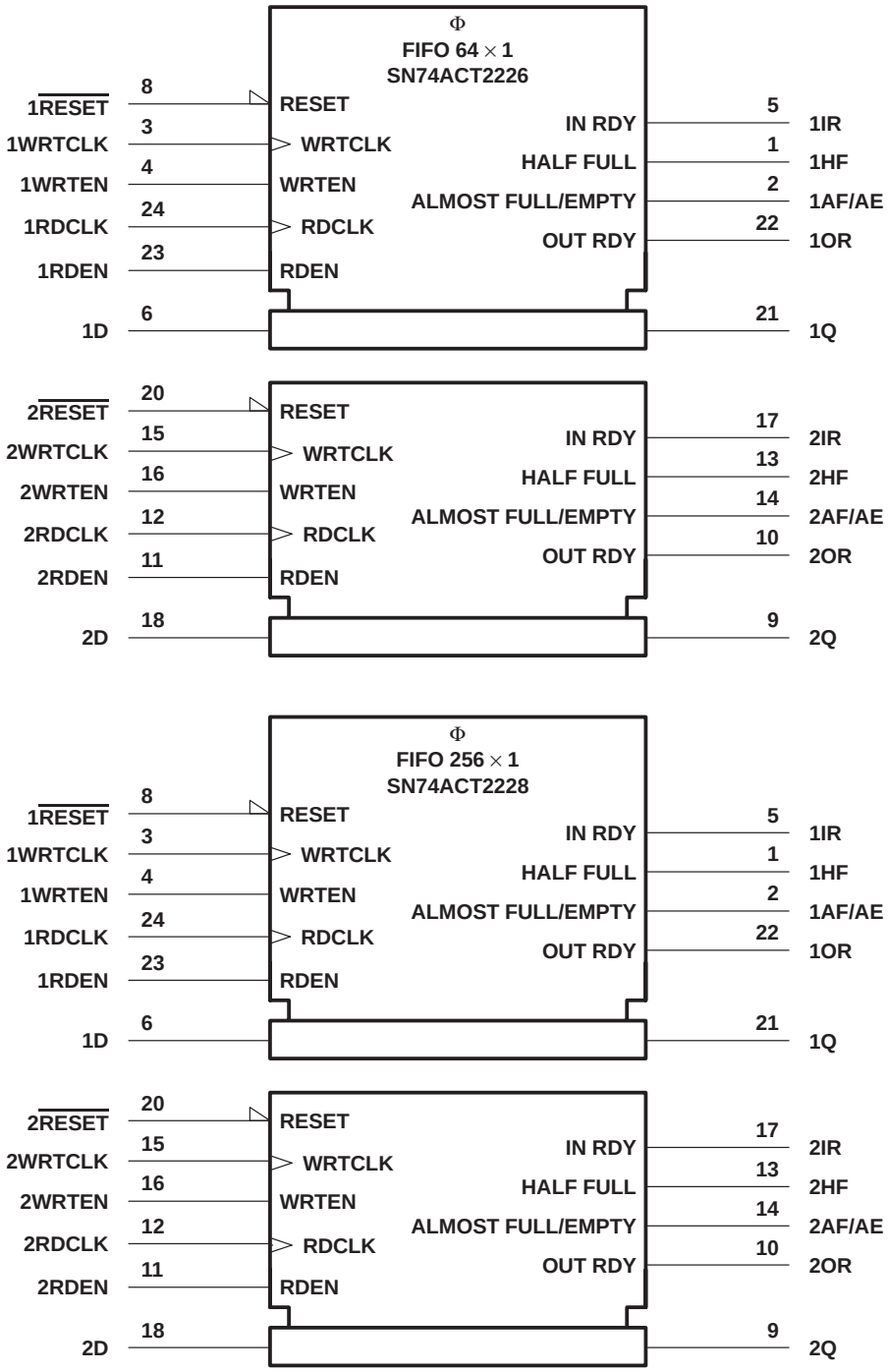
Each input-ready flag (1IR or 2IR) is synchronized by two flip-flop stages to its write clock (1WRTCLK or 2WRTCLK), and each output-ready flag (1OR or 2OR) is synchronized by three flip-flop stages to its read clock (1RDCLK or 2RDCLK). This multistage synchronization ensures reliable flag-output states when data is written and read asynchronously.

A half-full flag (1HF or 2HF) is high when the number of bits stored in its FIFO is greater than or equal to half the depth of the FIFO. An almost-full/almost-empty flag (1AF/AE or 2AF/AE) is high when eight or fewer bits are stored in its FIFO and when eight or fewer empty locations are left in the FIFO. A bit present on the data output is not stored in the FIFO.

The SN74ACT2226 and SN74ACT2228 are characterized for operation from –40°C to 85°C.

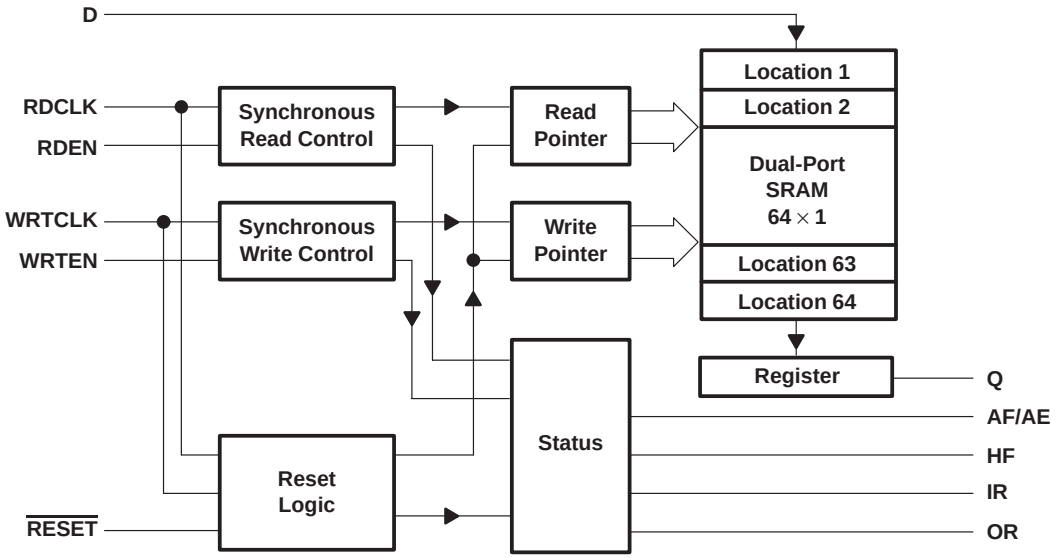
For more information on this device family, see the application report *FIFOs With a Word Width of One Bit* (literature number SCAA006).

logic symbols†

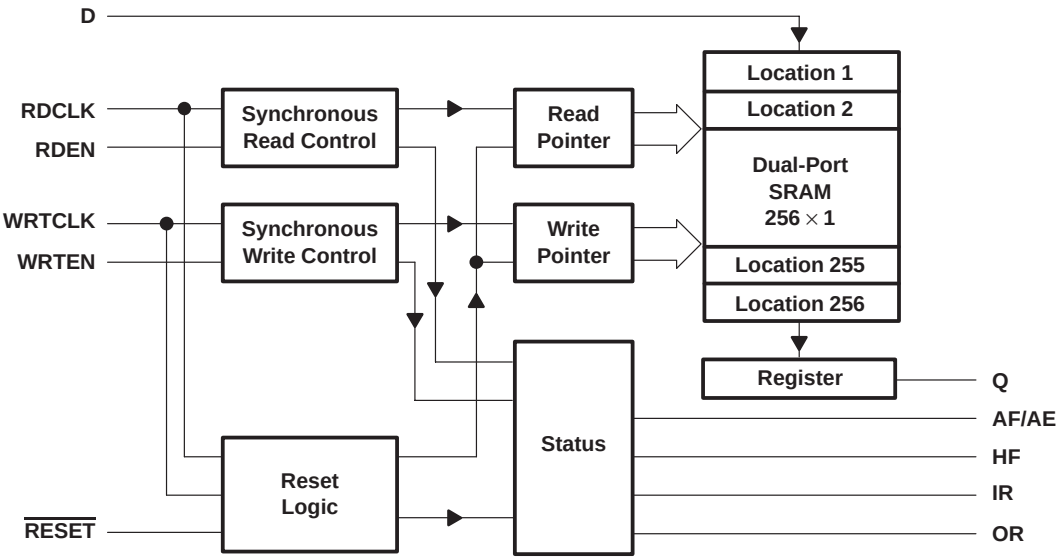


† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN74ACT2226 functional block diagram (each FIFO)



SN74ACT2228 functional block diagram (each FIFO)



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
1AF/AE 2AF/AE	2 14	O	Almost-full/almost-empty flag. AF/AE is high when the memory is eight locations or less from a full or empty state. AF/AE is set high after reset.
1D 2D	6 18	I	Data input
GND	7		Ground
1HF 2HF	1 13	O	Half-full flag. HF is high when the number of bits stored in memory is greater than or equal to half the FIFO depth. HF is set low after reset.
1IR 2IR	5 17	O	Input-ready flag. IR is synchronized to the low-to-high transition of WRTCLK. When IR is low, the FIFO is full and writes are disabled. IR is set low during reset and is set high on the second low-to-high transition of WRTCLK after reset.
1OR 2OR	22 10	O	Output-ready flag. OR is synchronized to the low-to-high transition of RDCLK. When OR is low, the FIFO is empty and reads are disabled. Ready data is present on the data output when OR is high. OR is set low during reset and set high on the third low-to-high transition of RDCLK after the first word is loaded to empty memory.
1Q 2Q	21 9	O	Data outputs. After the first valid write to empty memory, the first bit is output on the third rising edge of RDCLK. OR for the FIFO is asserted high to indicate ready data.
1RDCLK 2RDCLK	24 12	I	Read clock. RDCLK is a continuous clock and can be independent of any other clock on the device. A low-to-high transition of RDCLK reads data from memory when the FIFO RDEN and OR are high. OR is synchronous with the low-to-high transition of RDCLK.
1RDEN 2RDEN	23 11	I	Read enable. When the RDEN and OR of a FIFO are high, data is read from the FIFO on the low-to-high transition of RDCLK.
1$\overline{\text{RESET}}$ 2$\overline{\text{RESET}}$	8 20	I	Reset. To reset the FIFO, four low-to-high transitions of RDCLK and four low-to-high transitions of WRTCLK must occur while $\overline{\text{RESET}}$ is low. This sets HF, IR, and OR low and AF/AE high. Before it is used, a FIFO must be reset after power up.
V_{CC}	19		Supply voltage
1WRTCLK 2WRTCLK	3 15	I	Write clock. WRTCLK is a continuous clock and can be independent of any other clock on the device. A low-to-high transition of WRTCLK writes data to memory when WRTEN and IR are high. IR is synchronous with the low-to-high transition of WRTCLK.
1WRTEN 2WRTEN	4 16	I	Write enable. When WRTEN and IR are high, data is written to the FIFO on a low-to-high transition of WRTCLK.

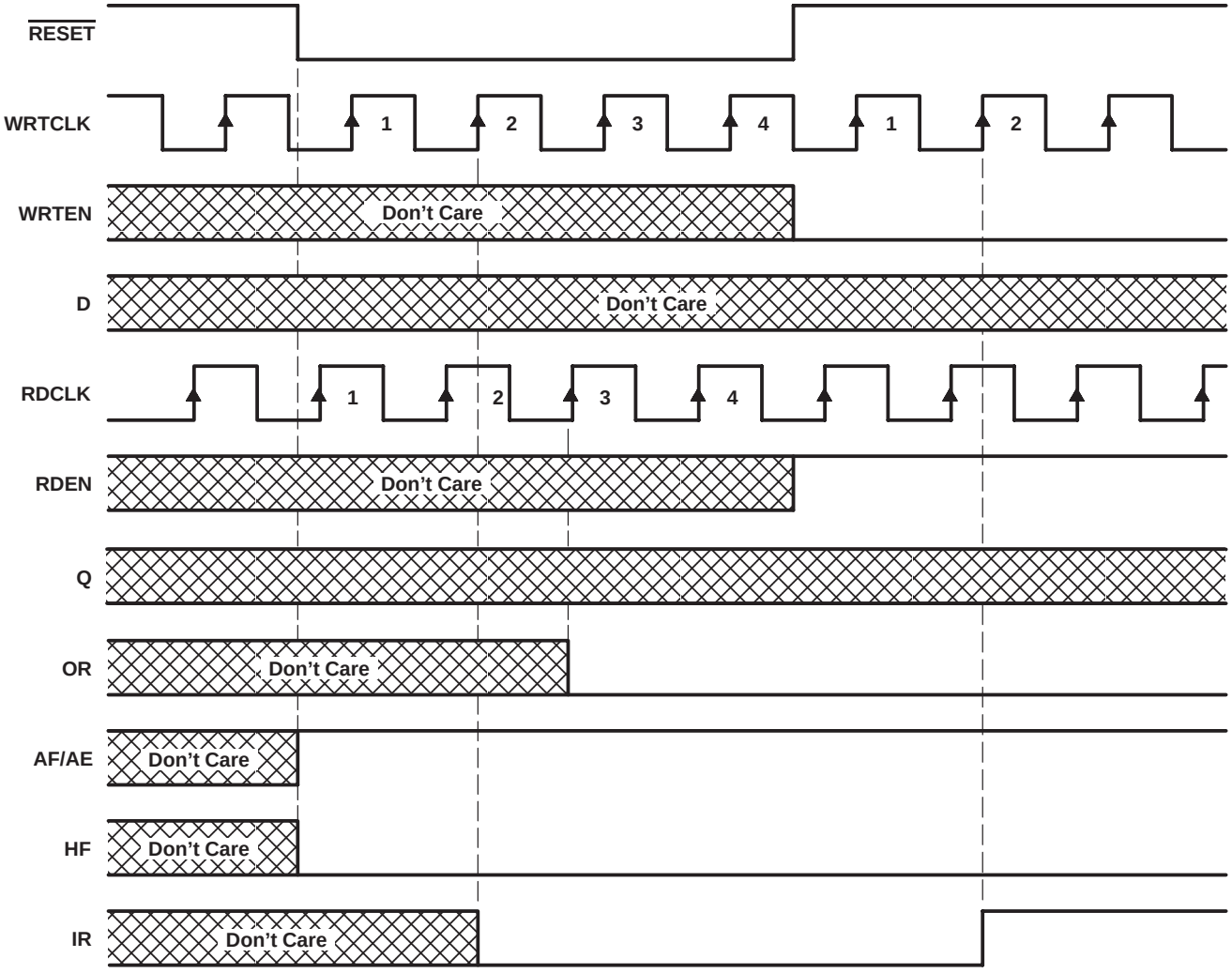
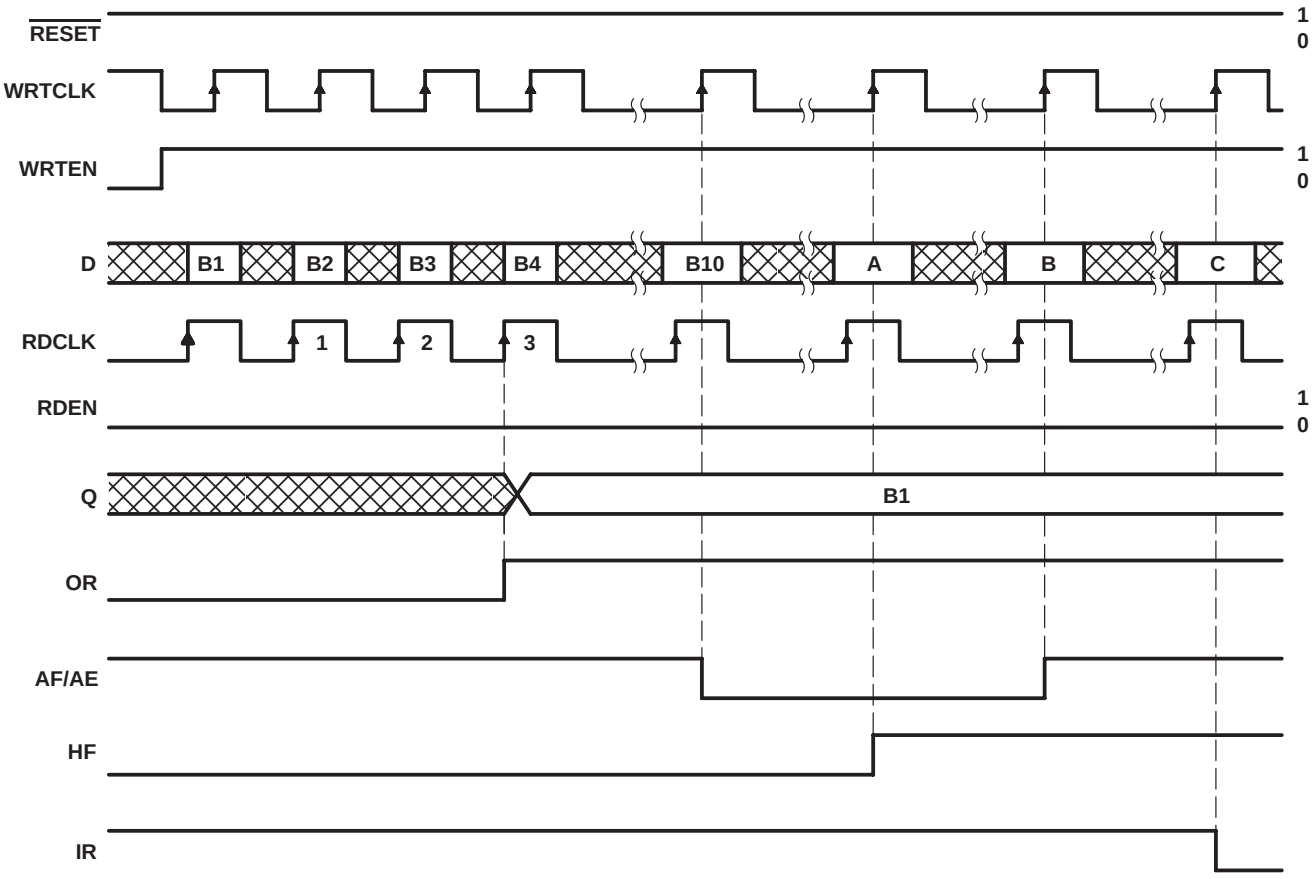


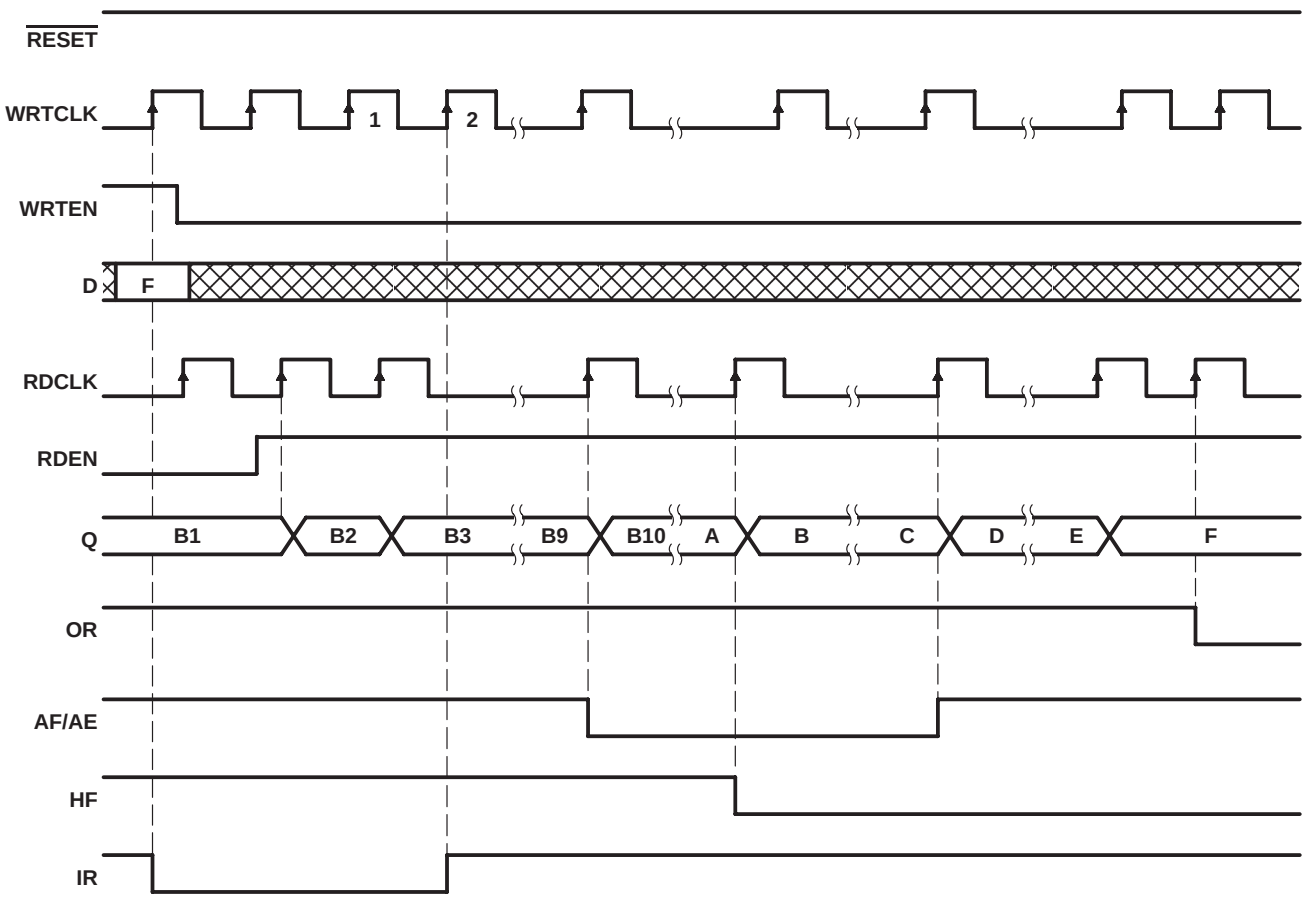
Figure 1. FIFO Reset



DATA BIT NUMBER BASED ON FIFO DEPTH

DEVICE	DATA BIT		
	A	B	C
SN74ACT2226	B33	B57	B65
SN74ACT2228	B129	B249	B257

Figure 2. FIFO Write



DATA BIT NUMBER BASED ON FIFO DEPTH

DEVICE	DATA BIT					
	A	B	C	D	E	F
SN74ACT2226	B33	B34	B56	B57	B64	B65
SN74ACT2228	B129	B130	B248	B249	B256	B257

Figure 3. FIFO Read

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND . . . . . ±200 mA
Package thermal impedance, θ_{JA} (see Note 2) . . . . . 81°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded provided that the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		4.5	5.5	V
V_{IH}	High-level input voltage		2		V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current	Q outputs, flags		–8	mA
I_{OL}	Low-level output current	Q outputs		16	mA
		Flags		8	
T_A	Operating free-air temperature		–40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = –8 mA		2.4			V
V_{OL}	Flags	V_{CC} = 4.5 V,	I_{OL} = 8 mA				0.5	V
	Q outputs	V_{CC} = 4.5 V,	I_{OL} = 16 mA				0.5	
I_I		V_{CC} = 5.5 V,	V_I = V_{CC} or 0				±5	µA
I_{OZ}		V_{CC} = 5.5 V,	V_O = V_{CC} or 0				±5	µA
I_{CC}		V_I = V_{CC} – 0.2 V or 0					400	µA
ΔI_{CC}§		V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			1	mA
C_i		V_I = 0,	f = 1 MHz			4		pF
C_o		V_O = 0,	f = 1 MHz			8		pF

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ This is the supply current when each input is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figures 1 through 3)

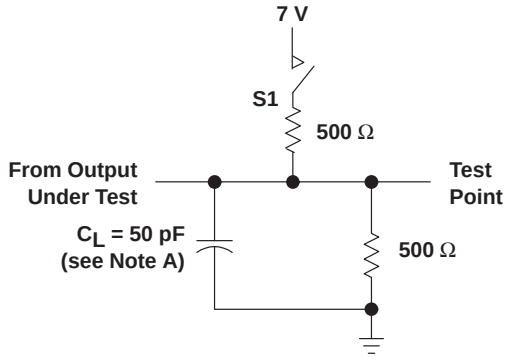
			MIN	MAX	UNIT
f_{clock}	Clock frequency			22	MHz
t_w	Pulse duration	1WRTCLK, 2WRTCLK high or low	15		ns
		1RDCLK, 2RDCLK high or low	15		
t_{su}	Setup time	1D before 1WRTCLK↑ and 2D before 2WRTCLK↑	6		ns
		1WRTEN before 1WRTCLK↑ and 2WRTEN before 2WRTCLK↑	6		
		1RDEN before 1RDCLK↑ and 2RDEN before 2RDCLK↑	6		
		1$\overline{\text{RESET}}$ low before 1WRTCLK↑ and 2$\overline{\text{RESET}}$ low before 2WRTCLK↑†	6		
		1$\overline{\text{RESET}}$ low before 1RDCLK↑ and 2$\overline{\text{RESET}}$ low before 2RDCLK↑†	6		
t_h	Hold time	1D after 1WRTCLK↑ and 2D after 2WRTCLK↑	0		ns
		1WRTEN after 1WRTCLK↑ and 2WRTEN after 2WRTCLK↑	0		
		1RDEN after 1RDCLK↑ and 2RDEN after 2RDCLK↑	0		
		1$\overline{\text{RESET}}$ low after 1WRTCLK↑ and 2$\overline{\text{RESET}}$ low after 2WRTCLK↑†	6		
		1$\overline{\text{RESET}}$ low after 1RDCLK↑ and 2$\overline{\text{RESET}}$ low after 2RDCLK↑†	6		

† Requirement to count the clock edge as one of at least four needed to reset a FIFO

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 4)

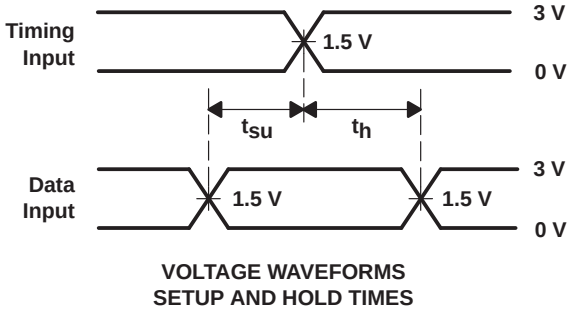
PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
f_{max}	1WRTCLK, 2WRTCLK, or 1RDCLK, 2RDCLK		22		MHz
t_{pd}	1RDCLK↑, 2RDCLK↑	1Q, 2Q	2	20	ns
	1WRTCLK↑, 2WRTCLK↑	1IR, 2IR	1	20	
	1RDCLK↑, 2RDCLK↑	1OR, 2OR	1	20	
	1WRTCLK↑, 2WRTCLK↑	1AF/AE, 2AF/AE	3	20	
	1RDCLK↑, 2RDCLK↑		3	20	
t_{PLH}	1WRTCLK↑, 2WRTCLK↑	1HF, 2HF	2	20	ns
t_{PHL}	1RDCLK↑, 2RDCLK↑		3	20	
t_{PLH}	1$\overline{\text{RESET}}$, 2$\overline{\text{RESET}}$ low	1AF/AE, 2AF/AE	1	20	ns
t_{PHL}		1HF, 2HF	1	20	

PARAMETER MEASUREMENT INFORMATION

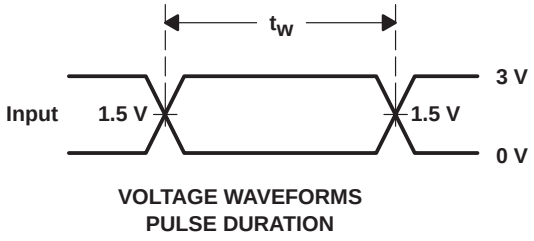


LOAD CIRCUIT

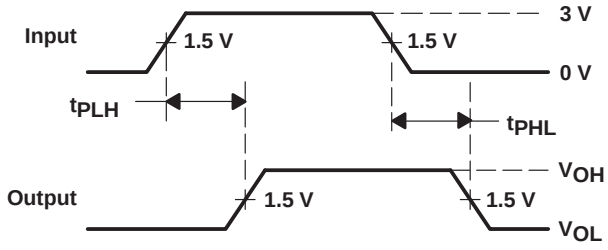
PARAMETER		S1
t_{en}	t_{PZH}	Open
	t_{PZL}	Closed
t_{dis}	t_{PHZ}	Open
	t_{PLZ}	Closed
t_{pd}	t_{PLH}	Open
	t_{PHL}	Open



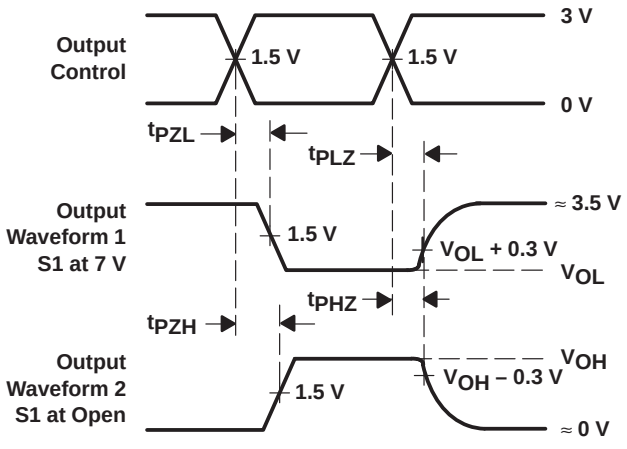
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTE A: C_L includes probe and jig capacitance.

Figure 4. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

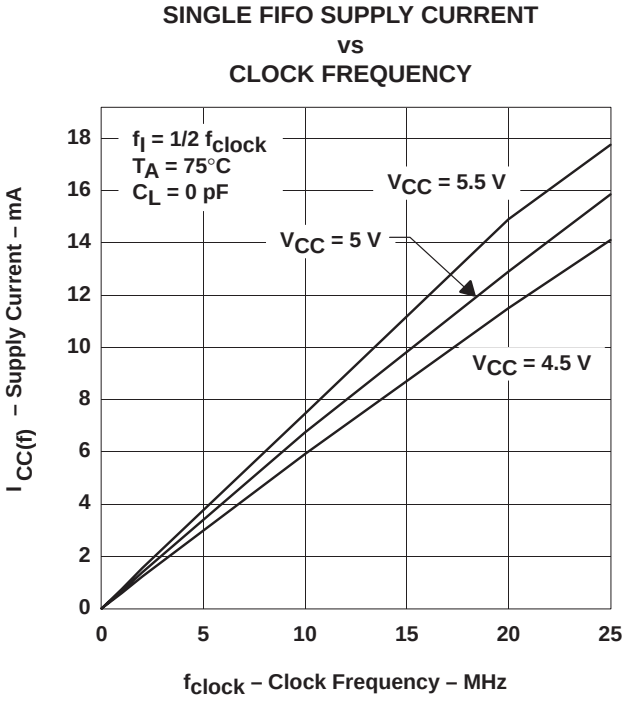


Figure 5

calculating power dissipation

Data for Figure 5 is taken with one FIFO active and one FIFO idle on the device. The active FIFO has both writes and reads enabled with its read clock (RDCLK) and write clock (WRTCLK) operating at the rate specified by f_{clock}. The data input rate and data output rate are half the f_{clock} rate, and the data output is disconnected. A close approximation of the total device power can be found by using Figure 5, determining the capacitive load on the data output and determining the number of SN74ACT2226/2228 inputs driven by TTL high levels.

With $I_{CC(f)}$ taken from Figure 5, the maximum power dissipation (P_T) of one FIFO on the SN74ACT2226 or SN74ACT2228 can be calculated by:

$$P_T = V_{CC} \times [I_{CC(f)} + (N \times \Delta I_{CC} \times dc)] + (C_L \times V_{CC}^2 \times f_o)$$

where:

- N = number of inputs driven by TTL levels
- ΔI_{CC} = increase in power-supply current for each input at a TTL high level
- dc = duty cycle of inputs at a TTL high level of 3.4 V
- C_L = output capacitive load
- f_o = switching frequency of an output

APPLICATION INFORMATION

An example of concentrating two independent serial-data signals into a single composite data signal with the use of an SN74ACT2226 or SN74ACT2228 device is shown in Figure 6. The input data to the FIFOs share the same average (mean) frequency and the mean frequency of the SYS_CLOCK is greater than or equal to the sum of the individual mean input rates. A single-bit FIFO is needed for each additional input data signal that is time-division multiplexed into the composite signal.

The FIFO memories provide a buffer to absorb clock jitter generated by the transmission systems of incoming signals and synchronize the phase-independent inputs to one another. FIFO half-full (HF) flags are used to signal the multiplexer to start fetching data from the buffers. The state of the flags also can be used to indicate when a FIFO read should be suppressed to regulate the output flow (pulse-stuffing control). The FIFO almost-full/almost-empty (AF/AE) flags can be used in place of the half-full flags to reduce transmission delay.

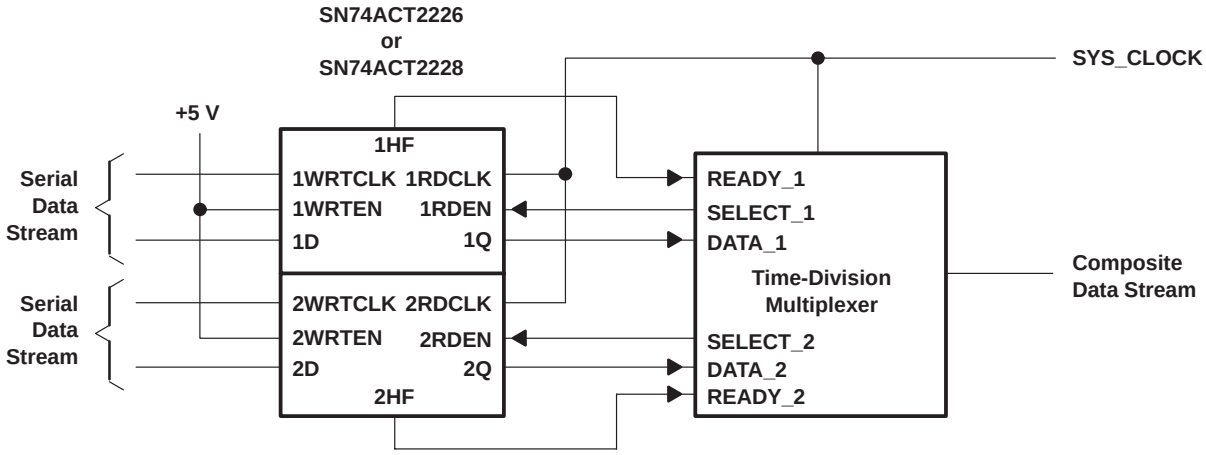


Figure 6. Time-Division Multiplexing Using the SN74ACT2226 or SN74ACT2228

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