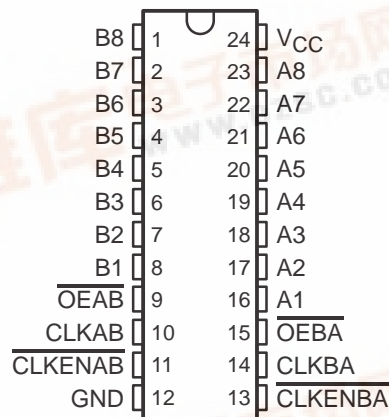


SN74LVC2952 OCTAL BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

SCAS311A – JANUARY 1993 – REVISED JULY 1995

- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce) $< 0.8\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) $> 2\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

DB, DW, OR PW PACKAGE
(TOP VIEW)

description

This octal bus transceiver and register is designed for 2.7-V to 3.6-V V_{CC} operation; it can interface to a 5-V system environment.

The SN74LVC2952 consists of two 8-bit back-to-back registers that store data flowing in both directions between two bidirectional buses. Data on the A or B bus is stored in the registers on the low-to-high transition of the clock ($\overline{\text{CLKAB}}$ or $\overline{\text{CLKBA}}$) input provided that the clock-enable ($\overline{\text{CLKENAB}}$ or $\overline{\text{CLKENBA}}$) input is low. Taking the output-enable ($\overline{\text{OEAB}}$ or $\overline{\text{OEBA}}$) input low accesses the data on either port.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVC2952 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE†

INPUTS				OUTPUT
$\overline{\text{CLKENAB}}$	$\overline{\text{CLKAB}}$	$\overline{\text{OEAB}}$	A	B
H	X	L	X	B_0^\ddagger
X	H or L	L	X	B_0^\ddagger
L	↑	L	L	L
L	↑	L	H	H
X	X	H	X	Z

† A-to-B data flow is shown; B-to-A data flow is similar but uses $\overline{\text{CLKENBA}}$, $\overline{\text{CLKBA}}$, and $\overline{\text{OEBA}}$.

‡ Level of B before the indicated steady-state input conditions were established

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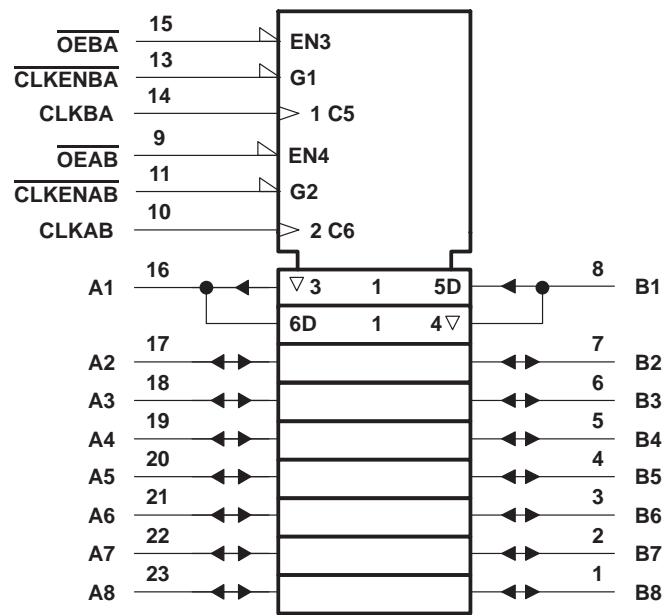


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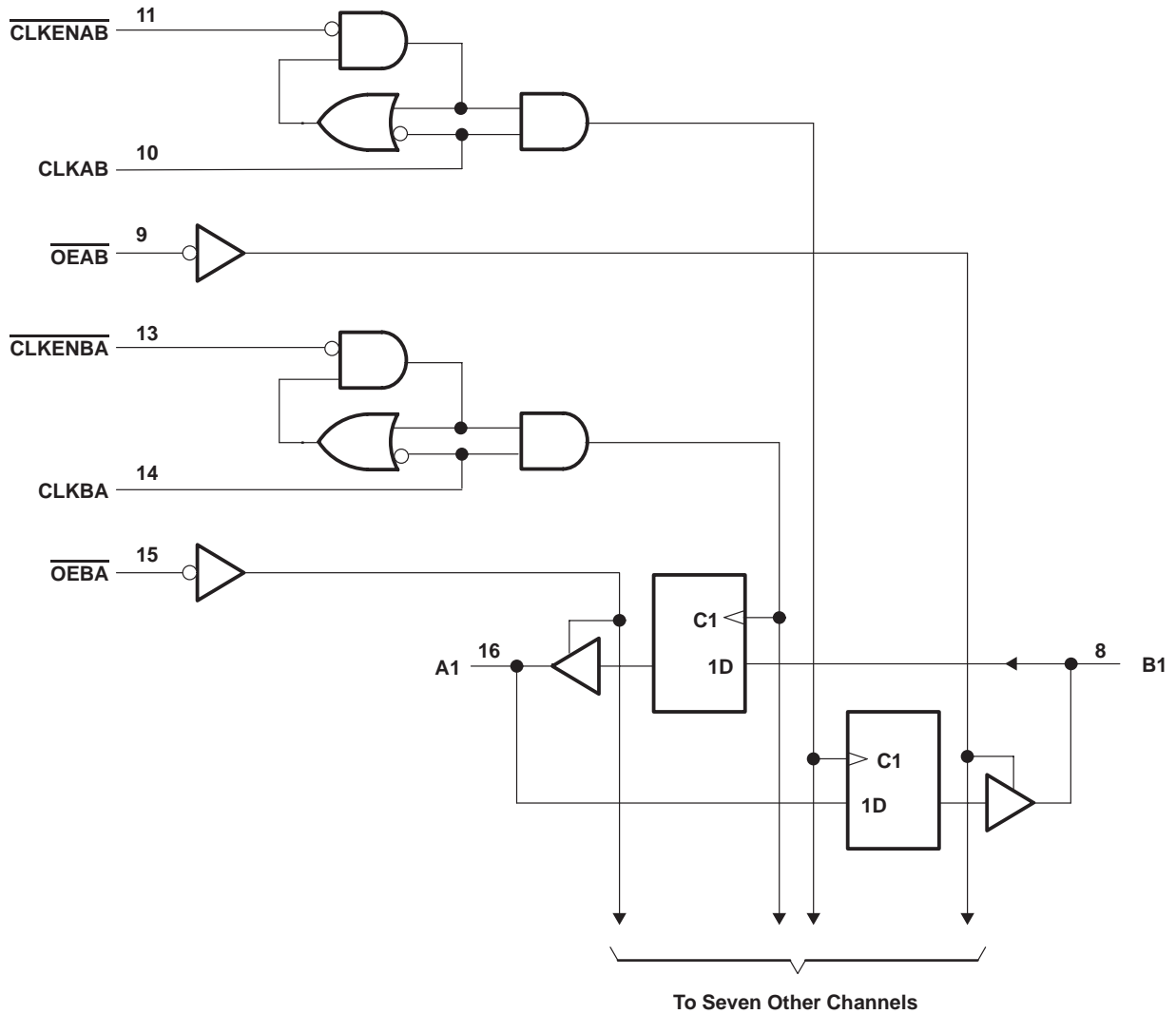
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high impedance state or power off state, V_O (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 3): DB package	0.65 W
DW package	1.7 W
PW package	0.7 W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	2	3.6
		Data retention only	1.5	
V_{IH}	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V	2	V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V	0.8	V
V_I	Input voltage	0	5.5	V
V_O	Output voltage	High or low state	0	V_{CC}
		3 state	0	5.5
I_{OH}	High-level output current	$V_{CC} = 2.7$ V	–12	mA
		$V_{CC} = 3$ V	–24	
I_{OL}	Low-level output current	$V_{CC} = 2.7$ V	12	mA
		$V_{CC} = 3$ V	24	
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	–40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC} [†]	MIN	TYP [‡]	MAX	UNIT
V _{OH}		I _{OH} = – 100 μA	MIN to MAX	V _{CC} –0.2		V	
		I _{OH} = – 12 mA	2.7 V	2.2			
			3 V	2.4			
		I _{OH} = – 24 mA	3 V	2.2			
V _{OL}		I _{OL} = 100 μA	MIN to MAX	0.2		V	
		I _{OL} = 12 mA	2.7 V	0.4			
		I _{OL} = 24 mA	3 V	0.55			
I _I		V _I = 5.5 V or GND	3.6 V	±5		μA	
I _{OZ} [§]		V _O = 5.5 V or GND	3.6 V	±10		μA	
I _{CC}		V _I = V _{CC} or GND, I _O = 0	3.6 V	20		μA	
ΔI _{CC}		One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V	500		μA	
C _i	Control inputs	V _I = V _{CC} or GND	3.3 V			pF	
C _{io}	A or B ports	V _O = V _{CC} or GND	3.3 V			pF	

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

[‡] All typical values are measured at V_{CC} = 3.3 V, T_A = 25°C.

[§] For I/O ports, the parameter I_{OZ} includes the input leakage current.

PRODUCT PREVIEW

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