SN54ABT5400, SN74ABT5400
11-BIT LINE/MEMORY DRIVERS
WITH 3-STATE OUTPUTS

SCBS094B – DECEMBER 1991 – JULY 1994

- **Output Ports Have 25-Ω Series Resistors, So No External Resistors Are Required**
- **State-of-the-Art *EPIC-*II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **Typical V_{OLV} (Output Undershoot) < 0.5 V at V_{CC} = 5 V, T_A = 25°C**
- **Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK) and DIPs (JT)**

SN54ABT5400 . . . JT PACKAGE
SN74ABT5400 . . . DW PACKAGE
(TOP VIEW)

```
        Y1   [ 1    28 ]  D1
        Y2   [ 2    27 ]  D2
        Y3   [ 3    26 ]  D3
        Y4   [ 4    25 ]  D4
        Y5   [ 5    24 ]  D5
        Y6   [ 6    23 ]  D6
       GND   [ 7    22 ]  VCC
       GND   [ 8    21 ]  VCC
        Y7   [ 9    20 ]  D7
        Y8   [ 10   19 ]  D8
        Y9   [ 11   18 ]  D9
       Y10   [ 12   17 ]  D10
       Y11   [ 13   16 ]  D11
       OE1   [ 14   15 ]  OE2
```

SN54ABT5400 . . . FK PACKAGE
(TOP VIEW)

```
            D4  D5  D6 VCC VCC D7  D8
             4   3   2   1  28  27  26
      D3  [ 5                        25 ]  D9
      D2  [ 6                        24 ]  D10
      D1  [ 7                        23 ]  D11
      Y1  [ 8                        22 ]  OE2
      Y2  [ 9                        21 ]  OE1
      Y3  [ 10                       20 ]  Y11
      Y4  [ 11                       19 ]  Y10
             12  13  14  15  16  17  18
             Y5  Y6 GND GND  Y7  Y8  Y9
```

description

These 11-bit buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.
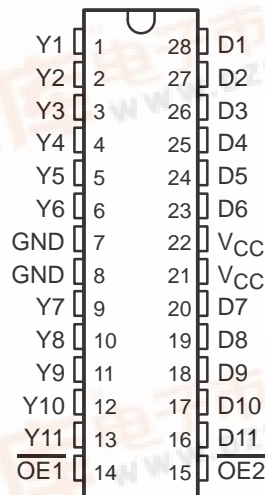
The 3-state control gate is a 2-input AND gate with active-low inputs so if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all 11 outputs are in the high-impedance state.

The outputs, which are designed to source or sink up to 12 mA, include 25-Ω series resistors to reduce overshoot and undershoot.
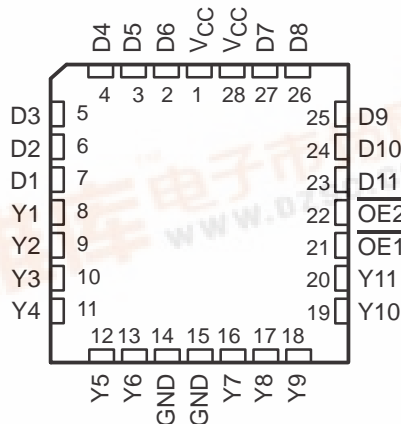
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT5400 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ABT5400 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	D	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

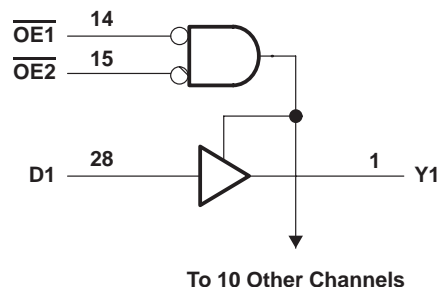**TEXAS INSTRUMENTS**

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SN54ABT5400, SN74ABT5400
11-BIT LINE/MEMORY DRIVERS
WITH 3-STATE OUTPUTS

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logic symbol†

$\overline{OE1}$	14	
$\overline{OE2}$	15	

& EN

D1	28	1	1	Y1
D2	27		2	Y2
D3	26		3	Y3
D4	25		4	Y4
D5	24		5	Y5
D6	23		6	Y6
D7	20		9	Y7
D8	19		10	Y8
D9	18		11	Y9
D10	17		12	Y10
D11	16		13	Y11

† This symbol is in accordance with ANSI/IEEE Std 91-1984
  and IEC Publication 617-12.
Pin numbers shown are for the DW and JT packages.

logic diagram (positive logic)

$\overline{OE1}$	14
$\overline{OE2}$	15

D1	28	1	Y1

To 10 Other Channels

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} .... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) .... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O .... −0.5 V to 5.5 V
Current into any output in the low state, I_O .... 30 mA
Input clamp current, I_{IK} (V_I < 0) .... −18 mA
Output clamp current, I_{OK} (V_O < 0) .... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DW package .... 1.2 W
Storage temperature range .... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
  functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
  implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
       2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
          For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology
          Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 2)

			SN54ABT5400		SN74ABT5400		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−12		−12	mA
I_{OL}	Low-level output current			12		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 3: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			$T_A = 25°C$			SN54ABT5400		SN74ABT5400		UNIT
				MIN	TYP[†]	MAX	MIN	MAX	MIN	MAX	
V_{IK}	$V_{CC} = 4.5$ V,	$I_I = -18$ mA				−1.2		−1.2		−1.2	V
V_{OH}	$V_{CC} = 4.5$ V,	$I_{OH} = -1$ mA		3.35	3.7		3.3		3.35		V
	$V_{CC} = 5$ V,	$I_{OH} = -1$ mA		3.85	4.2		3.8		3.85		
	$V_{CC} = 4.5$ V	$I_{OH} = -3$ mA					3		3.1		
		$I_{OH} = -12$ mA		2.6					2.6		
V_{OL}	$V_{CC} = 4.5$ V	$I_{OL} = 8$ mA						0.8		0.65	V
		$I_{OL} = 12$ mA								0.8	
I_I	$V_{CC} = 5.5$ V,	$V_I = V_{CC}$ or GND				±1		±1		±1	µA
I_{OZH}	$V_{CC} = 5.5$ V,	$V_O = 2.7$ V				50		50		50	µA
I_{OZL}	$V_{CC} = 5.5$ V,	$V_O = 0.5$ V				−50		−50		−50	µA
I_{off}	$V_{CC} = 0$,	V_I or $V_O \leq 4.5$ V				±100				±100	µA
I_{CEX}	$V_{CC} = 5.5$ V,	$V_O = 5.5$ V	Outputs high			50		50		50	µA
I_O	$V_{CC} = 5.5$ V,	$V_O = 2.5$ V		−25	−45	−100	−25	−100	−25	−100	mA
I_{OS}[‡]	$V_{CC} = 5.5$ V,	$V_O = 0$		−50		−200	−50	−200	−50	−200	mA
I_{CC}	$V_{CC} = 5.5$ V, $I_O = 0$, $V_I = V_{CC}$ or GND		Outputs high		5	50		50		50	µA
			Outputs low		36	45		45		45	mA
			Outputs disabled		1	50		50		50	µA
ΔI_{CC}[§]	$V_{CC} = 5.5$ V, One input at 3.4 V, Other inputs at V_{CC} or GND	Data inputs	Outputs enabled			1.5		1.5		1.5	mA
			Outputs disabled			0.05		0.05		0.05	
		Control inputs				1.5		1.5		1.5	
C_i	$V_I = 2.5$ V or 0.5 V				3						pF
C_o	$V_O = 2.5$ V or 0.5 V				8						pF

[†] All typical values are at $V_{CC} = 5$ V.
[‡] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
[§] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

TEXAS INSTRUMENTS

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT5400		SN74ABT5400		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Y	2	4.5	5.7	2	6.7	2	6.5	ns
t_{PHL}			1.5	3.7	4.5	1.5	5.5	1.5	5.2	
t_{PZH}	$\overline{OE}$	Y	2.5	5.7	6.6	2.5	8.6	2.5	8.5	ns
t_{PZL}			2	4.4	5.5	2	6.9	2	6.8	
t_{PHZ}	$\overline{OE}$	Y	1.5	3.6	4.4	1.5	5.5	1.5	5.2	ns
t_{PLZ}			1.5	4.2	5.4	1.5	7.4	1.5	6.9	

TEXAS
INSTRUMENTS

PARAMETER MEASUREMENT INFORMATION
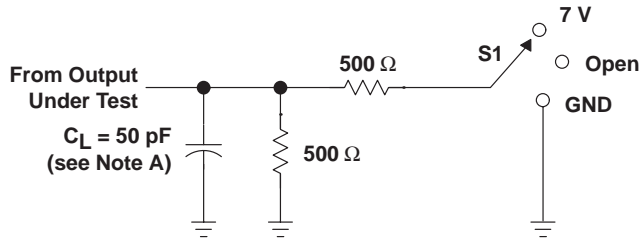
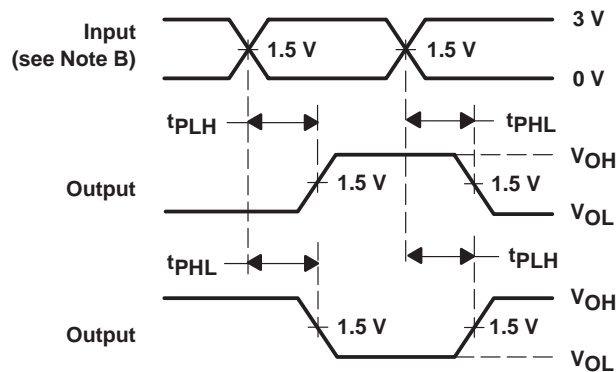**LOAD CIRCUIT FOR OUTPUTS**

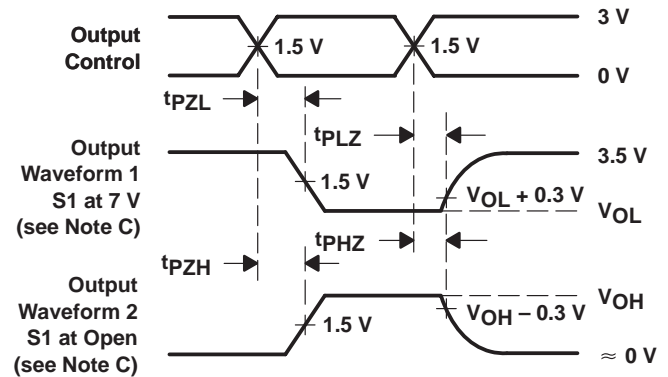| TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open
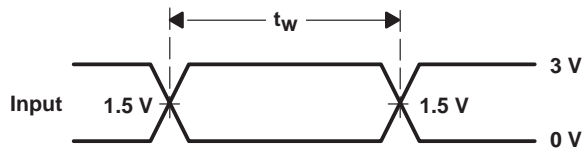
**VOLTAGE WAVEFORMS
PULSE DURATION**
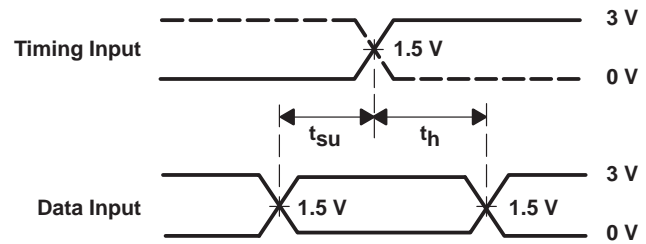
**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**

**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS**

**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING**

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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