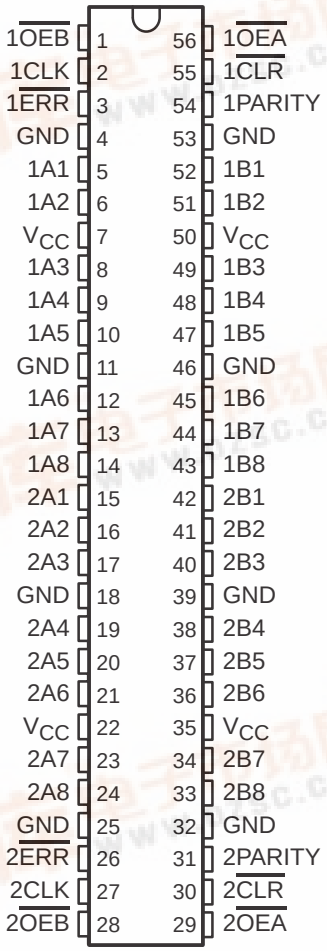
# SN54ABT16833, SN74ABT16833
# DUAL 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

SCBS097D – FEBRUARY 1991 – REVISED JANUARY 1997

- Members of the Texas Instruments *Widebus*™ Family
- State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical $V_{OLP}$ (Output Ground Bounce) < 1 V at $V_{CC}$ = 5 V, $T_A$ = 25°C
- Distributed $V_{CC}$ and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs (–32-mA $I_{OH}$, 64-mA $I_{OL}$)
- Parity-Error Flag With Parity Generator/Checker
- Register for Storage of Parity-Error Flag
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

**SN54ABT16833 . . . WD PACKAGE**
**SN74ABT16833 . . . DGG OR DL PACKAGE**
**(TOP VIEW)**




## description

The ’ABT16833 consist of two noninverting 8-bit to 9-bit parity bus transceivers and are designed for communication between data buses. For each transceiver, when data is transmitted from the A bus to the B bus, an odd-parity bit is generated and output on the parity I/O pin (1PARITY or 2PARITY). When data is transmitted from the B bus to the A bus, 1PARITY (or 2PARITY) is configured as an input and combined with the B-input data to generate an active-low error flag if odd parity is not detected.

The error (1$\overline{\text{ERR}}$ or 2$\overline{\text{ERR}}$) output is configured as an open-collector output. The B-to-A parity-error flag is clocked into 1$\overline{\text{ERR}}$ (or 2$\overline{\text{ERR}}$) on the low-to-high transition of the clock (1CLK or 2CLK) input. 1$\overline{\text{ERR}}$ (or 2$\overline{\text{ERR}}$) is cleared (set high) by taking the clear (1$\overline{\text{CLR}}$ or 2$\overline{\text{CLR}}$) input low.

The output-enable ($\overline{\text{OEA}}$ and $\overline{\text{OEB}}$) inputs can be used to disable the device so that the buses are effectively isolated. When both $\overline{\text{OEA}}$ and $\overline{\text{OEB}}$ are low, data is transferred from the A bus to the B bus and inverted parity is generated. Inverted parity is a forced error condition that gives the designer more system diagnostic capability.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

## description (continued)

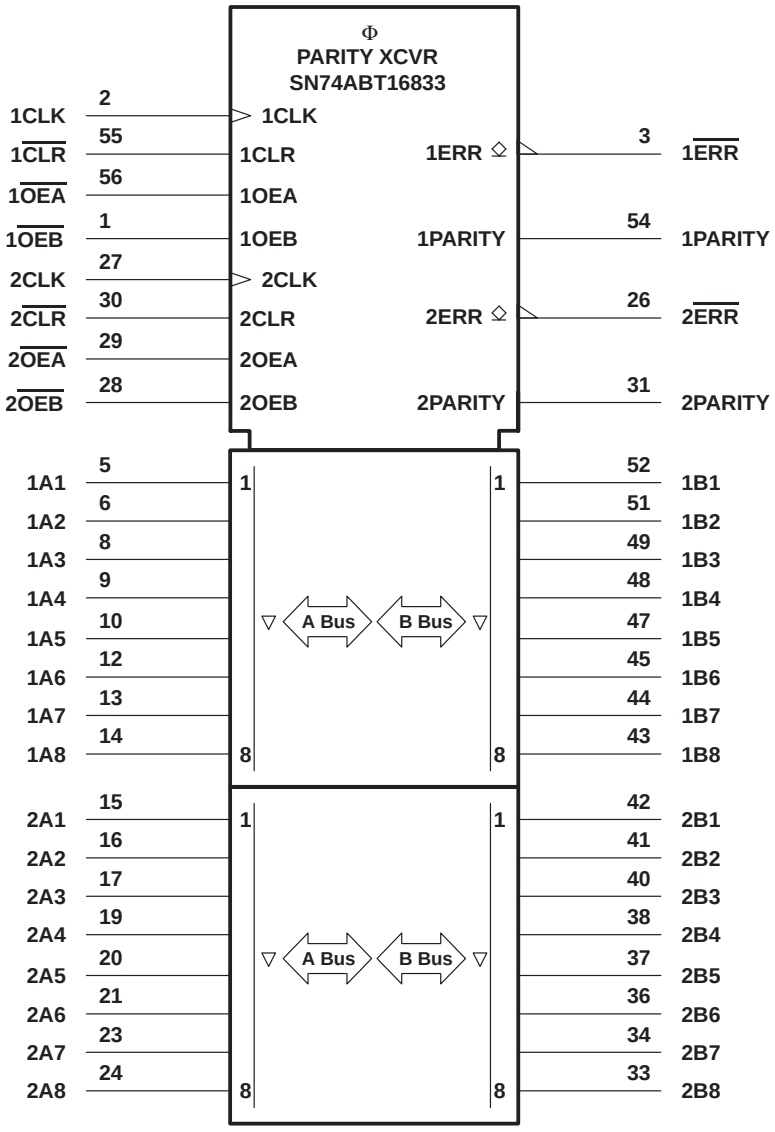
The SN54ABT16833 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT16833 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**

| INPUTS | | | | | | OUTPUT AND I/O | | | | FUNCTION |
|---|---|---|---|---|---|---|---|---|---|---|
| $\overline{OEB}$ | $\overline{OEA}$ | $\overline{CLR}$ | CLK | Ai<br>Σ OF H | Bi†<br>Σ OF H | A | B | PARITY | $\overline{ERR}$‡ | |
| L | H | X | X | Odd<br>Even | NA | NA | A | L<br>H | NA | A data to B bus and generate parity |
| H | L | H | ↑ | NA | Odd<br>Even | B | NA | NA | H<br>L | B data to A bus and check parity |
| X | X | L | X | X | X | X | NA | NA | H | Check error-flag register |
| H | H | H<br>L<br>H<br>H | No↑<br>No↑<br>↑<br>↑ | X<br>X<br>Odd<br>Even | X | Z | Z | Z | NC<br>H<br>H<br>L | Isolation§ |
| L | L | X | X | Odd<br>Even | NA | NA | A | H<br>L | NA | A data to B bus and generate inverted parity |

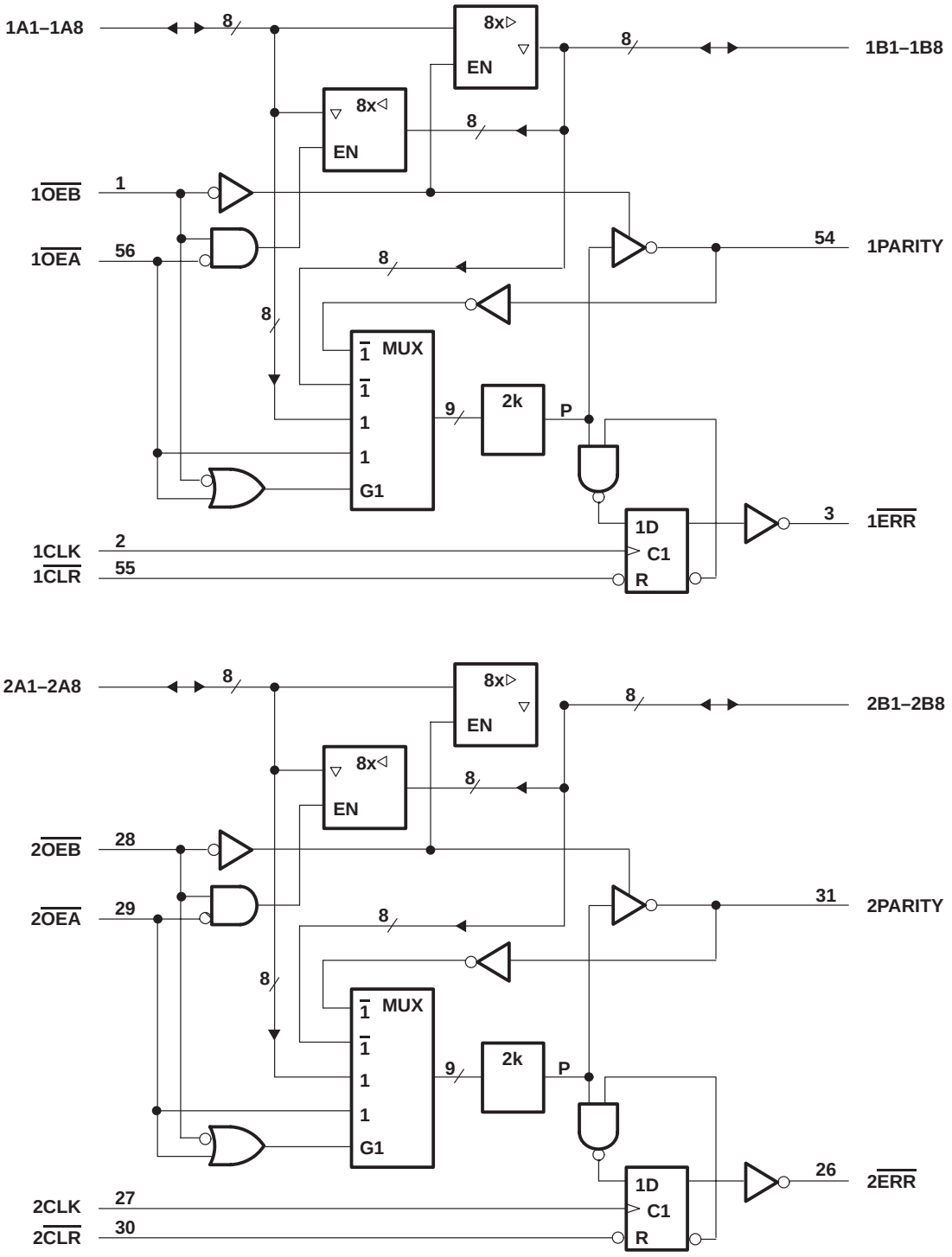
NA = not applicable, NC = no change, X = don't care
† Summation of high-level inputs includes PARITY along with Bi inputs.
‡ Output states shown assume $\overline{ERR}$ was previously high.
§ In this mode, $\overline{ERR}$ (when clocked) shows inverted parity of the A bus.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)

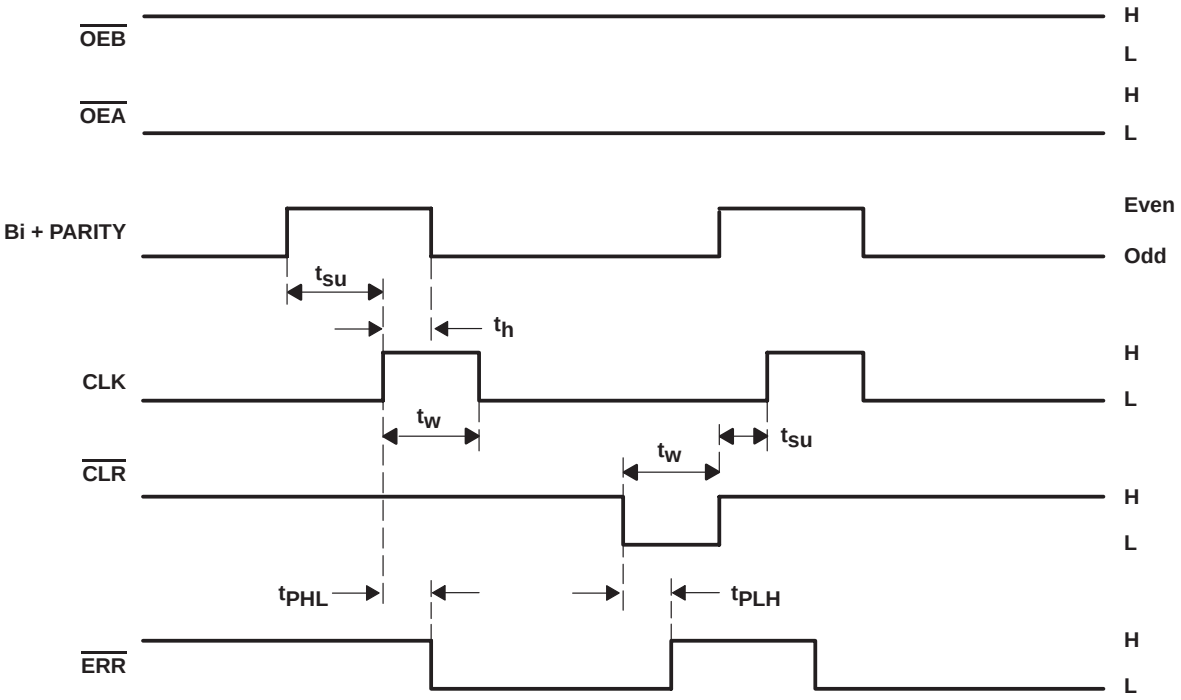


**ERROR-FLAG FUNCTION TABLE**

| INPUTS | | INTERNAL TO DEVICE | OUTPUT PRE-STATE | OUTPUT $\overline{ERR}$ | FUNCTION |
|---|---|---|---|---|---|
| $\overline{CLR}$ | CLK | POINT P | $\overline{ERR}_{n-1}$† | | |
| H | ↑ | H | H | H | Sample |
| H | ↑ | X | L | L | |
| H | ↑ | L | X | L | |
| L | X | X | X | H | Clear |

† State of $\overline{ERR}$ before changes at $\overline{CLR}$, CLK, or point P

## error-flag waveforms



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 7 V
Input voltage range, $V_I$ (except I/O ports) (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, $V_O$ . . . . . –0.5 V to 5.5 V
Current into any output in the low state, $I_O$: SN54ABT16833 . . . . . 96 mA
SN74ABT16833 . . . . . 128 mA
Input clamp current, $I_{IK}$ ($V_I$ < 0) . . . . . –18 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0) . . . . . –50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DGG package . . . . . 81°C/W
DL package . . . . . 74°C/W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

### recommended operating conditions (see Note 3)

| | | | SN54ABT16833 | | SN74ABT16833 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $V_{OH}$ | High-level output voltage | $\overline{ERR}$ | | 5.5 | | 5.5 | V |
| $I_{OH}$ | High-level output current | Except $\overline{ERR}$ | | –24 | | –32 | mA |
| $I_{OL}$ | Low-level output current | | | 48 | | 64 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | Outputs enabled | | 10 | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused pins (input or I/O) must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $T_A$ = 25°C | | | SN54ABT16833 | | SN74ABT16833 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | MAX | MIN | MAX | |
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = –18 mA | | | –1.2 | | –1.2 | | –1.2 | V |
| $V_{OH}$ | All outputs except $\overline{ERR}$ | $V_{CC}$ = 4.5 V, | $I_{OH}$ = –3 mA | 2.5 | 3 | | 2.5 | | | | V |
| | | $V_{CC}$ = 5 V, | $I_{OH}$ = –3 mA | 3 | 3.4 | | 3 | | 3 | | |
| | | $V_{CC}$ = 4.5 V | $I_{OH}$ = –24 mA | | | | 2 | | | | |
| | | | $I_{OH}$ = –32 mA | 2* | 2.7 | | | | 2 | | |
| $V_{OL}$ | | $V_{CC}$ = 4.5 V | $I_{OL}$ = 24 mA | | 0.25 | 0.55 | | 0.55 | | | V |
| | | | $I_{OL}$ = 64 mA | | 0.3 | 0.55* | | | | 0.55 | |
| $V_{hys}$ | | | | | 100 | | | | | | mV |
| $I_{OH}$ | $\overline{ERR}$ | $V_{CC}$ = 4.5 V, | $V_{OH}$ = 5.5 V | | | 20 | | 20 | | 20 | µA |
| $I_{off}$ | | $V_{CC}$ = 0, | $V_I$ or $V_O \le$ 4.5 V | | | ±100 | | | | ±100 | µA |
| $I_{CEX}$ | Outputs high | $V_{CC}$ = 5.5 V, | $V_O$ = 5.5 V | | | 50 | | 50 | | 50 | µA |
| $I_I$ | Control inputs | $V_{CC}$ = 5.5 V, $V_I$ = $V_{CC}$ or GND | | | | ±1 | | ±1 | | ±1 | µA |
| | A or B ports | | | | | ±100 | | ±100 | | ±100 | |
| $I_{IL}$ | A or B ports | $V_{CC}$ = 0, | $V_I$ = GND | | | –50 | | –50 | | –50 | µA |
| $I_O$‡ | | $V_{CC}$ = 5.5 V, | $V_O$ = 2.5 V | –50 | –100 | –180 | –50 | –180 | –50 | –180 | mA |
| $I_{OZH}$§ | | $V_{CC}$ =5.5 V, | $V_O$ = 2.7 V | | | 50 | | 50 | | 50 | µA |
| $I_{OZL}$§ | | $V_{CC}$ = 5.5 V, | $V_O$ = 0.5 V | | | –50 | | –50 | | –50 | µA |
| $I_{CC}$ | A or B ports | $V_{CC}$ = 5.5 V, $I_O$ = 0, $V_I$ = $V_{CC}$ or GND | Outputs high | | 1.5 | 2 | | 2 | | 2 | mA |
| | | | Outputs low | | 28 | 36 | | 36 | | 36 | |
| | | | Outputs disabled | | 1 | 2 | | 2 | | 2 | |
| $\Delta I_{CC}$¶ | | $V_{CC}$ = 5.5 V, One input at 3.4 V, Other inputs at $V_{CC}$ or GND | | | | 50 | | 50 | | 50 | µA |
| $C_i$ | Control inputs | $V_I$ = 2.5 V or 0.5 V | | | 3 | | | | | | pF |
| $C_{io}$ | A or B ports | $V_O$ = 2.5 V or 0.5 V | | | 9 | | | | | | pF |

* On products compliant to MIL-PRF-38535, this parameter does not apply.
† All typical values are at $V_{CC}$ = 5 V.
‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
§ The parameters $I_{OZH}$ and $I_{OZL}$ include the input leakage current.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}$ or GND.

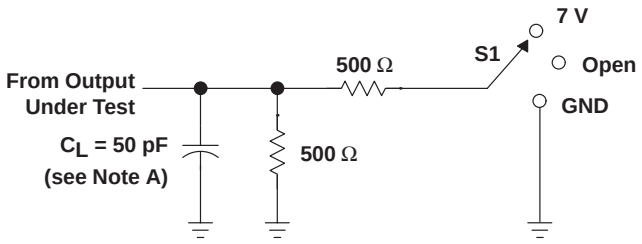
**timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)**

| | | | $V_{CC}$ = 5 V, $T_A$ = 25°C | | SN54ABT16833 | | SN74ABT16833 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration, CLK high or low | | 3 | | 3 | | 3 | | ns |
| $t_{su}$ | Setup time before CLK↑ | A port | 4.5 | | 4.5 | | 4.5 | | ns |
| | | $\overline{CLR}$ | 1 | | 1 | | 1 | | |
| | | $\overline{OEA}$ | 5 | | 5 | | 5 | | |
| $t_h$ | Hold time after CLK↑ | A port or $\overline{OEA}$ | 0 | | 0 | | 0 | | ns |

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | SN54ABT16833 | | SN74ABT16833 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A or B | B or A | 1.5 | 2.5 | 3.3 | 1.5 | 4.2 | 1.5 | 4.1 | ns |
| $t_{PHL}$ | | | 2 | 3.1 | 3.9 | 2 | 4.5 | 2 | 4.3 | |
| $t_{PZH}$ | $\overline{OE}$ | A or B | 2 | 3.9 | 4.9 | 2 | 5.8 | 2 | 5.6 | ns |
| $t_{PZL}$ | | | 2.5 | 4.3 | 5.1 | 2.5 | 6.2 | 2.5 | 6 | |
| $t_{PHZ}$ | $\overline{OE}$ | A or B | 2 | 3.6 | 4.5 | 2 | 5.5 | 2 | 5.4 | ns |
| $t_{PLZ}$ | | | 1.5 | 3 | 3.8 | 1.5 | 4.7 | 1.5 | 4.3 | |
| $t_{PLH}$ | A or $\overline{OE}$ | PARITY | 2 | 4.6 | 5.4 | 2 | 7 | 2 | 6.7 | ns |
| $t_{PHL}$ | | | 2 | 4.3 | 5.1 | 2 | 6.5 | 2 | 6.1 | |
| $t_{PZH}$ | $\overline{OE}$ | PARITY | 2 | 3.6 | 5 | 2 | 5.8 | 2 | 5.7 | ns |
| $t_{PZL}$ | | | 2.5 | 4.4 | 5.8 | 2.5 | 6.7 | 2.5 | 6.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | PARITY | 1.5 | 3.2 | 4 | 1.5 | 4.8 | 1.5 | 4.7 | ns |
| $t_{PLZ}$ | | | 1.5 | 2.9 | 3.7 | 1.5 | 4.2 | 1.5 | 4.1 | |
| $t_{PLH}$ | CLK, $\overline{CLR}$ | $\overline{ERR}$ | 2 | 3.4 | 4.2 | 2 | 4.8 | 2 | 4.6 | ns |
| $t_{PHL}$ | CLK | | 2 | 2.8 | 3.6 | 2 | 4.1 | 2 | 3.9 | |

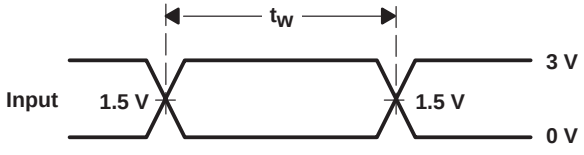
## PARAMETER MEASUREMENT INFORMATION



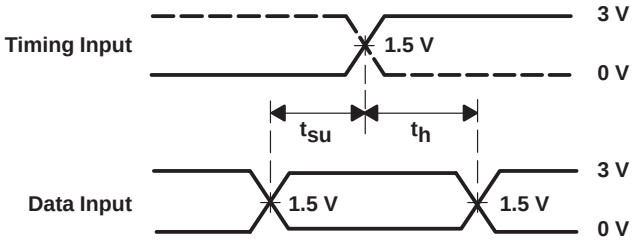

LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 7 V |
| $t_{PHZ}/t_{PZH}$ | Open |

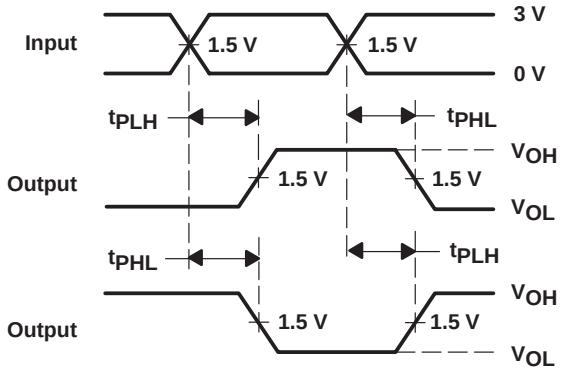
| $\overline{ERR}$ | S1 |
|---|---|
| $t_{PHL}$ (see Note E) | 7 V |
| $t_{PLH}$ (see Note F) | 7 V |



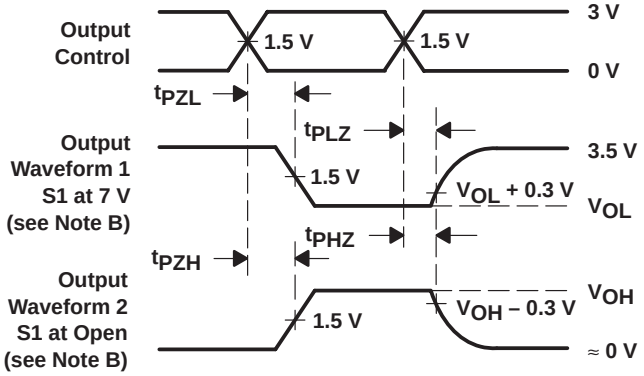

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. $t_{PHL}$ is measured at 1.5 V.
F. $t_{PLH}$ is measured at $V_{OL}$ + 0.3 V.

**Figure 1. Load Circuit and Voltage Waveforms**

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