

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static-Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Buffered Clock and Direct-Clear Inputs
- Individual Data Input to Each Flip-Flop
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- I_{off} Supports Partial-Power-Down-Mode Operation
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and Ceramic (J) DIPs

description

These octal D-type flip-flops are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

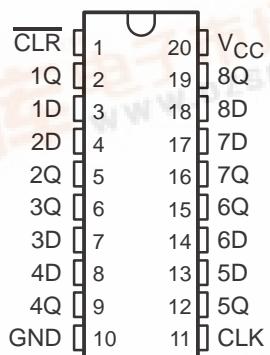
The 'LVTH273 devices are positive-edge-triggered flip-flops with a direct-clear input. Information at the data (D) inputs meeting the setup-time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock (CLK) input is at either the high or low level, the D-input signal has no effect at the output.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

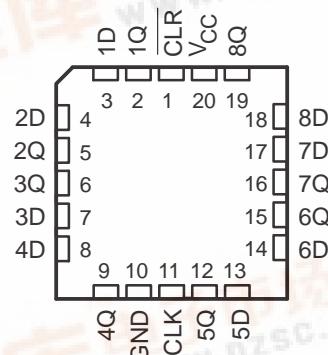
These devices are fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

The SN54LVTH273 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LVTH273 is characterized for operation from -40°C to 85°C.

SN54LVTH273 . . . J PACKAGE
SN74LVTH273 . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVTH273 . . . FK PACKAGE
(TOP VIEW)



 Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

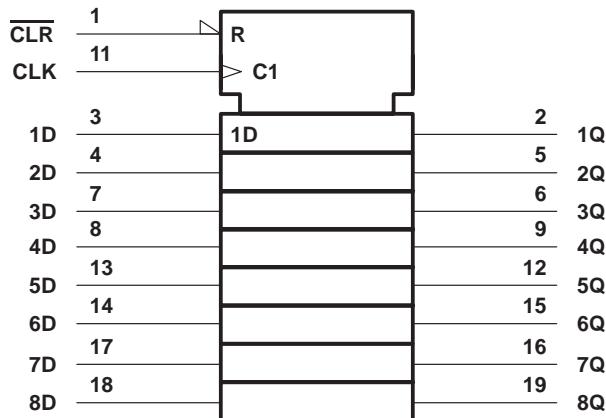
**SN54LVTH273, SN74LVTH273
3.3-V ABT OCTAL D-TYPE FLIP-FLOPS
WITH CLEAR**

SCBS136K – MAY 1992 – REVISED APRIL 1999

FUNCTION TABLE
(each flip-flop)

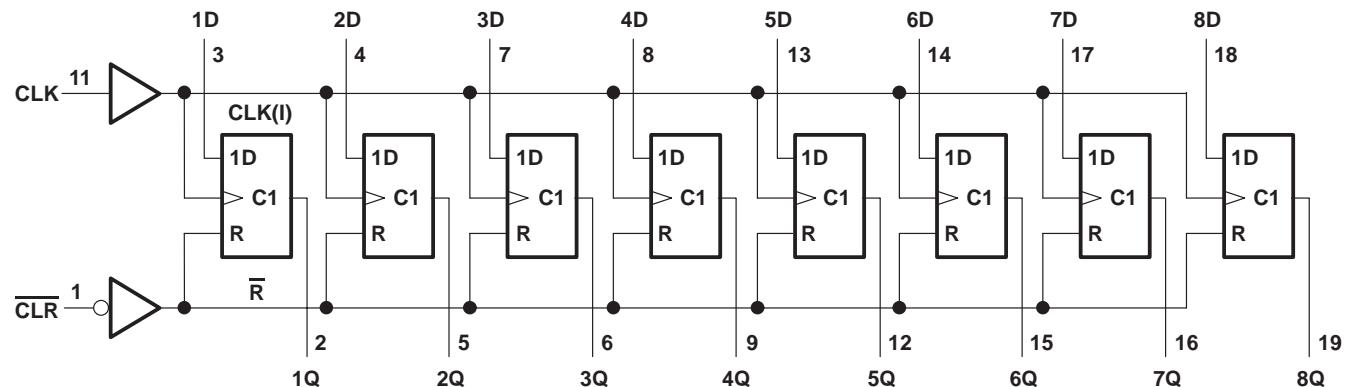
INPUTS			OUTPUT
CLR	CLK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	H or L	X	Q ₀

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



**SN54LVTH273, SN74LVTH273
3.3-V ABT OCTAL D-TYPE FLIP-FLOPS
WITH CLEAR**

SCBS136K – MAY 1992 – REVISED APRIL 1999

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
 3. The package thermal impedance is calculated in accordance with JEDEC 51.

recommended operating conditions (see Note 4)

		SN54LVTH273		SN74LVTH273		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
V _I	Input voltage		5.5		5.5	V
I _{OH}	High-level output current		-24		-32	mA
I _{OL}	Low-level output current		48		64	mA
Δt/Δv	Input transition rise or fall rate		10		10	ns/V
T _A	Operating free-air temperature	-55	125	-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**SN54LVTH273, SN74LVTH273
3.3-V ABT OCTAL D-TYPE FLIP-FLOPS
WITH CLEAR**

SCBS136K – MAY 1992 – REVISED APRIL 1999

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54LVTH273			SN74LVTH273			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$V_{CC} = 2.7 \text{ V}$, $I_I = -18 \text{ mA}$			-1.2			-1.2	V
V_{OH}	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$, $I_{OH} = -100 \mu\text{A}$	$V_{CC} - 0.2$			$V_{CC} - 0.2$			V
	$V_{CC} = 2.7 \text{ V}$, $I_{OH} = -8 \text{ mA}$	2.4			2.4			
	$V_{CC} = 3 \text{ V}$	$I_{OH} = -24 \text{ mA}$	2				2	
		$I_{OH} = -32 \text{ mA}$						
V_{OL}	$V_{CC} = 2.7 \text{ V}$	$I_{OL} = 100 \mu\text{A}$		0.2			0.2	V
		$I_{OL} = 24 \text{ mA}$		0.5			0.5	
	$V_{CC} = 3 \text{ V}$	$I_{OL} = 16 \text{ mA}$		0.4			0.4	
		$I_{OL} = 32 \text{ mA}$		0.5			0.5	
		$I_{OL} = 48 \text{ mA}$		0.55				
		$I_{OL} = 64 \text{ mA}$					0.55	
I_I	$V_{CC} = 0 \text{ or } 3.6 \text{ V}$, $V_I = 5.5 \text{ V}$			10			10	μA
	Control inputs	$V_{CC} = 3.6 \text{ V}$, $V_I = V_{CC} \text{ or GND}$		± 1			± 1	
	Data inputs	$V_{CC} = 3.6 \text{ V}$	$V_I = V_{CC}$	1			1	
		$V_{CC} = 3.6 \text{ V}$	$V_I = 0$	-5			-5	
I_{off}	$V_{CC} = 0$, $V_I \text{ or } V_O = 0 \text{ to } 4.5 \text{ V}$						± 100	μA
$I_I(\text{hold})$	Data inputs	$V_{CC} = 3 \text{ V}$	$V_I = 0.8 \text{ V}$	75			75	μA
			$V_I = 2 \text{ V}$	-75			-75	
		$V_{CC} = 3.6 \text{ V} \ddagger$	$V_I = 0 \text{ to } 3.6 \text{ V}$				500 -750	
I_{CC}	$V_{CC} = 3.6 \text{ V}$, $I_O = 0$, $V_I = V_{CC} \text{ or GND}$	Outputs high		0.19			0.19	mA
		Outputs low		5			5	
$\Delta I_{CC} \S$	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$, One input at $V_{CC} - 0.6 \text{ V}$, Other inputs at V_{CC} or GND			0.2			0.2	mA
C_I	$V_I = 3 \text{ V or } 0$			4			4	pF

† All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			SN54LVTH273		SN74LVTH273		UNIT	
			$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CC} = 2.7 \text{ V}$			
			MIN	MAX	MIN	MAX		
f_{clock}	Clock frequency		150			150		MHz
t_W	Pulse duration		3.3		3.3	3.3	3.3	ns
t_{SU}	Setup time	Data high or low before $\text{CLK} \uparrow$	2.3		2.7	2.3	2.7	ns
		CLR high before $\text{CLK} \uparrow$	2.3		2.7	2.3	2.7	
t_H	Hold time, data high or low after $\text{CLK} \uparrow$		0		0	0	0	ns

SN54LVTH273, SN74LVTH273
3.3-V ABT OCTAL D-TYPE FLIP-FLOPS
WITH CLEAR

SCBS136K – MAY 1992 – REVISED APRIL 1999

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

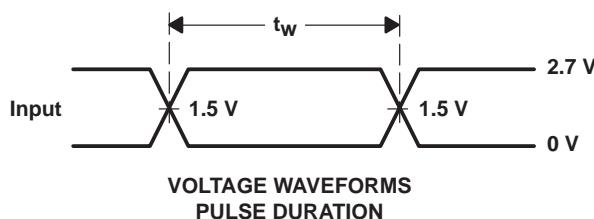
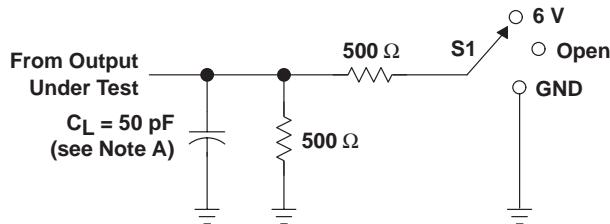
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH273				SN74LVTH273				UNIT
			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYPT [†]	MAX	MIN	MAX
f _{max}			150				150				MHz
t _{PLH}	CLK	Any Q	1.6	5	5.6	1.7	3.2	4.9		5.5	ns
			1.8	4.9	5.2	1.9	3.2	4.8		5.1	
t _{PHL}	CLR	Any Q	1.5	4.4	4.8	1.6	2.7	4.3		4.7	ns

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

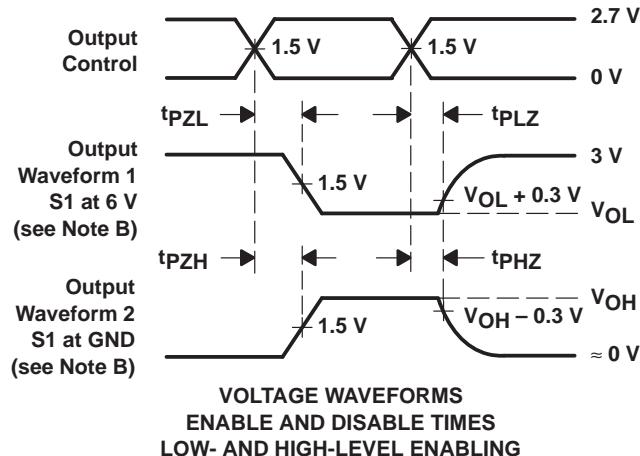
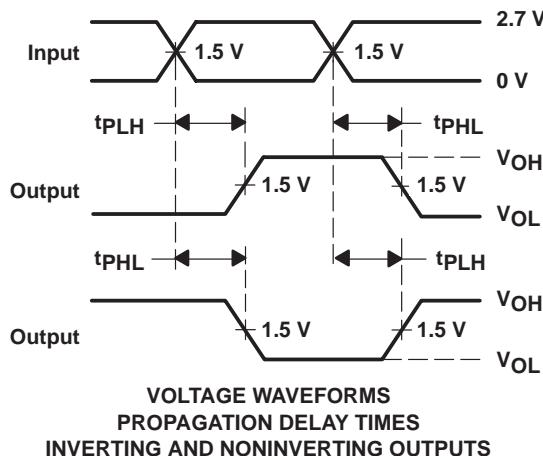
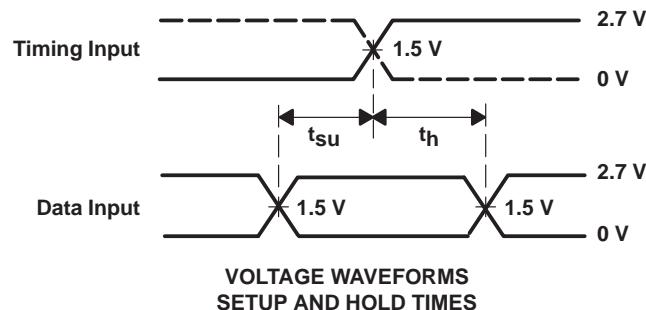
**SN54LVTH273, SN74LVTH273
3.3-V ABT OCTAL D-TYPE FLIP-FLOPS
WITH CLEAR**

SCBS136K – MAY 1992 – REVISED APRIL 1999

PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



NOTES:

- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
- The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.