SN54ABT863, SN74ABT863
9-BIT BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

SCBS201E – FEBRUARY 1991 – REVISED JULY 1998

- **State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **High-Impedance State During Power Up and Power Down**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Latch-Up Performance Exceeds 500 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB) Packages, and Thin Shrink Small-Outline (PW), Ceramic Chip Carriers (FK), Plastic (NT), and Ceramic (JT) DIPs**

description

The 'ABT863 devices are 9-bit transceivers designed for asynchronous communication between data buses. The control-function implementation allows for maximum flexibility in timing.
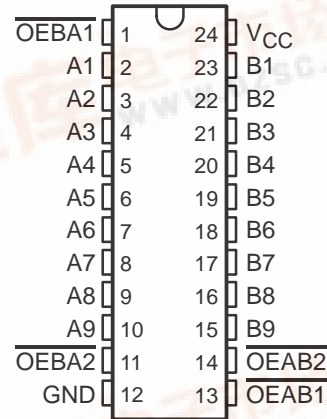
These devices allow noninverted data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic levels at the output-enable ($\overline{OEAB}$ and $\overline{OEBA}$) inputs.

The outputs are in the high-impedance state during power up and power down. The outputs remain in the high-impedance state while the device is powered down.
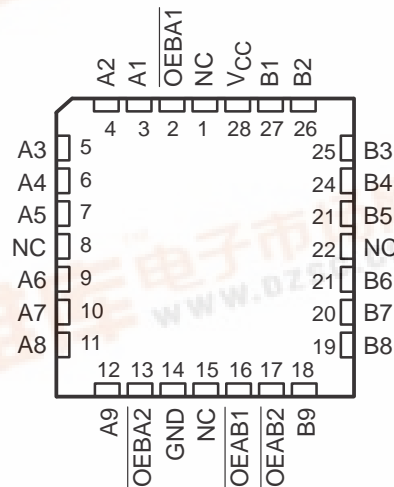
When V_{CC} is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT863 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT863 is characterized for operation from –40°C to 85°C.

SN54ABT863 . . . JT PACKAGE
SN74ABT863 . . . DB, DW, NT, OR PW PACKAGE
(TOP VIEW)

$\overline{OEBA1}$	1	24 V_{CC}
A1	2	23 B1
A2	3	22 B2
A3	4	21 B3
A4	5	20 B4
A5	6	19 B5
A6	7	18 B6
A7	8	17 B7
A8	9	16 B8
A9	10	15 B9
$\overline{OEBA2}$	11	14 $\overline{OEAB2}$
GND	12	13 $\overline{OEAB1}$

SN54ABT863 . . . FK PACKAGE
(TOP VIEW)

Top pins (4 3 2 1 28 27 26): A2, A1, $\overline{OEBA1}$, NC, V_{CC}, B1, B2

left	pin		pin	right
A3	5		25	B3
A4	6		24	B4
A5	7		21	B5
NC	8		22	NC
A6	9		21	B6
A7	10		20	B7
A8	11		19	B8

Bottom pins (12 13 14 15 16 17 18): A9, $\overline{OEBA2}$, GND, NC, $\overline{OEAB1}$, $\overline{OEAB2}$, B9

NC – No internal connection

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FUNCTION TABLE

INPUTS				OPERATION
$\overline{OEAB1}$	$\overline{OEAB2}$	$\overline{OEBA1}$	OEBA2	
L	L	L	L	Latch A and B
L	L	H	X	A to B
L	L	X	H	
H	X	L	L	B to A
X	H	L	L	
H	X	H	X	Isolation
H	X	X	H	
X	H	X	H	
X	H	H	X	

logic symbol†
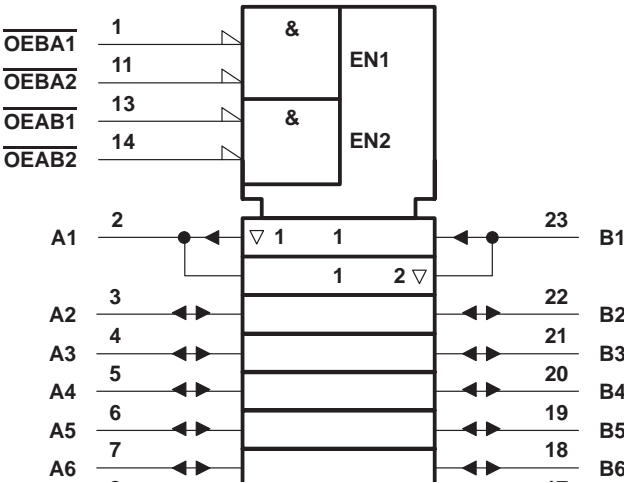
logic diagram (positive logic)

To Eight Other Channels
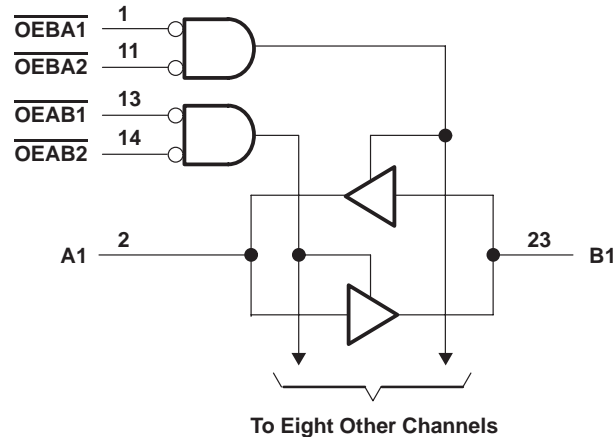
Pin numbers shown are for the DB, DW, JT, NT, and PW packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... –0.5 V to 7 V

Input voltage range, V_I (except I/O ports) (see Note 1) .... –0.5 V to 7 V

Voltage range applied to any output in the high or power-off state, V_O .... –0.5 V to 5.5 V

Current into any output in the low state, I_O: SN54ABT863 .... 96 mA

SN74ABT863 .... 128 mA

Input clamp current, I_{IK} ($V_I < 0$) .... –18 mA

Output clamp current, I_{OK} ($V_O < 0$) .... –50 mA

Package thermal impedance, θ_{JA} (see Note 2): DB package .... 104°C/W

DW package .... 81°C/W

NT package .... 67°C/W

PW package .... 120°C/W

Storage temperature range, T_{stg} .... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

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recommended operating conditions (see Note 3)

			SN54ABT863		SN74ABT863		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		5		5	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200		200		μs/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 3:   All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		$T_A = 25°C$ MIN	TYP†	MAX	SN54ABT863 MIN	MAX	SN74ABT863 MIN	MAX	UNIT
V_{IK}		$V_{CC} = 4.5$ V,	$I_I = -18$ mA			−1.2		−1.2		−1.2	V
V_{OH}		$V_{CC} = 4.5$ V,	$I_{OH} = -3$ mA	2.5			2.5		2.5		V
		$V_{CC} = 5$ V,	$I_{OH} = -3$ mA	3			3		3		
		$V_{CC} = 4.5$ V	$I_{OH} = -24$ mA	2			2				
			$I_{OH} = -32$ mA	2*					2		
V_{OL}		$V_{CC} = 4.5$ V	$I_{OL} = 48$ mA			0.55		0.55			V
			$I_{OL} = 64$ mA			0.55*				0.55	
V_{hys}					100						mV
I_I	Control inputs	$V_{CC} = 0$ to 5.5 V,	$V_I = V_{CC}$ or GND			±1		±1		±1	μA
	A or B ports	$V_{CC} = 2.1$ V to 5.5 V,	$V_I = V_{CC}$ or GND			±20		±20		±20	
I_{OZPU}		$V_{CC} = 0$ to 2.1 V, $V_O = 0.5$ V to 2.7 V, $\overline{OE} = *$ don't care				±50		±50**		±50	μA
I_{OZPD}		$V_{CC} = 2.1$ V to 0, $V_O = 0.5$ V to 2.7 V, $\overline{OE} = *$ don't care				±50		±50**		±50	μA
I_{OZH}‡		$V_{CC} = 2.1$ V to 5.5 V, $V_O = 2.7$ V, $\overline{OE} \geq 2$ V				10		10		10	μA
I_{OZL}‡		$V_{CC} = 2.1$ V to 5.5 V, $V_O = 0.5$ V, $\overline{OE} \geq 2$ V				−10		−10		−10	μA
I_{off}		$V_{CC} = 0$,	V_I or $V_O \leq 4.5$ V			±100*				±100	μA
I_{CEX}		$V_{CC} = 5.5$ V, $V_O = 5.5$ V	Outputs high			50		50		50	μA
I_O§		$V_{CC} = 5.5$ V,	$V_O = 2.5$ V	−50	−100	−225	−50	−225	−50	−225	mA
I_{CC}	A or B ports	$V_{CC} = 5.5$ V, $I_O = 0$, $V_I = V_{CC}$ or GND	Outputs high		1	250		250		250	μA
			Outputs low		24	30		38		38	mA
			Outputs disabled		0.5	250		250		250	μA
ΔI_{CC}¶	Data inputs	$V_{CC} = 5.5$ V, One input at 3.4 V, Other inputs at V_{CC} or GND	Outputs enabled			1.5		1.5		1.5	mA
			Outputs disabled			0.05		0.05		0.05	
	Control inputs	$V_{CC} = 5.5$ V, One input at 3.4 V, Other inputs at V_{CC} or GND				1.5		1.5		1.5	
C_i	Control inputs	$V_I = 2.5$ V or 0.5 V			4						pF
C_{io}	A or B ports	$V_O = 2.5$ V or 0.5 V			7						pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.
** On products compliant to MIL-PRF-38535, this parameter is not production tested.
† All typical values are at $V_{CC} = 5$ V.
‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
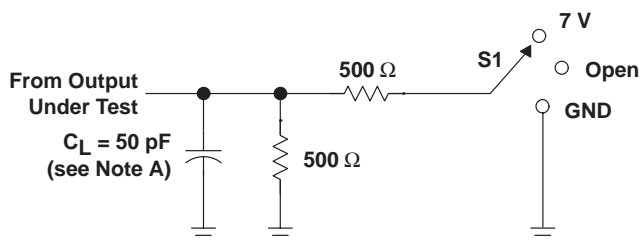
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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT863		SN74ABT863		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1	2.6	4.1	1	7	1	5.7	ns
t_{PHL}			1	2.3	3.3	1	3.9	1	3.9	
t_{PZH}	$\overline{OEAB}$ or $\overline{OEBA}$	B or A	1	3.2	4.3	1	5.4	1	5.5	ns
t_{PZL}			1	3.3	4.4	1	5.5	1	5.4	
t_{PHZ}	$\overline{OEAB}$ or $\overline{OEBA}$	B or A	2.5	4.8	6	2.5	6.8	2.5	6.7	ns
t_{PLZ}			1.5	4.4	5.9	1.5	7.8	1.5	6.9	

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PARAMETER MEASUREMENT INFORMATION

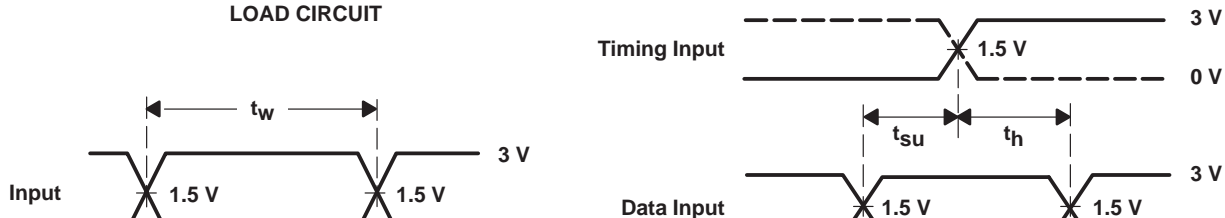| TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

Figure 1. Load Circuit and Voltage Waveforms

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