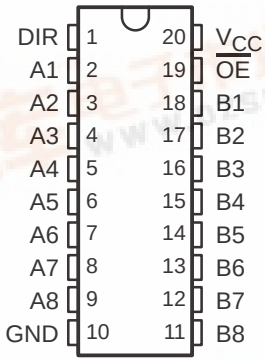
# CD74FCT245
# BiCMOS OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCBS721 – JULY 2000

- **BiCMOS Technology With Low Quiescent Power**
- **Buffered Inputs**
- **Noninverted Outputs**
- **Input/Output Isolation From $V_{CC}$**
- **Controlled Output Edge Rates**
- **64-mA Output Sink Current**
- **Output Voltage Swing Limited to 3.7 V**
- **SCR Latch-Up-Resistant BiCMOS Process and Circuit Design**
- **Package Options Include Plastic Small-Outline (M) and Shrink Small-Outline (SM) Packages and Standard Plastic (E) DIP**

**E, M, OR SM PACKAGE**
**(TOP VIEW)**




## description

The CD74FCT245 is an octal bus transceiver with 3-state outputs using a small-geometry BiCMOS technology. The output stages are a combination of bipolar and CMOS transistors that limit the output high level to two diode drops below $V_{CC}$. This resultant lowering of output swing (0 V to 3.7 V) reduces the power-bus ringing [a source of electromagnetic interference (EMI)] and minimizes $V_{CC}$ bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 64 mA.

The CD74FCT245 allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so that the buses are effectively isolated.

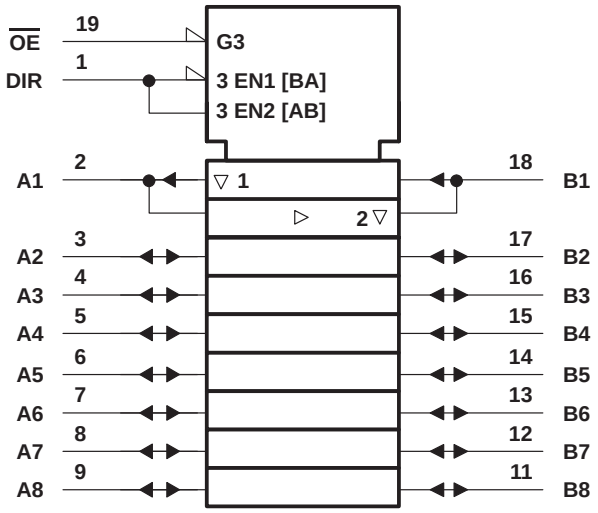
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The CD74FCT245 is characterized for operation from 0°C to 70°C.

**FUNCTION TABLE**

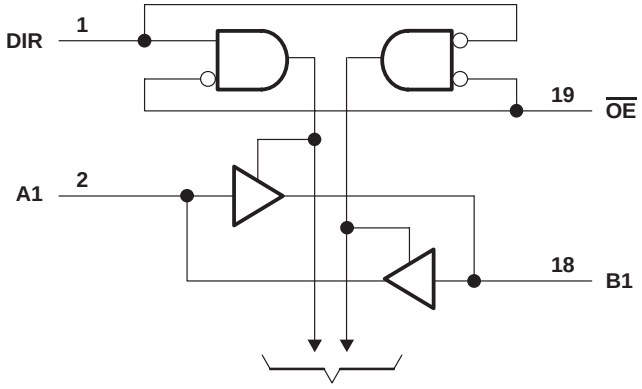
| INPUTS | | OPERATION |
|---|---|---|
| $\overline{OE}$ | DIR | |
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

DC supply voltage range, $V_{CC}$ . . . . . –0.5 V to 6 V
DC input clamp current, $I_{IK}$ ($V_I$ < –0.5 V) . . . . . –20 mA
DC output clamp current, $I_{OK}$ ($V_O$ < –0.5 V) . . . . . –50 mA
DC output sink current per output pin, $I_{OL}$) . . . . . 70 mA
DC output source current per output pin, $I_{OH}$) . . . . . –30 mA
Continuous current through $V_{CC}$, $I_{CC}$) . . . . . 140 mA
Continuous current through GND) . . . . . 528 mA
Package thermal impedance, $\theta_{JA}$ (see Note 1): E package) . . . . . 69°C/W
M package) . . . . . 58°C/W
SM package) . . . . . 70°C/W
Storage temperature range, $T_{stg}$) . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51.

### recommended operating conditions (see Note 2)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 4.75 | 5.25 | V |
| $V_{IH}$ | High-level input voltage | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | V |
| $V_I$ | Input voltage | 0 | $V_{CC}$ | V |
| $V_O$ | Output voltage | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –15 | mA |
| $I_{OL}$ | Low-level output current | | 64 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | 0 | 10 | ns/V |
| $T_A$ | Operating free-air temperature | 0 | 70 | °C |

NOTE 2: All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | $V_{CC}$ | $T_A$ = 25°C | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | | | |
| $V_{IK}$ | $I_I$ = –18 mA | | 4.75 V | | –1.2 | | –1.2 | V |
| $V_{OH}$ | $I_{OH}$ = –15 mA | | 4.75 V | 2.4 | | 2.4 | | V |
| $V_{OL}$ | $I_{OL}$ = 64 mA | | 4.75 V | | 0.55 | | 0.55 | V |
| $I_I$ | $V_I = V_{CC}$ or GND | | 5.25 V | | ±0.1 | | ±1 | µA |
| $I_{OZ}$ | $V_O = V_{CC}$ or GND | | 5.25 V | | ±0.5 | | ±10 | µA |
| $I_{OS}$‡ | $V_I = V_{CC}$ or GND, | $V_O$ = 0 | 5.25 V | –60 | | –60 | | mA |
| $I_{CC}$ | $V_I = V_{CC}$ or GND, | $I_O$ = 0 | 5.25 V | | 8 | | 80 | µA |
| $\Delta I_{CC}$§ | One input at 3.4 V,<br>Other inputs at $V_{CC}$ or GND | | 5.25 V | | 1.6 | | 1.6 | mA |
| $C_i$ | $V_I = V_{CC}$ or GND | | | | 10 | | 10 | pF |
| $C_o$ | $V_O = V_{CC}$ or GND | | | | 15 | | 15 | pF |

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed 100 ms.
§ This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$.

### switching characteristics over recommended operating conditions (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $T_A$ = 25°C TYP | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{pd}$ | A or B | B or A | 5 | 1.5 | 7 | ns |
| $t_{en}$ | $\overline{OE}$ | A or B | 6 | 1.5 | 9.5 | ns |
| $t_{dis}$ | $\overline{OE}$ | A or B | 6 | 1.5 | 7.5 | ns |

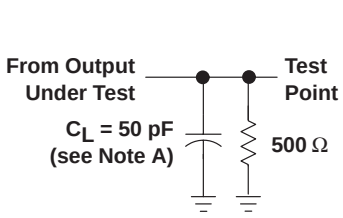
### noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 1 | | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | 0.5 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 0.8 | V |

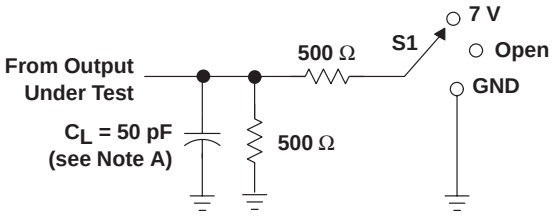
### operating characteristics, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, f = 1 MHz | 49 | pF |

## PARAMETER MEASUREMENT INFORMATION

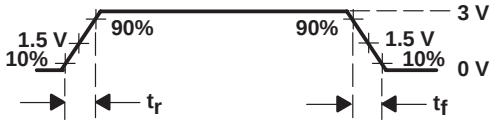



LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

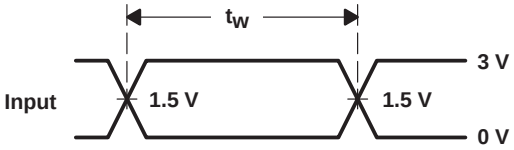



LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

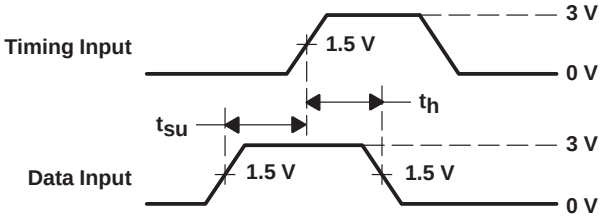
| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 7 V |
| $t_{PHZ}/t_{PZH}$ | Open |
| Open Drain | 7 V |



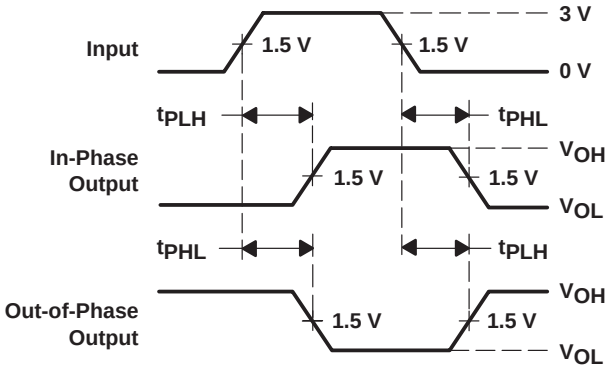

VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



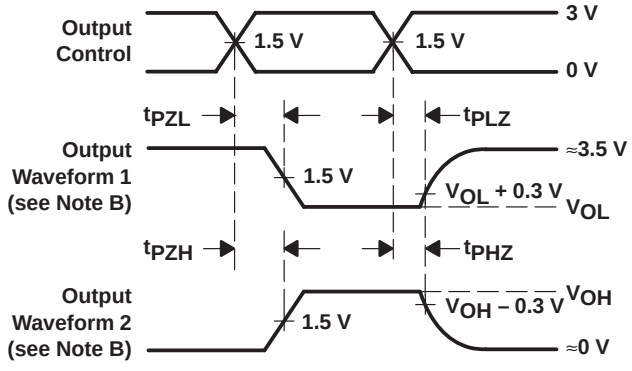

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ and $t_f$ = 2.5 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PHL}$ and $t_{PLH}$ are the same as $t_{pd}$.

**Figure 1. Load Circuit and Voltage Waveforms**

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